Parasitics and Current-Dispersion Modeling of AlGaN/GaN HEMTs Fabricated on Different Substrates using the Equivalent-Circuit Modeling Technique

Mohamad Alsabbagh, B.S.

uOttawa

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Ottawa-Carleton Institute for Electrical and Computer Engineering

School of Electrical Engineering and Computer Sciences

University of Ottawa

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Abstract

Electrical equivalent circuit modeling of active components is one of the most important approaches for modeling high-frequency high-power devices. Amongst the most used microwave devices, AlGaN/GaN HEMTs demonstrated their superior performance, making them highly suitable for 5G, wireless and satellite communications. Despite the remarkable performance of AlGaN/GaN HEMTs, these devices reside on substrates that invoke limitations on the operating-frequency, power-efficiency, and current dispersion phenomenon. Also, there is a limitation in present parameters extraction techniques being not able to consider both the substrate effect (Silicon, Silicon Carbide, and Diamond) and the asymmetrical GaN HEMT structure. In this thesis work, a single extrinsic parameters extraction technique using a single small-signal topology takes into account both the asymmetrical GaN HEMT structure and the different substrate types with their parasitic conduction will be developed and studied for the first time. Moreover, large-signal modeling using Quasi-Physical Zone Division technique has been applied to both GaN/D and GaN/SiC to model the isothermal-trapping free drain current, and combined with a new simple technique for comparing performance between active devices in terms of current-dispersion. The models were verified by simulating the small-signal *S*-parameters, large-signal IV characteristics, and single-tone load-pull. High accuracy was achieved compared to the measurement data available in the technical literature and obtained from fabricated devices.

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List of Symbols

$\Delta E_c(x)$	Conduction band offset at the AlGaN/GaN interface
μ_0	Low-field electron mobility
μ_{eff}	Effective electron mobility
C_{dd}	Parasitic conduction drain capacitance
C_{ds}	Intrinsic drain-to-source capacitance
C_{dsi}	Drain-to-source inter-electrode capacitance
C_{eff}	Effective gate capacitance per unit area
C_{gd}	Intrinsic gate-to-drain capacitance
C_{gd1}	Gate-to-drain depletion region capacitance
C_{gd2}	Capacitance between the gate and the GaN cap from drain side
C_{gdf}, C_{gdi}	Gate-to-drain inter-electrode capacitance
C_{gdp}	Feedback pad capacitance
C_{gg}	Parasitic conduction gate capacitance
C_{gs}	Intrinsic gate-to-source capacitance
C_{gs1}	Gate-to-source depletion region capacitance
C_{gs2}	Capacitance between the gate and the GaN cap from source side
C_{gsf}, C_{gsi}	Gate-to-source inter-electrode capacitance
C_m	Miller capacitance
C_{pd}	Drain pad capacitance
C_{pg}	Gate pad capacitance
C_{th}	Thermal capacitance

D	Effective density of quantum states
d	Thickness of AlGaN layer
E	Electric field
E_1	Second lowest quantized energy in 2DEG
E_c	Critical electric field
E_f	Position of the Fermi level
$\mathrm{E_{NET}}$	Induced electric field in AlGaN
E_o	Lowest quantized energy in 2DEG
f_{max}	Unity power-gain cutoff frequency
f_t	Unity current-gain cutoff frequency
G_{ds}, R_{ds}	Drain-to-source channel length modulation conductance/ resistance
G_{gdf}, R_{gdf}	Breakdown gate conduction / resistance
G_{gsf}, R_{gsf}	Forward gate conduction / resistance
G_m	Channel transconductance
G_{max}	The maximum power gain
h_{21}	short-circuit current gain
I_d, I_{ds}	Drain-to-source current
I_{ds}^{DC}	Measured DC current
I_{dso}	Isothermal trapping-free drain current
I_{dsp}	Pulsed drain current
I_{dsq}	Quiescent bias drain current value
I_{ds}^{RF}	RF DC current

I_g, I_{gs}	Gate current
I_{sat}	Maximum current achievable
L	Channel length
l_d	Drain access length
l_s	Source access length
N_d	Doping concentration of n-AlGaN layer
n_s	Density of 2DEG
P_{in}	RF input power
P_{out}	RF output power
$\mathrm{P_{PE}}$	Piezoelectric Polarization
$\mathrm{P_{SP}}$	Spontaneous Polarization
q	Electronic charge
Q_d	Quasi-static drain charge
Q_g	Quasi-static gate charge
Q_{gd}	Non Quasi-static gate-to-drain charge
Q_{gs}	Non Quasi-static gate-to-source charge
R_d	Drain electrode resistance
R_{dd}	Parasitic conduction drain resistance
R_{dp}	Shunt pad resistance at the drain side
R_{DT}, C_{DT}	Model for low frequency transition and trapping-effects at drain side
R_g	Gate metal resistance
R_{gd}	Depletion charging/discharging resistance from drain side

R_{gg}	Parasitic conduction gate resistance
R_{gp}	Shunt pad resistance at the gate side
R_{GT}, C_{GT}	Model for low frequency transition and trapping-effects at gate side
R_i	Depletion charging/discharging resistance at source side
R_s	Source electrode resistance
R_{th}	Thermal Resistance
S	Small-signal scattering parameter
v	Electron velocity
V_{br}	Breakdown voltage
V_{di}	Intrinsic drain voltage in zone division model
V_{DS}, V_{ds}	Drain-to-source voltage
V_{DSQ}, V_{dsq}	Drain-to-source quiescent bias
V_{dsqf}	Drain-to-source final quiescent bias point
V_{dsqi}	Drain-to-source initial quiescent bias point
V_{eff}	Effective gate-to-source voltage
V_{GS}, V_{gs}	Gate-to-source voltage
V_{GSQ}, V_{gsq}	Gate-to-source quiescent bias
V_{gsqf}	Gate-to-source final quiescent bias point
V_{gsqi}	Gate-to-source initial quiescent bias point
V_k	Knee voltage
V_p	Pinch-off voltage
v_{sat}	Electron Saturation Velocity

V_{si}	Intrinsic source voltage in zone division model
v_t	Thermal voltage at room temperature
V_{TH}	Self-heating voltage
W	Width of the channel
X	Wolf's position vector
X_p	Prey's position vector
Y	Small-signal admittance parameter
Y_{dd}	Admittance of the substrate network from drain side
Y_{ds}	Intrinsic drain-to-source admittance
Y_{gd}	Intrinsic gate-to-drain admittance
Y_{gg}	Admittance of the substrate network from gate side
Y_{gm}	Admittance of the intrinsic transconductance
Y_{gs}	Intrinsic gate-to-source admittance
Y_i	Intrinsic Y-parameters
Z	Small-signal impedance parameter
Z_1	Source Neutral Zone
Z_2	Intrinsic FET Zone
Z_3	Drain Neutral Zone
Z_o	Reference Impedance (50 Ω)
α	Ratio of gate-to-source capacitance to gate-to-drain capacitance
α_D	Fitting parameter for buffer-trapping effect
α_G	Fitting parameter for surface-trapping effect

α_T	Fitting parameter for self-heating effect
α_w	Leader of the wolf pack
β	Ratio of drain-to-source capacitance to gate-to-drain capacitance
β_w	Second best wolf
γ_0	Experimentally-measured value for E_0
γ_1	Experimentally-measured value for E_1
δ	Velocity saturation factor
δ_w	Third best wolf
ε	Percentage Error
ε_{AlGaN}	Permittivity of the AlGaN layer
Θ_1	First-order fitting parameter for the effective mobility
Θ_2	Second-order fitting parameter for the effective mobility
λ	Channel length modulation parameter
$\sigma(x)$	Polarization charge density
τ	Electron transit time
τ_{DT}	Buffer-traps time constant
τ_{GT}	Surface-traps time constant
τ_{th}	Self-heat time constant
$\phi_B(x)$	Schottky Barrier Height
ω	Frequency in rad/s
ω_w	Other wolves
Φ_{sd}	Surface potential at the drain side

Φ_{sm}	Average surface potential
Φ_{ss}	Surface potential at the source side

List of Abbreviations

2DEG	Two-Dimensional Electron Gas
ADS	Advanced Design System
CAD	Computer-Aided Design
CVD	Chemical Vapor Deposition
CW	Continuous-wave
DAC	Data Access Component
DC	Direct Current
DUT	Device-Under-Test
EC-LSM	Equivalent Circuit- Large-signal Model
ECM	Equivalent Circuit Model
EC-SSM	Equivalent Circuit- Small-signal Model
FET	Field-Effect Transistor
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GaN/D	GaN on Diamond substrate
GaN/Si	GaN on Silicon substrate
GaN/SiC	GaN on Silicon Carbide substrate
GWO	Grey Wolf Optimizer
HEMT	High Electron Mobility Transistor
IMD	Intermodulation-Distortion
LNA	Low Noise Amplifier

MESFET	Metal–Semiconductor Field-Effect Transistor
MODFET	Modulation-Doped Field-Effect Transistor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
PA	Power Amplifier
PAE	Power Added Efficiency
QPZD	Quasi-Physical Zone Division
RF	Radio Frequency
SDD	Symbolic Defined Device
SiN	Silicon Mononitride
SP	Surface Potential
UHF	Ultra High Frequency
VNA	Vector Network Analyzer

Chapter 1: Introduction

1.1 Motivations

Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs) are very attractive devices for high-frequency high-power applications, such as in satellite and 5G communication systems [1]-[7]. In fact, GaN HEMTs are commonly used nowadays for the design of high-efficiency power amplifiers, mainly because of their large bandgap energy (resulting in high breakdown voltages), and high saturation velocity, due to the separation of the dopant atoms from the free charge carriers and polarization effects (which mitigate the effect of the impurity scattering effects) [8]. Consequently, GaN devices exhibit a large output power and high Power Added Efficiency (PAE). However, the high power density of GaN HEMTs results in an increase in their operating temperature, which deteriorates their PAE during normal and overloaded functioning conditions [9]. This issue has led to a reduction in device lifetime as well as negative current drift due to both the nucleation layer used in-between the GaN buffer and the substrate (to reduce lattice mismatch between them) and the thermal resistance associated with the substrate (this latter must be as low as possible to efficiently dissipate the heat through the substrate) [9]. There should be tradeoffs to have both reduced temperature resistance and acceptable lattice matching between the substrate and the GaN buffer [10]. Therefore, in order to reach the full potential and capabilities of the GaN HEMT, one should retain a substrate that has both low thermal resistance to reduce self-heating effects and high electrical resistance to reduce leakage current. Furthermore, it should adhere to the GaN buffer by using a suitable material that provides a very little lattice mismatch with the substrate in order to reduce charge-trapping effects.

To address this issue, several substrate materials have been utilized for GaN HEMTs, from which Silicon Carbide (SiC) and Silicon (Si) substrates are the most commonly used [11]. The GaN HEMT on SiC-substrate (GaN/SiC) is the state-of-the-art GaN HEMT. SiC exhibits moderate thermal conductivity with high electrical resistivity [9]. On the other side, the Si substrate of GaN on Si-substrate (GaN/Si) has a thermal conductivity that is about three times lower than GaN/SiC and high electrical resistivity (comparable to GaN/SiC) [9]. Due to the lower thermal resistivity of the GaN/SiC

compared to GaN/Si, it will have a lower self-heating effect associated with it, which will reduce the current dispersion and hence improve the PAE. This feature shows the primary reason behind the choice of GaN/SiC as a state-of-the-art device.

In 2006, the GaN HEMT on a diamond substrate (GaN/D) was demonstrated in [12]. Diamond has a thermal conductivity that is two- to four-times the thermal conductivity of SiC. Therefore, the GaN/D can have a 40% reduction in channel temperature, leading to a spacing between the gate fingers three-times smaller compared to GaN/SiC, without worrying about thermal crosstalk. This implies, in theory, an expected output power three-times larger than that of GaN/SiC while maintaining thermal reliability [9]. Also, diamond has an electrical resistivity of about 10 orders of magnitude larger than SiC. Furthermore, its high substrate resistivity, with the potential of having good matching between the GaN buffer and diamond substrate, could lead to a tremendous improvement in PAE by reduced self-heating effects and leakage current induced by charge trapping effects [9]. It is clear that GaN/D holds valuable promises to the future of high-frequency high-power amplifier design due to its increased reliability of thermal management properties.

All of the above electrical characteristics, charge-trapping and self-heating effects, should be modeled to efficiently capture their impact and learn how to mitigate them. The electrical Equivalent Circuit Model (ECM) has been retained for the reason of good compromise between the physical model and the behavioral model [13]. It can also be relatively easy to integrate it in Computer-Aided Design (CAD) tools. The current dispersion due to buffer-charge-trapping, surface-charge-trapping, and self-heating effects can be modeled using the Equivalent Circuit-Large-signal Model (EC-LSM) [14]. Furthermore, pulsed IV measurements can allow us with the help of the EC-LSM to separate the three effects on current dispersion, allowing for more extensive studies on each distinctive effect, in order to reduce its impact. However, to develop an accurate EC-LSM, an accurate multi-biased Equivalent Circuit-Small-signal Model (EC-SSM) is required [14]. The EC-SSM can also describe the substrate electrical resistivity and the parasitic conduction through the substrate, which induces leakage current caused by buffer-trapping effects [15].

However, based on the technical literature, switching between different substrates implies considering different circuit models, thus, different extraction techniques for each circuit model. This approach increases complexity and obstructs the automation capabilities of the extractor. In addition to that, existing extraction techniques do not take into account both the asymmetrical GaN HEMT structure and the parasitic conduction through the substrate together, which does not work for asymmetrical devices that exhibit parasitic conduction through the substrate. A need for a single small-signal model that uses a single extraction technique for all types of GaN HEMTs should be studied regardless of the type of substrate used; it should also take into account the asymmetrical GaN HEMT structure and parasitic conduction effects in the extraction technique.

1.2 Literature Review

During the last three decades, numerous works have been proposed on developing various models and extraction techniques for the GaN HEMT that describe various physical and electrical characteristics. A large-signal modeling approach was applied to GaN/Si for RF high-power applications as presented in [15]. This model takes into account parasitic conduction through the substrate at lower frequencies as well as charge-trapping effects and self-heating effects associated with high-power applications. The obtained values were optimized using a hybrid optimization method that combines genetic and simplex optimization techniques. In 2004, a temperature-dependent model for continuous-wave (CW) and pulsed-mode operation was applied to GaN/SiC [16]. This model used pulsed measurements at various biases and temperatures to describe thermal and frequency dispersion using small- and large-signal GaN HEMT models. In [17], a general-purpose large-signal model for GaN and SiC MESFET devices was developed and evaluated using *DC*, *S*-parameters, and large-signal measurements. This model takes into account harmonics, which would describe physical dispersion and time delay of electrons to cross the channel. A table-based large-signal model for GaN HEMT on SiC substrate that takes into account charge-trapping and self-heating effects was developed in 2007 [18]. This model uses the *B*-spline-approximation technique for model-element construction that improves intermodulation-distortion (IMD) simulation. The intrinsic gate capacitances and conductances of the small-signal model were integrated in order to

develop the gate charge and current source of the large-signal model. Pulsed I-V measurements were used to characterize the current dispersion due to self-heating effects and charge-trapping effects under constant temperature. It was also found that using the *B*-spline approximation improves the I-V simulations. In [19], an empirical approach was used to deal with nonlinearly dynamic thermal effects. The model was most suitable for non-constant-envelope RF applications such as in pulsed radar. It uses Volterra's nonlinear system modeling theory; however, the series was modified in order to simplify the model. All of the above-mentioned papers depend on static I-V measurements, pulsed I-V measurements, and/or *S*-parameters measurements in order to develop both the EC-SSM and EC-LSM; they have also used different models depending on the type of substrate used for the GaN HEMT.

As for the parameter extraction of the extrinsic part of the EC-SSM, the existing extraction techniques differ in terms of complexity, accuracy, and type of topology implemented in the extrinsic part. In 1988, a paper addressing small-signal modeling for MOSFETs was presented [20]. The paper describes a direct extraction of the extrinsic and intrinsic parts of the small-signal model using a few simple matrix manipulations. It was verified that the model's *S*-parameters fit well up to 26.5 GHz. In [21], dedicated on-wafer test-structures were used to model the RF behavior of the Device-Under-Test (DUT). It proposes an improved three-step de-embedding to subtract the influence of parasitics and accurately model the RF behavior of the DUT. The paper in [22] showed that extremely high gate voltages have to be applied to correctly determine the series resistances of the extrinsic part of GaN HEMT's EC-SSM. The authors in [20] and [22] used cold pinch-off and forward *S*-parameters measurements at high gate voltage, while in [21], test structures were used to extract the extrinsic parameters. In 2006, a model parameter-extraction procedure for GaN HEMT was introduced showing that high gate voltage is not necessary to extract the parasitic inductances and resistances [23]. An efficient and accurate extraction algorithm for GaN HEMT was introduced in [24]; it uses only cold devices to extract all the extrinsic parameters without the need for forward *S*-parameter measurements. This model takes into account the time-delay in the output conductance as well. The work in [25] built a model that has 12 extrinsic components and developed an extraction technique that uses only cold pinch-off *S*-parameters

measurements. This model is applicable for large GaN HEMT devices with a 3.2 mm gate periphery. It shows high accuracy with measurements without the need for forward *S*-parameters measurements. The techniques described in [23]-[25] used pinch-off *S*-parameter measurements to extract the extrinsic inductances and resistances without relying on the forward *S*-parameters measurements. Although GaN HEMT circuit modeling is usually derived from linear conventional *S*-parameters; nonlinear scattering parameters, or "*X*-parameters" can also be used to model the HEMTs [26]. *X*-parameters are a superset of "small-signal" *S*-parameters and "large-signal" *S*-parameters. The main reason for using the *X*-parameters for modeling GaN HEMT devices is their ability to include the device behaviour at harmonics of the fundamental frequency at specific bias points. This leads to combining both the parameter extraction process and nonlinear modeling by incorporating the nonlinear *X*-parameter measurements. However, it was stated that *X*-parameters lead to improvements in the extracted parameters only via incorporating an artificial neural network, leading to additional complexity in the extraction procedure [26]. In addition to that, *X*-parameters do not describe the circuit structure of GaN HEMT, which leads to different conversion rules and equations to convert them to *S*-parameters, hence adding additional complexity [26]. *X*-parameters have great promising for the future of GaN modeling, but these behavioral-based measurements still impose difficulties in the field of GaN modeling.

A performance comparison between GaN/D and GaN/SiC was presented in [27]. The GaN/D and GaN/SiC were modeled using an EC-LSM in order to compare the extrinsic and the intrinsic parameters of both devices. However, no study was performed to evaluate the charge-trapping effects of both devices. The work in [28] used an EC-SSM that takes into account ambient temperature changes on the extrinsic and intrinsic parts of the EC-SSM for both GaN/D and GaN/SiC. Self-heating effects were investigated in [29] between the GaN/D and GaN/Si by performing a direct comparison between static DC and pulsed I-V measurements. It showed that self-heating effects are direr in GaN/Si compared to GaN/D due to the excellent thermal conductivity of the diamond substrate. No charge-trapping effects were studied in this reference. Most works in GaN/D are still in their early phases, thus requiring more extensive studies in order to improve the development and application of the GaN/D HEMT technology [28].

The above literature review is certainly not comprehensive since that there has been a great deal of work in the field of GaN HEMTs modeling; however, it provides the necessary information for the work presented in this thesis.

1.3 Objectives

As mentioned above, analyzing GaN HEMTs with different substrates will imply considering different topologies for the extrinsic network of the EC-SSM. This, in turn, will require multiple extraction techniques thus, increasing complexity. The first objective of this research work is to develop a single extraction technique for the extrinsic part of the EC-SSM of GaN HEMTs, assuming a unique EC-SSM, regardless of the substrate type. This model should be also applicable to different types of small-scaled high mobility devices. This technique would simplify the automation of the extractor and allows such an extraction technique to be applied for different devices with different substrate characteristics.

In [30], it was shown that due to asymmetrical device-structure, a passivation layer, and buffer-trapping effects, there will be an electric field rearrangement that will cause asymmetry between the gate-source side and gate-drain side as appose to typical MOSFET structures. This asymmetry should be considered in our extraction technique. To the best of the authors' knowledge, there is no existing extraction technique that takes into account both the asymmetrical GaN HEMT structure and the parasitic conduction through the substrate together. The proposed extraction technique takes into account, for the first time, both the asymmetrical GaN HEMT structure and the parasitic conduction effect. The extraction technique and its corresponding EC-SSM should be validated by using other devices such as Graphene-based FETs and as well as devices with different characteristics than GaN/D and GaN/SiC, such as the GaN/Si, which has parasitic conduction through the substrate at lower frequencies due to buffer-trapping effects.

The extracted parameters of the intrinsic and extrinsic parts will then undergo a new optimization technique for fine-tuning their values. The optimization technique is known as Grey Wolf Optimizer, which was shown that has high accuracy and high chances of avoiding local minima if the scanning range is small enough, which is quite suitable with

our extraction technique [31-33]. The next objective would be to implement the EC-LSM that takes into account the nonlinear characteristics of the GaN HEMT's drain-to-source current. The EC-LSM, with the addition of pulsed IV measurements, will allow us to separate the self-heating and charge-trapping effects that are superimposed on the I-V measurements. This step would, therefore, allow for a direct comparison of the performance of the GaN/D vs. the state-of-the-art GaN/SiC device, based on the separated effects. The EC-LSM will be implemented in the Advanced Design System (ADS) for validation purposes and used to simulate multiple class-AB power amplifiers (operating at different frequency ranges) to test bench our model and compare the results with the technical literature.

The objectives of this work may be summarized as follows:

- Develop an extraction technique that simplifies the automation of extracting the extrinsic part of GaN HEMT, even on different substrates.
- Take into account the asymmetry between the gate-source and gate-drain electric field distribution due to asymmetrical device-structure, passivation layer deposition, and buffer charge-traps. It should also take into account parasitic conduction through the substrate.
- Optimizing the extracted extrinsic and intrinsic parameter using Grey Wolf Optimizer, this tool is suitable for this type of problem due to its high accuracy and local minima avoidance enabled by the extraction technique.
- Extraction technique validation by applying it to GaN/Si, GaN/SiC and GaN/D, and by applying it on Graphene-based FETs.
- Develop the EC-LSM for both GaN/D and GaN/SiC and using the pulsed I-V measurements in order to model the self-heating and charge-trapping effects on current dispersion individually for each effect.
- Implement the model using ADS for both GaN/SiC and GaN/D.
- Test bench the models in ADS by applying the model into multiple class AB power amplifiers targeted for applications operating at the X band and/or UHF frequency range.

1.4 Original contributions

Original contributions can be highlighted from this work as:

- Proposing, for the first time, a single extraction technique for the extrinsic network, which uses a single EC-SSM that works accurately for major types of substrates of GaN HEMTs. This extraction technique takes into account both the asymmetrical GaN HEMT structure and the parasitic conduction through the substrate, which is a first in the field of GaN HEMT modeling.
- Also, for the first time, to the best of the authors' knowledge, comparing, individual effects of self-heating, surface-trapping, and buffer-trapping effects on current dispersion between GaN/D and GaN/SiC-based devices using empirical fitting parameters extracted from pulsed IV measurements.

1.5 Outline

Chapter 2 will be discussing the theoretical background of GaN HEMT necessary for modeling its behavior. We will be detailing the reasons behind choosing GaN HEMT as a candidate for high-power high-frequency circuit design, and its basic structures and physics. 2-DEG and polarization effects will be shown. Non-ideal effects that are of major concern when performing device modeling will be detailed. These non-ideal effects can be related to current dispersion due to self-heating effects and charge trapping effects, parasitics within the device, and the substrate choice. Measurement data necessary for this work will be discussed showing how each type of measurement is considered and how can they be utilized for building various circuit models. Finally, modeling approaches will be discussed showing how the equivalent circuit model compromises both the physical-based and the behavioral-based model.

Chapter 3 is mainly divided into two parts. The first is related to the theory and different small-signal modeling approaches of GaN HEMT. The second is related to our work and contributions to the field of small-signal modeling. In this chapter, we will be showing the major parasitics found in the small-signal model of GaN HEMTs. Different structures for the extrinsic part of GaN HEMT will be studied since they differ in terms of extraction techniques and the amount of parasitics they consider. RF performance

metrics such as the transit frequency will be derived. Types of extraction approaches will be provided. The proposed EC-SSM and extraction technique will be presented in-depth detailing the steps taken to extract the extrinsic parameters of GaN HEMT and the advantages behind the proposed extraction technique. The extraction technique is then applied to *S*-parameters measurements obtained from the technical literature, specifically 2x100 um GaN/D [27], 4x50 um GaN/SiC [34], 2x200 um GaN/Si [35] as well as Graphene-based FET [36]. The extracted data will be discussed and validated for these devices.

In Chapter 4, we will be modeling the non-linear drain-to-source current with its dispersive effects caused by charge-trapping and self-heating phenomena. First, we will be looking at different topologies used for large-signal modeling, two of which representing the intrinsic capacitances as charge components, while the third topology will represent the intrinsic capacitances as current components. Then, we will be considering the techniques used to build the isothermal trapping-free current [18][37-38]; this latter can be developed using empirical methods such as extracting the isothermal trapping-free current from pulsed IV measurements, or by using quasi-physical models such as the Surface Potential model [37] or Quasi-Physical Zone Division model [38]. We will be retaining the Quasi-Physical Zone Division model in our research work due to its simplicity, high accuracy, and lower number of fitting parameters compared to the Surface Potential model. The position of the Fermi level and the density of the 2-DEG will be numerically solved and fitted into a simplified expression, then the isothermal trapping-free current will be derived taking into consideration mobility degradation and velocity saturation. Finally, pulsed-IV measurements will be used for both GaN/D and GaN/SiC to develop the overall model that takes into account charge-trapping and self-heating effects, we will be comparing the fitting parameters extracted from the pulsed IV measurements between GaN/D and GaN/SiC and compare our insights with the observations from the literature.

Chapter 5 will be related to model validation by implementing the overall model in the Keysight Technologies Advanced Design System commercial software [30]. We will be showing how to implement the model using a Symbolically Defined Device and how

to read the intrinsic components with the help of Data Access Components and Variables. We will first simulate the *S*-parameters under small signal input and large-signal DC bias to verify their accuracy with measurements. Next, we will be comparing the static DC IV characteristics between simulations and measurements for both GaN/D and GaN/SiC. Load-pull and single-tone simulations for class AB operation will be provided and compared with measurements.

Chapter 6 will summarise the work while giving research directions to future work.

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Chapter 2: Technical Background

In this chapter, we will be discussing the basics of AlGaN/GaN HEMT. This discussion includes the reasons behind choosing the AlGaN/GaN HEMT, its basic structure, and its principle of operation related to the formation of 2-Dimensional Electron Gas (2DEG) and polarization effects. We will be also looking into the non-idealities of the AlGaN/GaN HEMT, mainly in terms of current dispersion effects, parasitics, and substrate choice. The measurements required to model these non-idealities will be discussed as well. Measurements uncertainty is also an issue that should be addressed while taking these measurements. Finally, we will be considering modeling approaches, detailing their advantages and disadvantages.

2.1 Why GaN HEMT?

During the last decade, there has been a demand for high-frequency high-power semiconductor devices for microwave and radio frequency applications such as wireless communications, satellite communications, and radars [1]. In the past, the Gallium Arsenide (GaAs) Metal-Semiconductor Field-Effect Transistor (MESFET) was able to achieve such demanding requirements by having a short channel length and increasing the channel doping under the gate, which led to a high saturation current and high output power [2]. However, reducing the channel length and increasing the doping concentration of the channel raised many issues such as velocity saturation and mobility degradation, which makes it impossible for such devices to achieve the demanding requirements for upcoming years [2]. The mobility degradation and velocity saturation are caused by the existence of a large number of dopant atoms and charge carriers in the same region (the channel), where they start to experience multiple collisions with each other causing a reduction in the average mobility of the carriers. This phenomenon is known as the impurity scattering effect [2].

In order to mitigate this issue, the free charge carriers must be separated from the dopant atoms; this can be achieved by using two different semiconductor materials with different bandgap energies that enable such separation, like AlGaN and GaN. This type of transistor is known as the High Electron Mobility Transistor (HEMT). The idea is to

cause a discontinuity at the metallurgical junction, which will create a 2DEG that has only free charge carriers with no dopant atoms in the channel and, hence, the mobility of charge carriers will increase greatly and the impurity scattering effects will be mitigated [2].

The reasons for choosing AlGaN/GaN heterojunction as HEMT are mainly due to [2]:

- The large bandgap energy of the GaN that causes the breakdown voltage to be extremely high (which allows a large voltage swing across it).
- The high saturation velocity, due to the separation of the dopant atoms from the free charge carriers, which mitigates the effect of the impurity scattering effects (causing a large saturation current and large transconductance).
- The existence of both high voltage swings and high saturation currents, which allows HEMT devices to exhibit large output powers and high PAE (making such devices highly useful for high-frequency high-power applications).

Figure 2.1 shows operating powers and frequencies for different technologies used in developing RF power-amplifiers for various applications, underlining the fact that the largest overlap is indeed covered by the GaN HEMT [3].

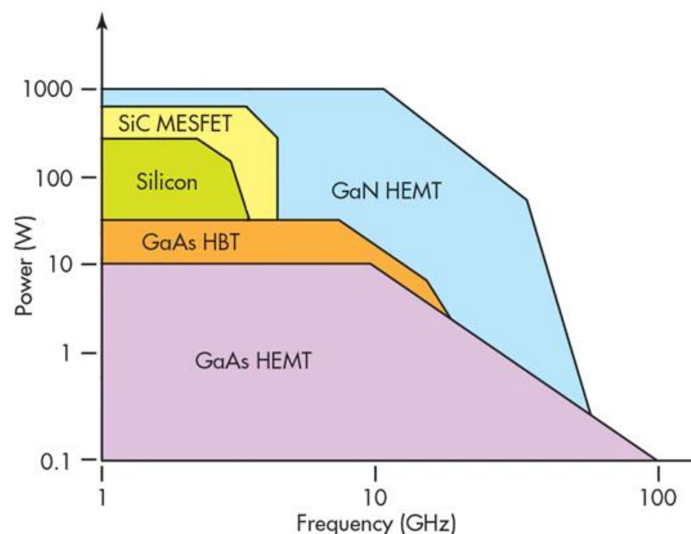

Figure 2.1 Operating power and frequencies for different technologies [3].

2.2 Fundamentals of GaN HEMT

It is important to understand the basic physics behind AlGaN/GaN HEMT operation and the principles behind the formation of the channel that is responsible for current conduction. It will be shown that AlGaN/GaN is a heterojunction that forms an electron gas known as 2DEG. This 2DEG is formed either by free electrons donated by dopant atoms from AlGaN or by polarization effects. The basic structure of AlGaN/GaN HEMT will also be discussed. This fundamental theory is necessary to understand the non-idealities that arise from such a complex structure.

2.2.1 Heterojunctions

There are two different types of semiconductor junctions. The first is known as the homojunction type where the two materials used to build this junction are of the same material and hence they have equivalent bandgap energy. An example of a homojunction is the typical pn junction used to build rectifier Diodes. The second type is the heterojunction type, where two different materials with different bandgap energies (such as AlGaAs/GaAs or AlGaN/GaN) are used to build the junction [2]. Since the materials used to build the heterojunction have different bandgap energies, it will result in a discontinuity at the junction interface, causing the energy bands to bend depending on the type and the density of dopant atoms in each material as well as the overlap amount between the bandgap energies of both materials. The different combinations of types and levels of doping of the materials, in addition to their bandgap energy alignment, will create several types of heterojunctions with different characteristics [2].

There are three possible alignments for heterojunctions, as shown in Figure 2.2a. The first one is called straddling where the bandgap energy of the wide-gap material completely overlaps the bandgap of the narrow-gap material. Another type is the staggered alignment where each bandgap covers a portion of the other material's bandgap energy (Figure 2.2b). The case where there is no intersection between the two bandgap energies is called the broken gap alignment [2]. The broken gap is shown in Figure 2.2c.

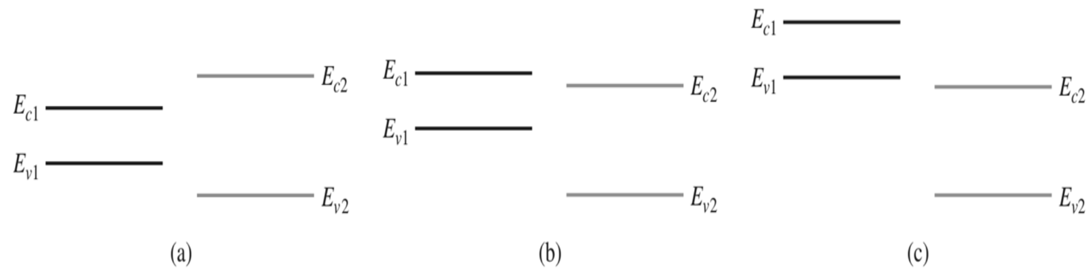

Figure 2.2 Types of heterojunctions based on alignments: (a) Straddling, (b) Staggered and (c) Broken Gap [2].

From the type of dopants point of view, when both materials are doped using different types of carriers such as nP or pN heterojunctions (the lower case letter is used for the narrow bandgap material and the upper case letter is used for the wide bandgap material), they are known as anisotype heterojunctions [2]. Isotype heterojunctions occur when both materials are doped using the same type of carriers such as nN or pP. This discussion about the heterojunctions and their different types is crucial for realizing 2DEG as will be seen in subsection 2.2.2.

2.2.2 AlGaN/GaN as a heterojunction and the formation of 2DEG

2DEG is a terminology that is used when electrons have quantized energy levels that confine the movement of electrons in two dimensions only [2], i.e., in order to form 2DEG, the energy bands should bend in a way that confines the movement of electrons in two dimensions only. 2DEG is formed by having isotype junction with bandgap energies that have a straddling configuration as was shown in Figure 2.2a. Figure 2.3a shows the energy band diagram of AlGaN/GaN heterojunction before equilibrium condition, where the wide bandgap material is an n-type doped AlGaN, and the GaN is an intrinsic narrow bandgap material. In order to achieve equilibrium, the Fermi levels of both materials should be equal at equilibrium conditions. For that to happen, the bands should bend in appropriate manners to achieve such conditions. Since the electrons density of the AlGaN is higher than that of the GaN, the electrons will diffuse from AlGaN to GaN causing the conduction band of the AlGaN close to the interface to bend upwards away from the Fermi energy level. This will, in turn, increase the number of electrons at the GaN side,

which will cause the conduction band at the edge of the interface of the GaN to bend downward closer to the Fermi energy level. The resultant energy band diagram should be similar to that of Figure 2.3b.

The major advantage behind such 2DEG formation is that the free electrons in the GaN formed inside the potential well are separated from the donor atoms in the AlGaN, which will mitigate the effects of impurity scattering effects thus, reducing mobility degradation and velocity saturation [2]. Subsequently, the high electron mobility results in large current density and large transconductance of the device.

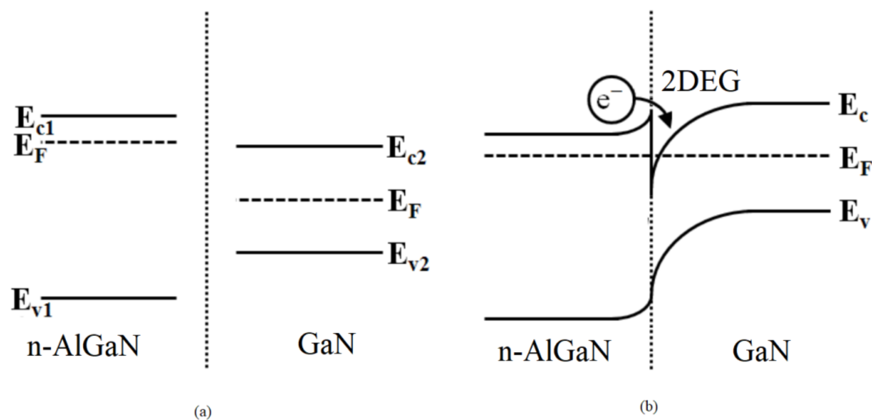

Figure 2.3 AlGaN/GaN heterostructure energy band diagram (a) before equilibrium and (b) at equilibrium [4].

2.2.3 Polarization effects and AlGaN/GaN as a HEMT

In AlGaN/GaN HEMT, the formation of the 2DEG is not entirely due to the doping density of the AlGaN wide bandgap material. It was found that a 2DEG can still be formed regardless of whether we doped or intentionally undoped the AlGaN layer [4]. The formation of 2DEG in the case of the undoped AlGaN layer is due to the existence of an inherent electric field that has two components: one is due to spontaneous polarization P_{SP} and the other is due to piezoelectric polarization P_{PE}. The polar nature of GaN and AlGaN crystals generates a negative sheet charge at one face of the crystal and a positive sheet charge on the other face. The generation of the sheet charge is mainly due to the

high electro-negativity of the nitrogen [4]. These charges will produce a built-in polarization field known as spontaneous polarization as shown in Figure 2.4a.

AlGaN and GaN crystals have different lattice constants, which results in tensile stress on the AlGaN layer near the interface of the heterojunction. The stress does not have any significant effect on the channel because, typically, the thickness of the GaN layer is made larger than the AlGaN. This tensile stress induces static charge and a built-in polarization field due to the properties of Nitride. The direction of the piezoelectric polarization has the same direction as the spontaneous polarization, as shown in Figure 2.6b. Both types of polarization will result in a net positive charge at the AlGaN/GaN interface and a net negative charge at the top of the AlGaN layer, forming a polarization dipole, as shown in Figure 2.6c. These net charges are similar to the polarization of dielectrics, meaning they are not free charge carriers [4]. Due to the polarization dipole and the electric field E_{NET} induced in the AlGaN layer, the 2DEG will be formed in order to compensate for the net positive charge at the interface of the AlGaN/GaN. The formation of such 2DEG is possible even without doping the AlGaN layer [4]. However, since the 2DEG is not supplied from the AlGaN, it must have a different source of electrons. The source is the surface donor states near the top of the AlGaN layer. To achieve equilibrium conditions and generate the final charge distribution, the polarization dipole should be complemented by an opposite dipole; this dipole causes the formation of the 2DEG at the heterojunction interface and the positive charge density at the top side of the AlGaN layer [5]. This phenomenon is presented in Figure 2.4d.

AlGaN/GaN HEMT resides on a semi-insulating substrate that should have a good lattice matching with the narrower bandgap material in order to reduce charge-trapping effects, otherwise, it induces leakage currents through the substrate and reduces energy efficiency [5]. The drain and the source are made out of ohmic contacts to allow current to flow from the drain to source or vice versa. The gate is formed from a Schottky contact with the AlGaN wide bandgap material [5]. A basic structure of AlGaN/GaN HEMT is shown in Figure 2.5. The control of the channel conductance is similar to the operation of a Modulation-Doped Field-Effect Transistor (MODFET): when a negative voltage is applied at the gate, an electric field will be induced depleting the channel. If the voltage

applied at the gate exceeds the pinch-off voltage, the conductivity of the channel will increase. Figure 2.6 illustrates how the 2DEG is depleted when the voltage applied at the gate is well below the pinch-off point.

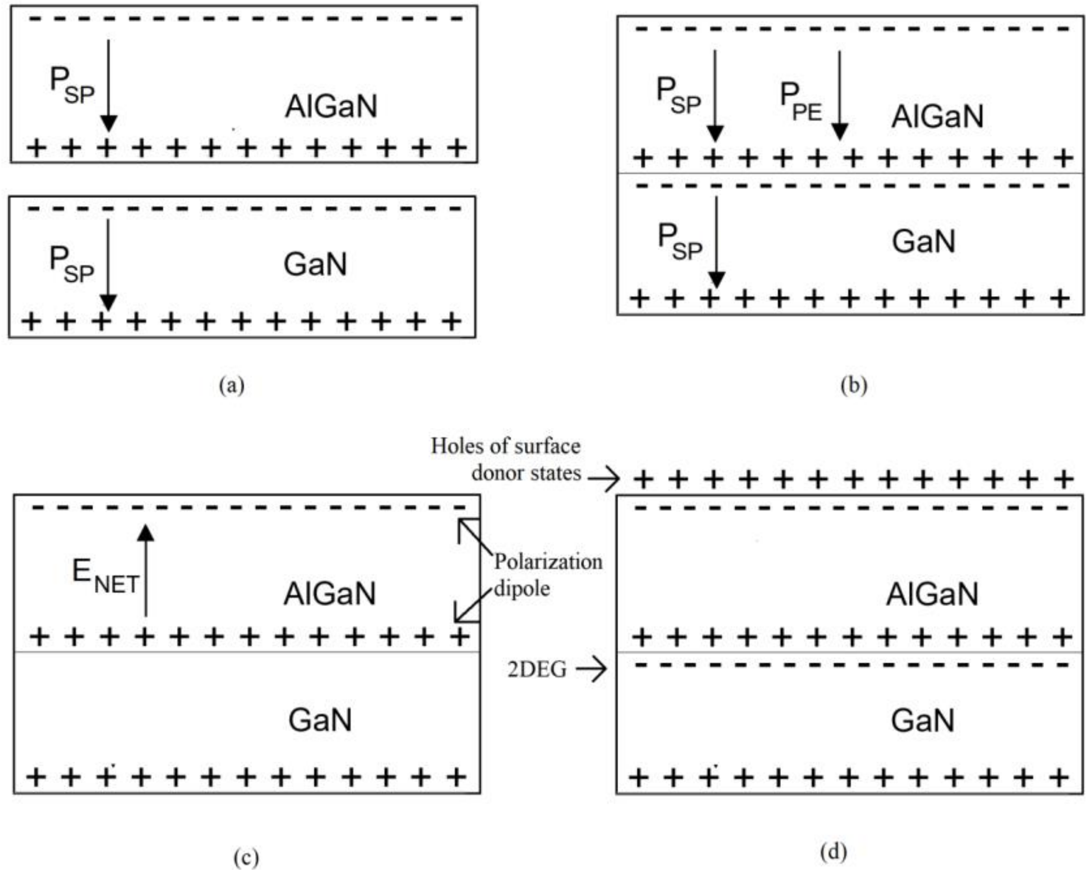

Figure 2.4 Illustration of polarization effects on forming 2DEG in AlGaN/GaN heterojunction: (a) Spontaneous polarization before the heterojunction, (b) The junction creates tensile stress and piezoelectric polarization, (c) interface sheet charges interact to form the polarization dipole and E_{NET} and (d) The dipole and E_{NET} form the 2DEG with electrons of surface donor states [4].

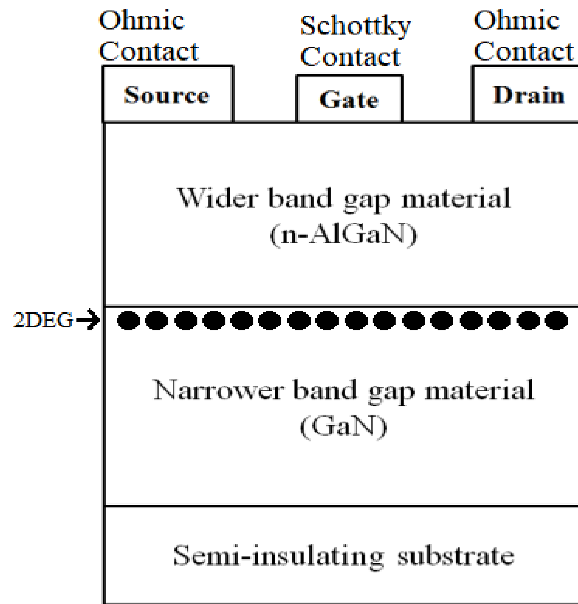

Figure 2.5 Basic structure of AlGaN/GaN HEMT [5].

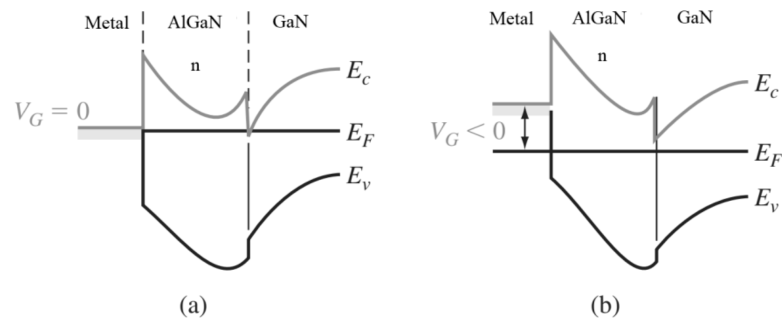

Figure 2.6 Energy band diagram of AlGaN/GaN HEMT with (a) $V_G = 0$ and (b) $V_G < 0$ [2].

2.3 Non-ideal effects of AlGaN/GaN HEMT

GaN HEMT exhibits a great deal of non-idealities due to the high mobility of its electrons, and the structure of the device. These non-idealities can cause effects that reduce the performance of the device. The high electron mobility causes a large current density that produces heat, which decreases the drain current, and, in severe cases, the current may collapse. Other effects are related to charge-traps due to imperfections in the

structure of the GaN HEMT. There are parasitics associated with the device structure that can lower the performance of the GaN HEMT. The choice of the substrate greatly influences the PAE of the GaN HEMT.

2.3.1 Current Dispersion due to self-heating and charge-trapping effects

Current Dispersion is the reduction in the value of drain-to-source current under static-DC and RF operation [6]. This reduction is dependent on the frequency of the RF signal and the bias conditions [6]. The current dispersion can be identified easily by eyeballing the differences between static DC I-V measurements and pulsed I-V measurements, as shown in Figure 2.7. These differences can depend on the pulse repletion, the duty cycle, and the quiescent bias conditions at which the pulsed I-V measurements were performed [7]. Current dispersion due to operating frequency for MESFET was explained by the finite times the electrons required to form or deplete the channel, which lags the current response due to the rapid varying (high-frequency pulsed I-V) to non-variant (Static DC) or slowly-varying inputs [7]. AlGaN/GaN (called GaN for simplicity) HEMTs have their currents highly dispersed and this dispersion is not due to operating frequency only, but also attributed to other effects such as self-heating and charge-trapping effects.

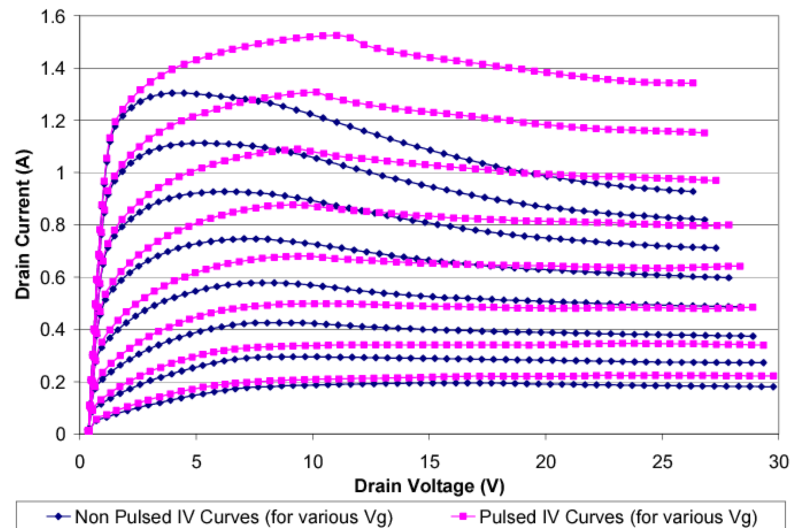

Figure 2.7 Static DC (non-pulsed) and Pulsed I-V measurements for arbitrary GaN HEMT [8].

Since GaN HEMT devices are able to achieve very large power densities, there will be a high-temperature rise within their active regions. This high temperature can deteriorate the performance of the GaN HEMT during normal and overload operating conditions, thus causing current dispersion [4]. This thermal increase can also lead to current collapse due to the reduction of electron's saturation velocity. The source of this heat can be due to current flow in the active regions of the device, the ambient temperature, and/or the substrate thermal conductivity. The heat needs to be transferred to other layers in order for it to dissipate; this dissipation depends on the thermal conductivity of the GaN layer (called GaN Buffer), the nucleation layer (detailed later in subsection 2.3.3) and the substrate. The finite thermal conductivity of materials results in delays in transferring/dissipating the heat, which in result, will confine the thermal heating in the active regions of the device, causing a reduction in the output current and the rated power [4]. Self-heating effects lead to a correlation between the present state and the output signals of the device, which causes the power amplifier to be dependent on previous states or input signals. This is known as thermal memory [9]. Self-heating effects can be accurately modeled by employing an electro-thermal model using the Equivalent Circuit-Large-signal Model (EC-LSM), which will be discussed in chapter 4.

Other important factors in current dispersion are the charge-trapping effects; charge-trapping is the case of capture of an electron from and to the conduction band [9]. The place at which an electron is captured is called a "center" or "trap". If a trap captures an electron from the conduction band and later emits it to the valence band, then this capturing nature is known as a recombination center or trap. Traps can exist at the surface of the GaN HEMT, in the interfaces between layers or in the bulk of the semiconductor layer [9]. The first type of charge-trapping effect is the surface-trapping effect, which is related to electrons moving from the metal gate to the available positively charged states in the surface layer of the GaN HEMT [9]. The positively charged surface states are due to the polarization effect discussed in subsection 2.2.3. Passivation layer added to the surface of the GaN HEMT around the gate metal can prevent the surface states from being neutralized by electrons, maintaining positive charge [10]. Figure 2.8 shows the inclusion of a passivation layer to reduce electron traps. If the passivation process is not perfect, which is usually the case, the electrons will be able to leak from the metal gate to

the surface states and be trapped. Such behaviour usually occurs under the influence of a large electric field, which is the case under high power operation [11]. This reduction in the surface charge will affect the equilibrium and the opposite dipole will cause a reduction to the 2DEG density in order to reach equilibrium, leading to surface traps induced current dispersion.

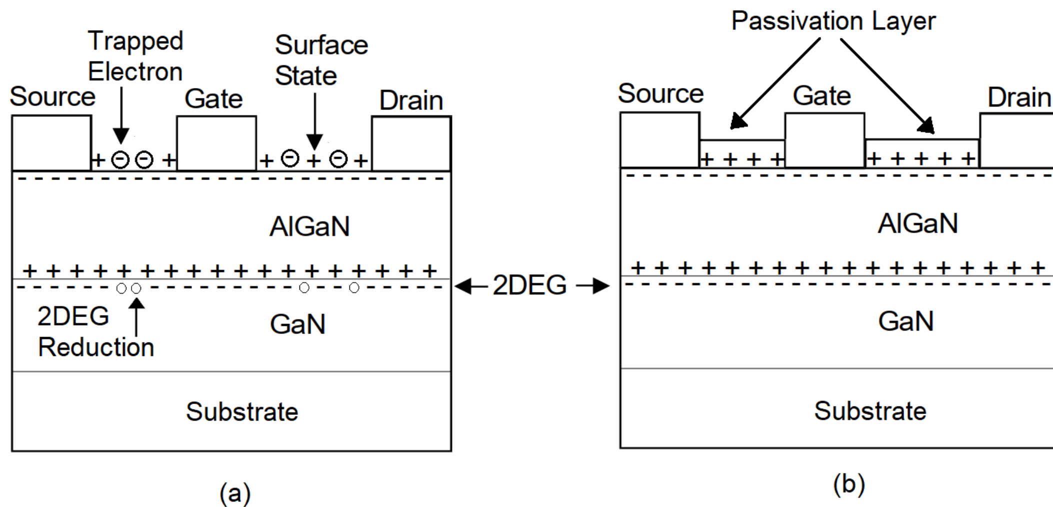

Figure 2.8 Illustration of passivation layer inclusion in GaN HEMT: (a) trapped electrons on surface and reduction in 2DEG density and (b) passivation layer preventing electron traps.

The other type of charge-trapping effect is the buffer-trapping effect related to traps that exist at deep levels inside the GaN buffer or at the interface between the GaN buffer and the substrate [10]. Under conditions of high drain-source voltage and high electric fields, electrons that are moving inside the 2DEG channel could be trapped inside the buffer traps. The long trapping time constant, in the order of 0.1 ms, prohibits the electrons from following the high-frequency signal, making such electrons unavailable for current conduction [12]. The trapped electrons produce a negative charge, which reduces the 2DEG density and reduces the channel current. This is called buffer-trapping induced current dispersion. The reason behind such traps is a large number of dislocations in the GaN buffer due to the large lattice mismatch between the GaN buffer and the substrate [13]. Such dislocations will cause electrons to be trapped. A common solution to reduce dislocations is to add a nucleation layer between the GaN buffer and

the substrate. Another source of buffer-traps is the existence of background electrons due to a small number of native donors. These donors can be compensated by adding acceptor atoms. If the number of acceptor atoms was not enough to compensate the already existent donor atoms, leakage current during pinch-off voltage can be induced through the buffer and the substrate. However, overcompensation of the acceptor atoms will cause more electron traps, and hence the number of acceptor atoms should be optimized to have the minimum traps possible [10].

2.3.2 Parasitic effects in GaN HEMT

Parasitic effects in GaN HEMT are related to capacitive, inductive, and conductive effects that are mainly due to device structure, electric field linkage, pad connections, charge-trapping effects, and gate electrodes. In order to increase the output power of GaN HEMT, we may require to enlarge the total horizontal area of the gate electrodes [4]. This can be done by increasing the electrode width or adding more gate electrodes and connecting them in parallel as if we are adding more transistors in parallel. However, with an increased number of gate electrodes, the capacitive coupling and thermal crosstalk effects are of great concern. Capacitive effects are well-known parasitics related to the separation between metal surfaces and the charge density on these surfaces. The parasitic elements can be distinguished into two parts namely, the intrinsic part related to the physical structure of the device and the extrinsic part due to contact pads and metallization effects.

The intrinsic elements are composed mainly of parasitic capacitances and parasitic conductive phenomena. Figure 2.9 shows a structure of a GaN HEMT showing the most common capacitive components that can be found inside the intrinsic part of the device. The N+ GaN is used to provide improved contact with the drain and source electrodes [14]. C_{gsf} and C_{gdf} are extremely small, and they are the capacitances associated with the inter-electrode electric field linkage between both electrodes. C_{gs1} is due to the depletion region under the gate, which couples the gate to the low resistivity 2DEG region underneath the gap between the gate and the source [14]. C_{gs2} is the fringing capacitance between the gate and the GaN Cap layer under the source electrode. These three capacitances can be lumped into a single small-signal capacitance C_{gs} (will be shown

later in the EC-SSM). C_{gd} has a similar composition to C_{gs} and can also be lumped into a single small-signal capacitance.

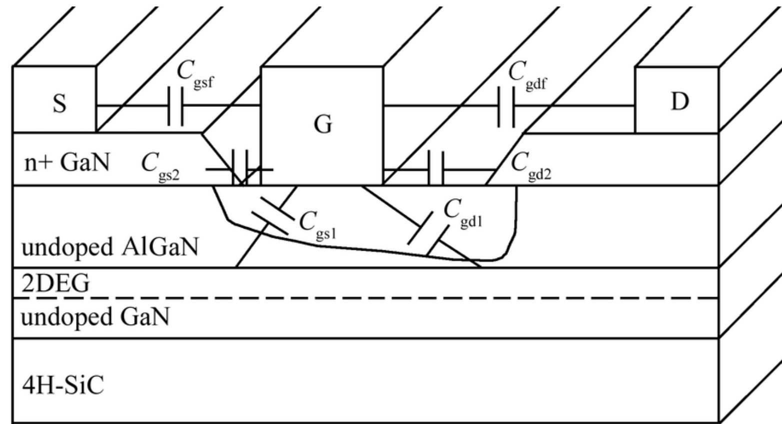

Figure 2.9 Intrinsic capacitances of GaN HEMT [14].

Figure 2.10 shows typical C_{gs} and C_{gd} plots for multi-bias points (different V_{gs} and different V_{ds}) [14]. It can be noted from C_{gs} plot that C_{gs} increases with V_{gs}. When the GaN HEMT is below the pinch-off voltage, C_{gs} is dependent only on the width of the depletion region and hence has the minimal value of its distribution and is independent (remain constant) of V_{ds} variations due to the depletion of the 2DEG region. When V_{gs} reaches the pinch-off point, there will be a sudden increase in C_{gs} value due to the formation of 2DEG and the decrease in the depletion width. Any increase in the value of V_{gs} would only increase C_{gs} by a small amount, indicating an insensitive source edge-to-gate to the depletion region [14]. C_{gd} plot shows that C_{gd} increases with increasing V_{gs}, but decreases with increasing V_{ds}. The electric field has a peak value at the drain end and decreases along the gate-to-drain length, which leads to a drop in charge. As V_{ds} increases, the peak electric field point will be shifted along with the space between the drain and the source, which causes a reduction in the channel charge, and hence C_{gd} decreases [14].

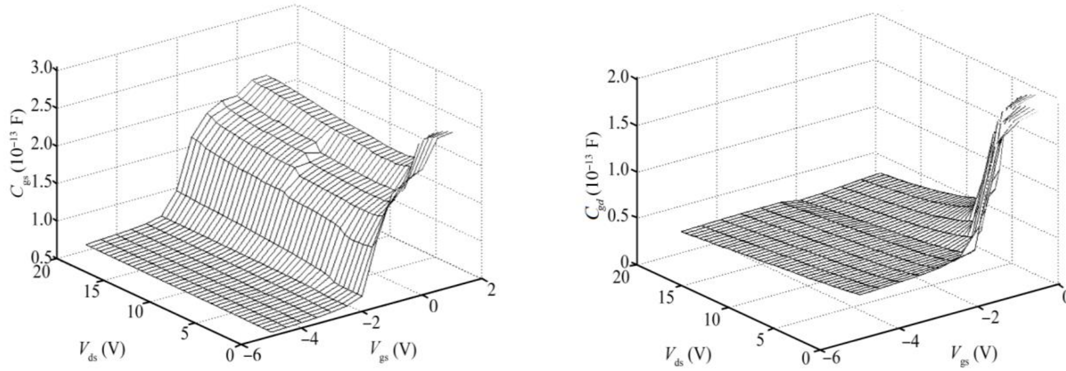

Figure 2.10 Typical C_{gs} and C_{gd} plots under different bias conditions for GaN HEMT [14].

A common assumption usually made is that $C_{gs} = C_{gd}$ below pinch-off point to reflect the symmetry between the drain and the source with respect to their distances to the gate electrode [4]. The location of the gate in a centered location between the drain and the source is a common practice in small FETs. Any variation in the ratio of C_{gs}/C_{gd} from 1 can be attributed to two main reasons (i) having different distances between the source-to-gate and the drain-to-gate electrodes and (ii) charge-trapping effects and passivation layers [15]. For example, an increased distance between the gate and the drain will increase the breakdown voltage of the GaN HEMT, hence increasing its output power even further [16]. Another scenario resembles two versions of the 0.2 mm AlGaN/GaN HEMT that were studied in [15], one having SiN passivation layer and the other without it. The paper mentioned that C_{gs} increased in large magnitude below pinch point for the device with SiN layer compared to the device that was not passivated. These effects make the ratio $C_{gs}/C_{gd} > 1$ and should be taken into account during small-signal modeling.

For the extraction technique we implemented (as will be seen later in chapter 3), we took into account that C_{gs}/C_{gd} might be greater than one. It will be shown later that GaN/D and GaN/SiC studied in this work will have a C_{gs}/C_{gd} ranging from 3 to 5 due to the asymmetrical structure of the GaN/D and GaN/SiC, where the distances between the gate and both the drain and the source were 2 um and 1 um, respectively [17][18]. The remaining intrinsic parasitic elements are the gate forward conduction, gate breakdown conduction, and drain-to-source channel length modulation.

The gate forward and breakdown conductions are related to gate-to-source and gate-to-drain active regions where diode-like behavior occurs, causing leakage current depending on the bias conditions of the device. The drain-to-source channel length modulation is due to the shift in the location of the peak electric field from the drain edge toward the source. This will cause an electric field in the depletion region, which accelerates electrons at the pinched point of the channel thus, increasing current. The drain-to-source conductance should decrease with increasing V_{ds}.

The extrinsic structure of the GaN HEMT is related mainly to inter-electrode and crossover capacitances between the gate, source, and drain [10]. It can also include the capacitive effects of pad connections, measurement equipment, probes, and probe tip-to-device contact transitions [10]. In addition, there are some inductive effects related to metal contact pads and access transmission lines. There are also some resistive effects at the drain and source ohmic contacts and the gate metallization electrode [19]. Since the probes and metallic connections are made at the gate and the drain of the GaN HEMT, the extrinsic elements should be symmetrical in values if the connections and the probes are perfectly made; any deviation in the symmetry of these values can be related to imperfections in the probes and connections as well as in the structural symmetry. The extrinsic section may include parasitic conduction through the substrate depending on the leakage current through the substrate caused by buffer-trapping effects and lattice mismatch between the substrate/nucleation layer/GaN buffer [20]. This conduction will be exhibited for both GaN/D and GaN/Si.

2.3.3 Substrate choice

As mentioned earlier, GaN devices exhibit a large output power and PAE, which leads to an increase in their operating temperature. This temperature increase leads to self-heating induced current dispersion that can deteriorate the PAE during normal and overloaded functioning conditions. Two major reasons of such effect are due to the nucleation layer used in-between the GaN buffer and the substrate (to reduce lattice mismatch between them) and the thermal resistance associated with the substrate (this latter must be as low as possible to efficiently dissipate the heat through the substrate) [21]. There should be tradeoffs to have both reduced temperature resistance and

acceptable lattice-matching between the substrate and the GaN buffer [22]. Therefore, in order to reach the full potential and capabilities of the GaN HEMT, we should retain a substrate that has both low thermal resistance to reduce self-heating effects and high electrical resistance to reduce leakage current. Furthermore, it should adhere to the GaN buffer by using a suitable material that provides a very little lattice mismatch with the substrate in order to reduce buffer-trapping effects. A full structure of GaN HEMT that includes all the layers added starting from section 2 is shown in Figure 2.11.

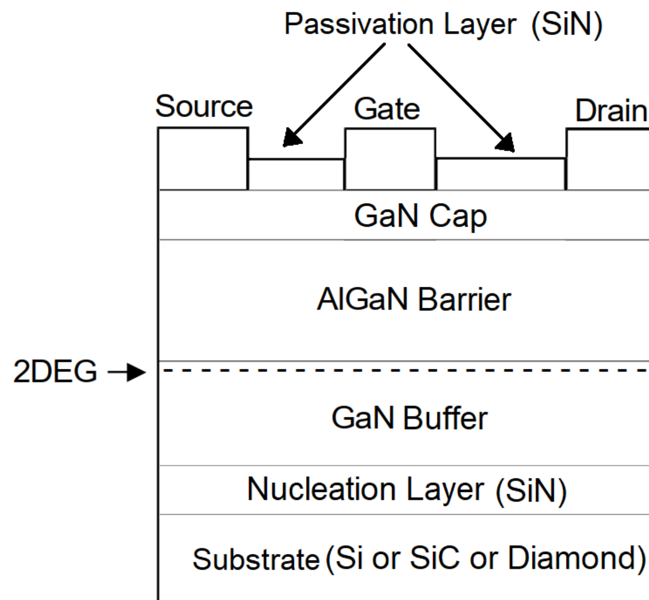

Figure 2.11 GaN HEMT full structure with all defined layers.

To address this issue, several substrate materials have been utilized for GaN HEMTs, from which Silicon Carbide (SiC) and Silicon (Si) substrates are the most commonly used [1]. The GaN/SiC is the state-of-the-art GaN HEMT. SiC substrate exhibits 390-450 W/m-K thermal conductivity and 10^4-10^6 Ω-cm electrical resistivity [21]. On the other side, the Si substrate of GaN/Si has a thermal conductivity in the range of 135-150 W/m-K and electrical resistivity of about 2.3×10^5 Ω-cm [21]. It can be noted that, compared to Si substrate, the SiC substrate presents a thermal conductivity three times higher as well as a larger substrate resistance at low frequencies [20][21]. These features show the primary reasons behind the choice of GaN/SiC as a state-of-the-art device. In 2006,

GaN/D was demonstrated in [23]. Diamond has a thermal conductivity of 1000-2000 W/m-K, i.e., two- to four times higher than that of SiC. Therefore, the GaN/D can have a 40% reduction in channel temperature, leading to a spacing between the gate fingers three-times smaller compared to GaN/SiC, without worrying about thermal crosstalk. This implies, in theory, an expected output power three-times larger than that of GaN/SiC while maintaining thermal reliability [21]. Furthermore, the diamond substrate has an electrical resistivity of about 10^{16} Ω-cm, which is 10 orders of magnitude larger than that of SiC substrate. The high substrate resistivity, with the potential of having a good adhesive layer between the GaN buffer and the diamond substrate, could lead to a tremendous improvement in leakage current with an increased PAE. It is clear that GaN/D holds valuable promises to the future of high-frequency high-power amplifier design due to its increased reliability and thermal management properties.

From an economical prespective, GaN/D exhibits superior thermal performance in terms of thermal resilience, which leads to lower cooling costs compared to both GaN/SiC and GaN/Si [21]. Even without cooling, GaN/D has lower mean time-to-fail and longer lifetime compared to both GaN/Si and GaN/SiC under normal and overloaded working conditions, which will lead to substantial energy savings for as long as 30 years [21]. In addition to that, the separation between the gate fingers of GaN/D can be brought closer to each other without worrying about thermal crosstalk as apposed to GaN/SiC and GaN/Si. This allows for increased fabrication density per wafer for GaN/D compared to GaN/SiC and GaN/Si, thus reducing fabrication costs [21].

On the other hand, GaN/D is, in fact, a relatively immature technology that requires a unique fabrication process compared to other GaN HEMTs. GaN/D is fabricated by first mounting a pre-fabricated GaN/SiC on a temporary carrier wafer (usually SiC) from the GaN-cap side before depositing the active regions. Next, the native SiC substrate is etched via plasma etching. A silicon mononitride (SiN) nucleation layer is subsequently added on top of the GaN buffer. Diamond is then deposited on the surface of the nucleation layer via Chemical Vapor Deposition (CVD). Finally, the carrier wafer is etched via plasma etching, and the active regions are deposited on the surface of the GaN Cap layer [18]. This approach exposes the GaN buffer during the wafer transfer process

thus, possibly introducing dislocations and impurity atom contaminations. Also, the SiN passivation layer adds thermal resistivity to the device and slightly improves matching. The resultant device incurs increased self-heating and buffer-trapping effects as a consequence (thus triggering leakage currents) [21].The selected substrate will greatly influence the electrical characteristics of the GaN HEMT. However, the particular specificities of any retained substrate should be taken into account for efficient modeling of the device behavior. For the GaN/Si, the lower frequency impedance reduction of the Si substrate should be considered [20]. This impedance reduction is due to the moderate resistivity of the Silicon, which causes a p-i-n diode formation (p-silicon/GaN/Metal) inside the GaN HEMT [20]. For the GaN/SiC, the self-heating effect is the most dominant and should be modeled as well. Finally, for the GaN/D, the self-heating effects should be compared with the state-of-the-art GaN/SiC in order to determine the effects of self-heating on the current dispersion of the two devices.

All of the mentioned effects, parasitics, and substrates, should be efficiently modeled to predict the behavior of the GaN HEMT and to produce an accurate model that can be used for building up various circuits. As will be seen in chapters 3 and 4, there are numerous small-signal and large-signal models in the literature that differ in terms of complexity and their ability to model the complex effects of modern GaN HEMTs.

2.4 Typical characteristics and measurements

In order to model the GaN HEMT and its non-idealities, we need to characterize the device using different types of measurements. The necessary measurements are *S*-parameters measurements, Static DC I-V measurements, and Pulsed I-V measurements. It is also important to take care of measurement uncertainties associated with the equipment as will be discussed in this section.

2.4.1 Two-port network parameters and their measurements

A two-port network has one input port and one output port, and a block that represents transfer and impedance functions used to characterize the two-port network. Numerous network parameters can describe a two-port network: impedance *Z*-, admittance *Y*-, hybrid *H*-, transmission *ABCD*- and scattering *S*-parameters. Of main

importance to the modeling of GaN HEMT are the *Z*-, *Y*-, and *S*-parameters. The *Z*-parameters are represented by a 2 x 2 matrix:

$$\begin{bmatrix} v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \end{bmatrix} \tag{2.1}$$

where:

$$Z_{11} = \frac{v_1}{i_1}\Big/_{i_2=0} \tag{2.2}$$

$$Z_{12} = \frac{v_1}{i_2}\Big/_{i_1=0} \tag{2.3}$$

$$Z_{21} = \frac{v_2}{i_1}\Big/_{i_2=0} \tag{2.4}$$

$$Z_{22} = \frac{v_2}{i_2}\Big/_{i_1=0} \tag{2.5}$$

where Z_{11} is the open-circuit input impedance, Z_{12} is the open-circuit transfer impedance from the input port to the output port, Z_{21} is the open-circuit transfer impedance from the output port to the input port, Z_{22} is the open-circuit output impedance [24]. The *Z*-parameters are mainly useful when trying to write an expression of series elements. The *Y*-parameters are represented by a 2 x 2 admittance matrix as follows:

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{2.6}$$

where:

$$Y_{11} = \frac{i_1}{v_1}\Big/_{v_2=0} \tag{2.7}$$

$$Y_{12} = \frac{i_1}{v_2}\Big/_{v_1=0} \tag{2.8}$$

$$Y_{21} = \frac{i_2}{v_1}\Big/_{v_2=0} \tag{2.9}$$

$$Y_{22} = \frac{v_2}{i_2}\Big/_{v_1=0} \tag{2.10}$$

where Y_{11} is the short-circuit input admittance, Y_{12} is the short-circuit transfer admittance from the output port to the input port, Y_{21} is the short-circuit transfer admittance from the input port to the output port, and Y_{22} is the short-circuit output admittance [25]. The *Y*-parameters are extremely valuable when writing equations for parallel components of a circuit.

S-parameters are represented based on an incident or reflected waves on the two-port network, *a* and *b*, respectively. Figure 2.12 shows a representation of a two-port network with the incident and reflected waves. The *S*-parameters can be represented by a 2 x 2 matrix as follows:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.11}$$

where:

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \tag{2.12}$$

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \tag{2.13}$$

$$S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \tag{2.14}$$

$$S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \tag{2.15}$$

where a_1 and a_2 are the incident waves at the input port and the output port, respectively, and b_1 and b_2 are the reflected waves. Z_0 is typically 50 Ω. S_{11} represents the input reflection coefficient, S_{12} is the reverse transmission coefficient, S_{21} is the forward transmission coefficient, and S_{22} is the output reflection coefficient [26].

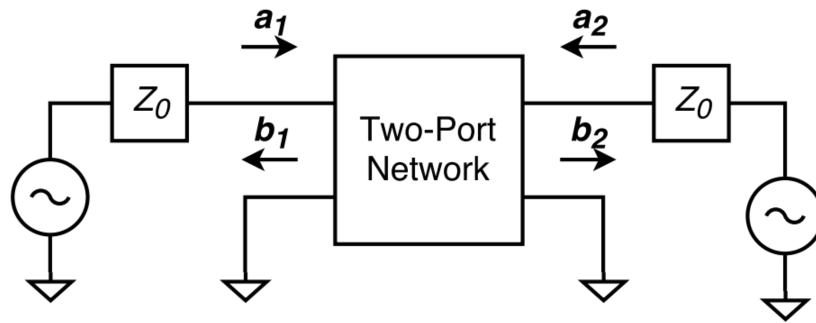

Figure 2.12 Two-port network for *S*-parameter measurement [27].

S-parameters are very useful for describing devices in the microwave range and they are defined as traveling waves. *Z*- and *Y*-parameters measurement techniques do not work appropriately in the high-frequency range due to the necessity of having short and open circuit tests that cannot be implemented due to parasitic effects [26]. If deemed necessary during the calculations, *S*-parameters can be converted to *Z*- or *Y*-parameters using well-known conversion equations (Appendix I).

In order to measure the S-parameters, we require a Vector Network Analyzer (VNA). Figure 2.13 shows a typical measurement setup for S-parameters measurements [28]. The measurement setup has a VNA, Device Under Test (DUT), bias tee, power supplies, RF cables, and Bias cables. VNA measurements are done with respect to the reference plane, meaning that the VNA does not only take into counts the waves at its terminals, but also the effects of extra components in the network (shown in Figure 2.14). This requires the VNA to be calibrated using either Short-Open-Load-Thru (SOLT) or Line-Reflect-Reflect-Match (LRRM) techniques [29]. The basic principle is to use dummy test structures with different layouts (e.g. open, short) to characterize the area around the DUT. The measurements obtained from different test structures can be used to remove the reference plane effects and hence obtain measurements that are more accurate.

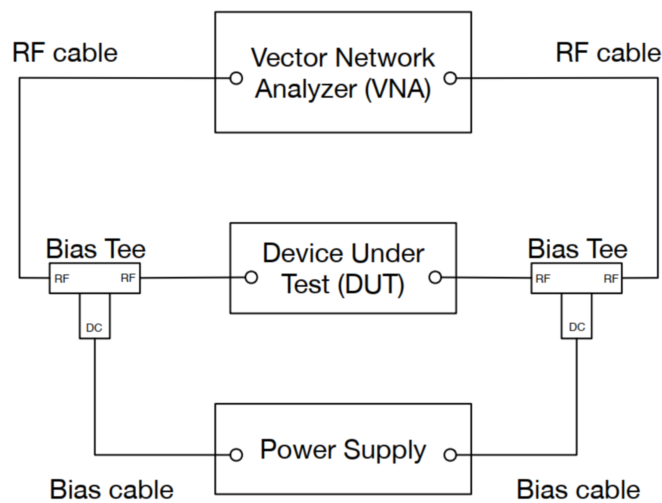

Figure 2.13 Typical setup for measuring S-parameters [28].

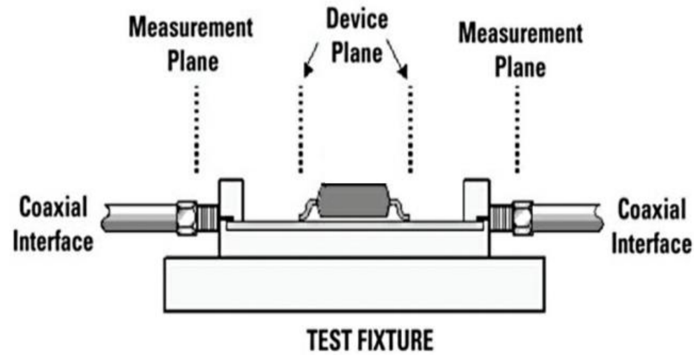

Figure 2.14 Difference between device plane reference and measurement plane reference on accuracy of *S*-parameters measurements [29].

2.4.2 Static DC I-V characteristics and measurements

The static DC I-V measurements include the output characteristics and the transfer function. They describe the DC drain current with respect to the drain-to-source voltage. This is done by sweeping the drain-to-source voltage for every gate-to-source voltage and measuring the current at each voltage step. Figure 2.15 shows typical static DC measurements highlighting important regions, voltages, and currents. V_{DS} at which the device is at the edge of the ohmic region and the saturation region is known as the knee voltage (V_k). I_{sat} is the maximum current value achievable by the device during the linear mode of operation. V_p is the pinch-off point (called threshold voltage) at which the device enters the conduction mode. V_{br} is the breakdown voltage [4].

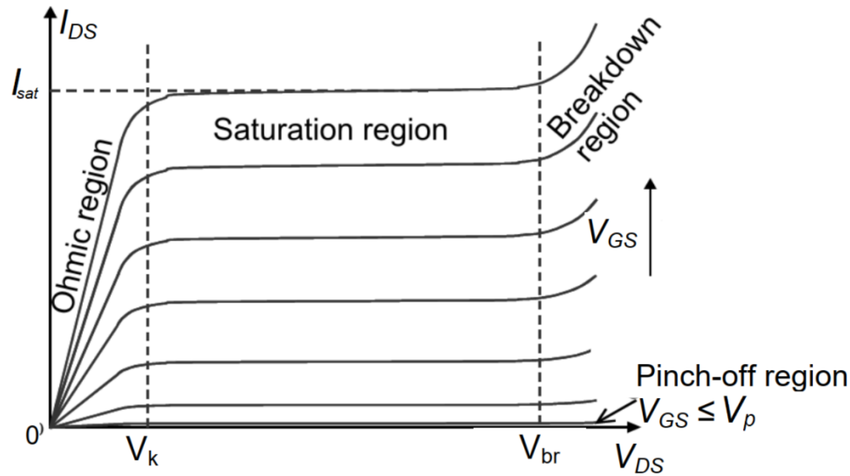

Figure 2.15 Static DC I-V characteristics [4].

The measurement setup is done by on-wafer probing station and DC voltage sources that have current ammeter embedded with them. The supply voltage provides only positive values, which requires modifying the connections such that it provides negative voltage to the gate electrode [4].

2.4.3 Pulsed DC I-V characteristics and measurements

Drain current measurements are taken using pulsed voltages as the bias instead of static DC bias. Pulsed I-V measurements are done to remove the thermal effects of the device [4]. To remove thermal effects, the pulse width of the voltage pulses should be significantly smaller than the time constants of the pulse width. If the duty cycle is low, the heat produced by the current on each pulse will not be added up at the next pulse. The pulse voltages known as quiescent bias points (V_{GSQ} and V_{DSQ}) should be superimposed on static-DC bias points characterized by V_{GS} and V_{DS}. By choosing a particular V_{GSQ} and V_{DSQ}, we can build a family of curves by producing pulsed-to-point measurements, where the points are the varied V_{GS} and V_{DS} [4]. Charge trapping effects are impacted by the quiescent bias point and the pulse amplitude. Under pulse operation and when the device is initially pinched off, the electrons are injected into traps under a high electric field. If the pulse is short, electrons will not be able to escape the traps due to the low response time to the short pulse [10]. However, if the quiescent bias point increases from the pinch-off point, electrons response time will increase and hence they will emit from the traps. Hence, by stepping-up the quiescent bias point above the pinch-off voltage, the

amount of trapped electrons, and the amount of current dispersion can be determined [10].

The measurement setup for pulsed DC IV measurements includes an on-wafer probing station and a dynamic I-V analyzer. The dynamic I-V analyzer sets the quiescent bias points and generates the DC voltage pulses with the desired duty cycle. It also measures automatically the dynamic drain current of the device.

2.4.4 Uncertainties in measurements

Measurement uncertainties are classified as random uncertainties and systematic uncertainties. Random uncertainties are statistical fluctuations that are random in nature. They are due to the precision limitations of the measurement device. Such uncertainties are not reproducible. These types of uncertainties can be minimized through averaging. Systematic uncertainties are the most important type of uncertainties and they are deterministic in nature and usually associated with the measuring equipment [30]. Systematic uncertainties can be minimized through the calibration of the measurement system as was discussed in subsection 2.4.1. Hence, the measurement accuracy is a function of the calibration of the measuring equipment. It is important to calibrate the measuring device to avoid inclusion of any parasitic effects that are not associated with the GaN HEMT and to avoid such parasitics to appear in the EC-SSM. It was found in [30] that due to the non-idealities or imperfections of the calibration technique, measurement errors increase as the frequency of measurement increases. Another concern of high-frequency measurement is the addition of parasitic elements at a high frequency that are not included in the EC-SSM. As will be seen in chapter 3, the *S*-parameters measurements were taken up to a frequency of 40 GHz and measurement uncertainties started to take effect at around 20 GHz, causing a small reduction in accuracy of measurement recording. However, it was stated in [30] that the accuracy of *S*-parameters is not greatly affected for small devices (i.e. < 400 um) in the high-frequency range and hence measurement up to 40 GHz are accurate enough to describe the parasitic of the device. It is important to know the frequency limit of the measuring equipment at which it can provide the last accurate reading.

2.5 Modeling approaches

Device modeling can be classified into three types: physical-based model, Behavioral-based model, and Equivalent Circuit-based model.

2.5.1 Physical-based model

In physical-based modeling, the device can be described using physical data such as carrier transport properties, material characteristics, and device geometry. The major advantage of this model is the ability to control the device fabrication process in order to enhance the described physics data. The response of the device is obtained by solving nonlinear differential equations to describe the internal field of the device and the electron transport theory. Numerical methods are needed to solve such complex equations, requiring a very long time and large storage memory to process such equations, which is not practical for the purposes of simple device modeling [31].

2.5.2 Behavioral-based model

The behavioral-based model treats the device as a black box that has inputs and outputs. The basic principle is to inject signals at the input and then due to a response from the black box, the output will be produced and measured. By testing the device under various conditions, we can obtain data from the output that can describe the "behavior" of the device. Two of the major advantages of this modeling approach are that (i) it is faster than the other modeling approaches and (ii) it is a convenient modeling approach when there is not enough information about the device. The drawback of behavioral modeling is it does not provide meaningful information about the device from the physical perspective. This, in turn, makes it difficult to implement a model that describes process variations in the device. It should also be noted that the accuracy of the model is limited to the range of measurements at which they were taken [31].

2.5.3 Equivalent Circuit-based model

The last modeling approach is known as Equivalent Circuit modeling. This modeling approach compromises between physical and behavioral models [32]. In order to form the equivalent circuits, we require both behavioral measurements and physical knowledge of the device. Behavioral measurements can be *S*-parameters measurements, static DC measurements, and pulsed DC measurements. Physical knowledge can be related to self-

heating, charge-trapping effects, parasitics, and substrate effects on GaN HEMT. The Equivalent Circuit modeling approach is divided into two major parts, one is the Equivalent Circuit-Small-signal Model (EC-SSM) which requires *S*-parameters measurements in order to describe parasitic and substrate effects. The second part is the Equivalent Circuit-Large-signal Model (EC-LSM) which uses static and pulsed I-V measurements to describe current dispersion due to self-heating and charge-trapping effects. The data from the EC-SSM are necessary to build the EC-LSM, and hence, the final model should describe all of the mentioned effects of the GaN HEMT. EC-SSM parameters are extracted using direct extraction and hence they are much faster than the physical modeling approaches. Optimization techniques can be added to enhance the extracted parameter values; however, optimization techniques may be computationally exhaustive. Nevertheless, Equivalent Circuit modeling approach is still faster than physical modeling. EC-SSM will be discussed in chapter 3 while EC-LSM will be discussed in chapter 4.

2.6 Conclusion

In this chapter, we showed the importance of GaN HEMT devices in 5G, satellite, and wireless communications. This is due to the high mobility and high breakdown characteristics of the AlGaN/GaN material. We presented the fundamentals of GaN HEMT's operation and physics, showing that the GaN HEMT is an isotype junction of bandgap energies that have the straddling configuration. This allows the formation of 2DEG in the quantum well, which separates the free electrons from the dopant atoms in the AlGaN. Even if the 2DEG is not formed conventionally via the AlGaN/GaN heterojunction (i.e. undoped AlGaN), 2DEG can still be formed through the polarization effect due to the polar nature of GaN and AlGaN crystals and the electro-negativity of nitrogen. Nonideal effects of GaN HEMT on current dispersion were also discussed. One of them is the self-heating effect that produces self-heating induced current dispersion. Another effect is the surface-trapping effect caused by positively-charged states or traps existing at the surface of the GaN HEMT near the gate. Another trapping effect is the buffer-trapping effect due to traps existent in the interfaces between the GaN buffer, the

nucleation layer, and the semi-insulating substrate. If electrons get trapped, they would cause charge-trapping induced current dispersion.

Parasitics within the GaN HEMT structure include intrinsic and extrinsic capacitances, gate forward conduction, gate breakdown conduction, extrinsic resistances, and inductances. Among them, parasitic conduction through the substrate is an important parasitic that exists due to buffer-traps and the finite resistivity of the substrate. The effects of asymmetrical GaN structure, the passivation layer, and buffer-traps on the symmetry of the intrinsic capacitances were exposed.

The substrate choice affects greatly the electrical characteristics of a GaN HEMT. Silicon substrate has a low-frequency reduction in the input and output impedance, which leads to parasitic conduction through the substrate. Silicon Carbide substrate is affected by the self-heating effect due to the moderate thermal conductivity of Silicon Carbide. GaN on Diamond substrates have high thermal conductivity but may be affected by buffer-traps due to the wafer transfer process.

Developing a model that can describe the mentioned non-ideal effects require measured data like *S*-parameters or/and static/pulsed IV measurements. Modeling approaches were briefly introduced, showing that the Equivalent-circuit modeling approach is a good compromise between the empirical and physical modeling approaches.

The theoretical background presented in this chapter builds the foundations needed to develop the device EC-SSM and EC-LSM. However, the development of EC-LSM necessitates the development of EC-SSM, which will be presented in the next chapter.

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Chapter 3: Small-Signal Modeling and Proposed Extraction Technique

In this chapter, we will be mainly concerned with the topologies of the small-signal model and their extraction techniques. We will start by describing the parameters of the intrinsic and the extrinsic parts of the structures of GaN HEMTs. RF performance metrics will be derived for the GaN HEMT. We will be showing the most common extraction techniques for the extrinsic part while introducing our proposed extraction technique, a convenient approach that takes into account different substrates and parasitic conduction for GaN HEMTs as well as the effects of asymmetrical structure, the passivation layer, and charge-trapping phenomena on charge distribution. A recent optimization technique will also be applied to tune the extracted parameter values. It will also show the high rate of convergence of the optimizer and its capabilities of avoiding local minima points. After that, a typical intrinsic extraction technique will be applied to extract the intrinsic parameters of GaN HEMTs. The proposed extraction technique will be applied to four devices' *S*-parameters measurements obtained from technical literature: GaN/D, GaN/SiC, GaN/Si, and Graphene-Based FET.

3.1 Small-signal model topologies

As mentioned in section 2.5, the small-signal model should be able to consider all components that model the physical behavior of the device. The elements associated with the active region of the device are known as intrinsic elements. The intrinsic network may include the channel capacitances, gate forward and breakdown conduction elements, output impedance, and channel transconductance. The elements associated with the outside network are known as extrinsic elements. These elements may include capacitive effects of pad connections, probes, and probe tip-to-device contact transitions. It can also model the parasitic conduction through the substrate due to finite substrate resistance and buffer-trapping effects. Figure 3.1 shows parasitic elements and conduction elements mapped on a basic GaN HEMT structure.

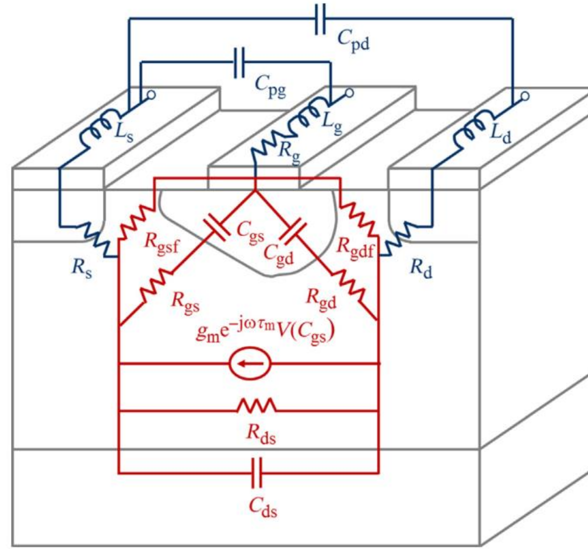

Figure 3.1 Parasitic and conductive elements of GaN HEMT showing intrinsic (red) and extrinsic (blue) elements [1].

3.1.1 Intrinsic Circuit

A typical intrinsic network is shown in Figure 3.2. This network considers all intrinsic components that can be found in a typical GaN HEMT. In this figure, C_{gs} is a lumped capacitance that comprises of three capacitance elements namely, the capacitance due to the depletion layer separating the gate and the 2DEG from the source side, the fringing capacitance between the gate and the GaN Cap, and the capacitance between the inter-electrodes of the gate and the source. C_{gs} can be summarized as an intrinsic gate-to-source capacitance. C_{gd} is the intrinsic gate-to-drain capacitance and has the same distribution of C_{gs} but with the drain instead of the source. R_i and R_{gd} are resistances associated with the charging and discharging of the depletion region from the source side and the drain side, respectively [2]. G_{gsf} is the forward gate conduction and G_{gdf} is the gate breakdown conductance. These two conductive elements are due to the diode-like behavior occurring in the device active regions. G_m is the channel transconductance [2]. τ is the transit time of electrons to move from the source to the drain. The exponential function is due to the reduction of the transconductance at higher frequencies due to the electrons' transit time τ. G_{ds} and C_{ds} form the intrinsic output impedance modulated by

the drain voltage. G_{ds} can be attributed to drain-to-source channel length modulation and C_{ds} to the intrinsic capacitance between the source and the drain [2].

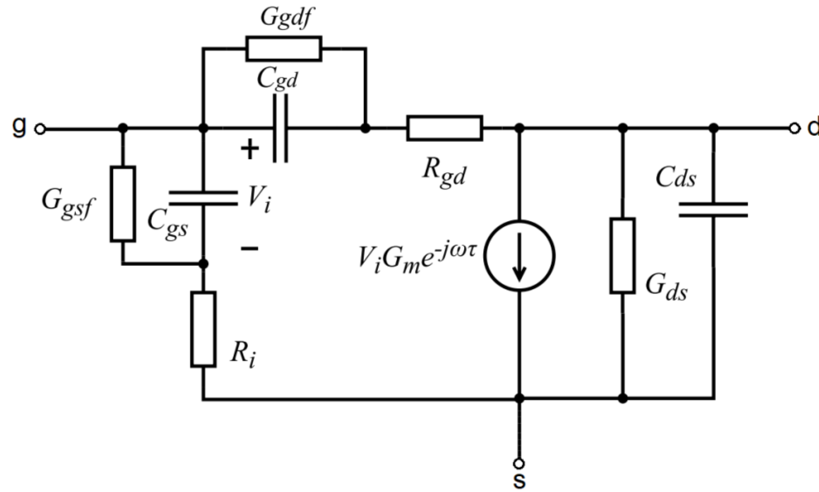

Figure 3.2 Intrinsic small-signal model of GaN HEMT [2].

It should be noted that the intrinsic parameters are bias dependant, which requires *S*-parameters measurements at different bias points. It is extremely important to guarantee accurate estimates of C_{gs}, C_{gd} and C_{ds} under pinch-off point because these intrinsic capacitances are correlated with the extrinsic capacitances and hence they affect the extracted intrinsic elements at these multiple bias points. The multi-bias intrinsic elements can be used to build a simple EC-LSM.

3.1.2 Extrinsic Circuits

There have been multiple approaches on which extrinsic network best describes the extrinsic part of the GaN HEMT. Figure 3.3 shows the most commonly used extrinsic networks for the GaN HEMT [2-10]. All of them include extrinsic series resistances (R_g, R_d, and R_s) and inductances (L_g, L_d, and L_s). R_s and R_d are due to the source and drain ohmic contacts, respectively. R_g is due to the gate metallization [1]. L_g, L_s, and L_d are related to the inductive contribution of the metallic contact pads and access transmission lines. The model in Figure 3.3a takes into consideration all expected parasitic elements of the device and reflects the physics of the device over a wide bias and frequency range [3]. This model is accurate for large gate devices where the electrode and crossover

capacitances can be distinguished from pad capacitances [3]. In this model, C_{gsi}, C_{gdi} and C_{dsi} are related to the inter-electrode and crossover capacitances between the gate, source and drain. C_{gp}, C_{dp} and C_{gdp} take into consideration the capacitances due to pad connections, probes and probe tip-to-device contact transition [3]. C_{pg} is assumed to be equal to C_{dp} under the conditions of symmetry between the two pads or/and the measuring probes. C_{gdi} is assumed to be equal to twice the value of C_{gdp}. If the spacing between gate-to-source and gate-to-drain are equal, we can assume $C_{gs} = C_{gd}$. It was also found that making $C_{dsi} = 3C_{pd}$ minimizes the error significantly [3].

The model in Figure 3.3b is used for small GaN HEMT devices where the interelectrode capacitances and the crossover capacitances may be ignored [4]. As a result, the model simplifies to an extrinsic network of C_{gp} and C_{dp} only. In this model, the values of C_{gp} and C_{dp} are tuned until a predefined error value is reached [4]. The extractor should be designed carefully to make sure reliable values are achieved when the minimal error is found. For example, C_{gp} should not be significantly different from C_{dp} to take into account the symmetry of the device's pads [3]. However, both models in Figure 3.3a and 3.3b do not take into account parasitic conduction through the substrate related to the finite electrical resistance of the substrate and buffer-trapping effects. Parasitic conduction is critically exhibited by GaN/Si devices and mildly exhibited by GaN/D [5], [11]. GaN/SiC has a very good lattice matching between the GaN buffer and SiC substrate. GaN/Si must include a substrate model meaning that the models in 3.3a and 3.3b fail to characterize the device [2]. The models in Figures 3.3(c-e) take into consideration the substrate network to model parasitic conduction [6-10]. Figure 3.3c introduces R_{gg}, C_{gg}, R_{dd} and C_{dd} to model the parasitic conduction through the substrate, which induces a leakage current through the substrate. In this model, due to a large number of unknowns, it was assumed that C_{gs} should be equal to C_{gd} under conditions of symmetry, and C_{ds} should be at minimum value [2]. The model may also include a shunt pad resistances R_{gp} and R_{dp} as shown in Figure 3.3d [7]. However, this model was tested in [8] using open test structure for GaN/Si and showed that the values of R_{gp} and R_{dp} are very large compared to the impedances of C_{gp} and C_{dp} at lower frequencies, hence the model can be simplified to the one shown in Figure 3.3c. The model in Figure 3.3e was also proposed to improve the accuracy of the substrate model for GaN/Si. The model

proposes the inclusion of segments of RC network to model the p-i-n parasitics of the p-silicon/GaN/Metal layers within the GaN/Si structure [5], [9]-[10]. The major disadvantages of such topology is an increase in complexity of the extractor, as well as an increase in the number of parameters that need to be optimized, which makes it more likely for the optimizer to fall in local minima points.

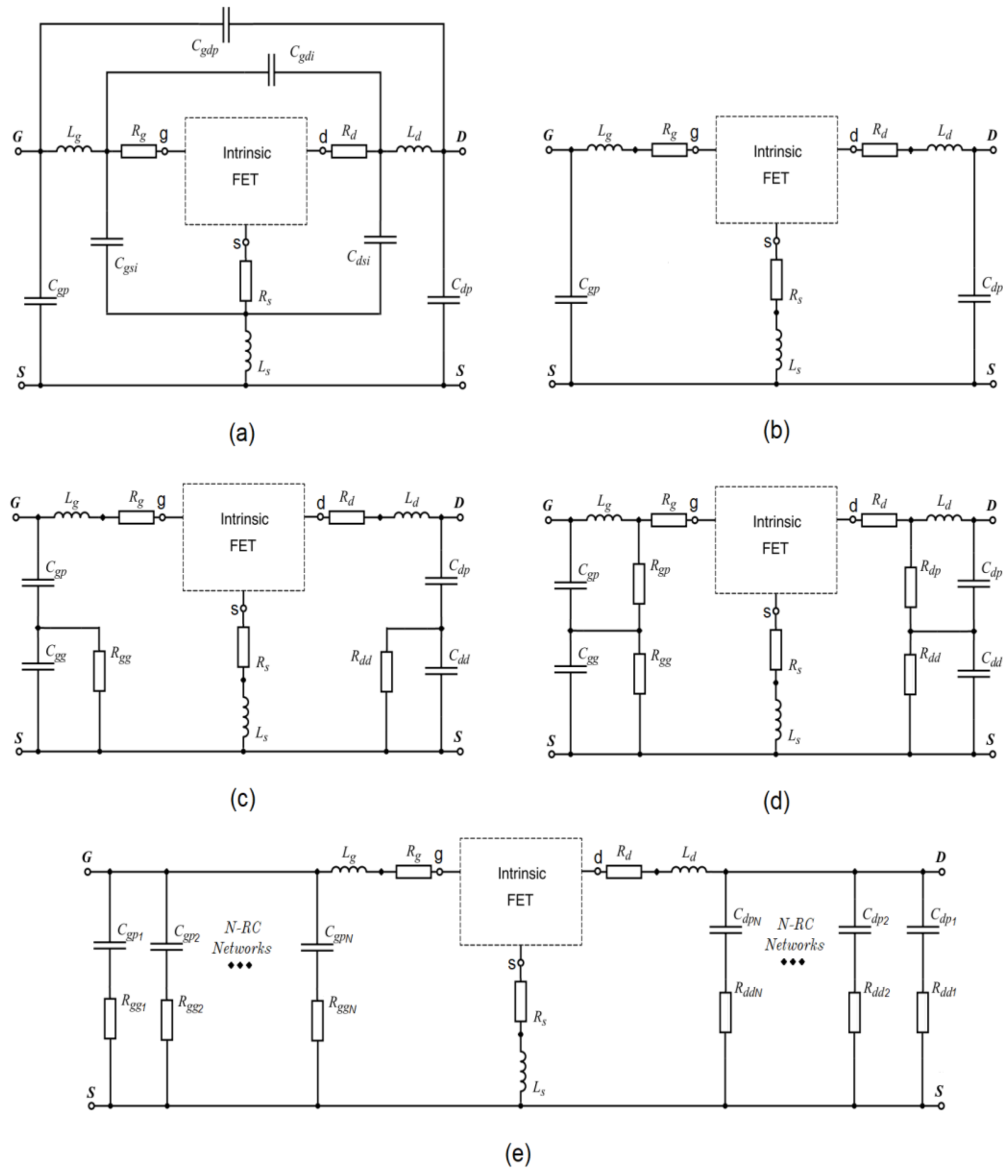

Figure 3.3 Different circuit topologies for GaN HEMT (a) for large periphery gates with no substrate model, (b) GaN/SiC model for small devices with no substrate model, (c) model for small devices with substrate model (d) another configuration for substrate model and (e) N-RC substrate model [2]-[10].

The extrinsic parameters are bias independent, and hence they are extracted only once (and optimized once) for all bias points (under the conditions that they are independent of frequency and bias voltages). The extrinsic parameters can be extracted using various methods and techniques as will be seen in section 3.3.

For our developed extraction technique, we have decided to choose the model in Figure 3.3c. The model is suitable for evaluating the parasitic conduction through the substrate as appose to the first two models. In addition to that, it has a lower number of components compared to Figures 3.3d and 3.3e thus, minimizing the computational costs for both the extractor and the optimizer. The model should also work even if parasitic conductions are at minimal effects.

3.2 RF Performance metrics

There are two figures of merits used to characterize the performance of GaN HEMTs: the unity current-gain cutoff frequency f_t and the unity power-gain cutoff frequency f_{max}. f_t and f_{max} set up the design constraints for the GaN HEMT such as the operating frequency, size, gain, and number of gate fingers. In order to find f_t, we need to find the magnitude of the short-circuit current gain $|h_{21}|$ first and then equate it to 1. With the help of the simplified circuit in Figure 3.4, we can write the current equations as follows:

$$I_{in} = V_i j\omega(C_{gs} + C_m) \tag{3.1}$$

$$I_{out} = \frac{G_m R_{ds} V_i e^{-j\omega\tau}}{(R_d + R_s + R_{ds})} \tag{3.2}$$

where C_m is the miller capacitance calculated using:

$$C_m = C_{gs} + C_{gd}(1 + G_m e^{-j\omega\tau} \frac{R_{ds}(R_d + R_s)}{R_{ds} + R_d + R_s}) \tag{3.3}$$

dividing (3.2) by (3.1) and taking the magnitude, we get:

$$|h_{21}| = \left|\frac{I_{out}}{I_{in}}\right| = \frac{G_m R_{ds}}{\omega(C_{gs} + C_{gd})(R_{ds} + R_d + R_s) + C_{gd}\omega G_m R_{ds}(R_d + R_s)} \tag{3.4}$$

given $\omega=2\pi f$, by equating (3.4) to one and solving for f_t we get the final equation:

$$f_t = \frac{G_m}{2\pi(C_{gs}+C_{gd})(1+G_{ds}(R_s+R_d))+G_m C_{gd}(R_s+R_d)} \tag{3.5}$$

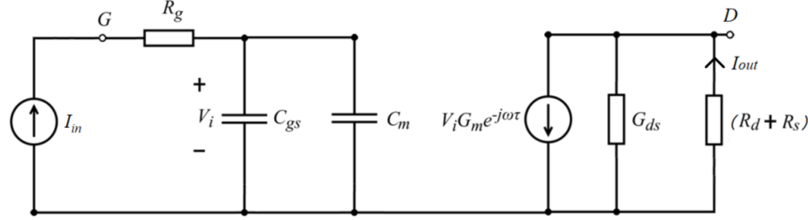

Figure 3.4 Small-signal model for calculations of f_t.

In order to derive an equation for f_{max}, we have to find the maximum power gain G_{max} and equate it to 1. However, the derivation requires the addition of a conjugate power matching in order to achieve this maximum power gain. The equation in (3.5) may be simplified to assist in the derivation. If we neglect the extrinsic series resistances and the drain to source channel length modulation and assume $C_{gs}>>C_{gd}$, we can rewrite (3.5) as:

$$f_t \cong \frac{G_m}{2\pi C_{gs}} \tag{3.6}$$

and hence (3.4) can be written as:

$$\left|\frac{I_{out}}{I_{in}}\right| = \frac{G_m}{2\pi f C_{gs}} = \frac{f_t}{f} \tag{3.7}$$

we may use the circuit in Figure 3.5 to assist in the derivation of f_{max}. Under match conditions, the maximum power gain can be written as:

$$G_{\max} = \frac{\frac{1}{2} I_{out}{}^2 R_{out}}{\frac{1}{2} I_{in}{}^2 R_{in}} = \frac{1}{4}\left(\frac{f_t}{f}\right)^2 \frac{R_{out}}{R_{in}} \tag{3.8}$$

where the current is halved due to the current splitting between the load and the output resistance (or the input and the input resistance) and quartered due to the resistance being halved due to impedance matching.

R_{out} and R_{in} can be formulated as follows:

$$R_{out} \cong \left(\frac{1}{R_{ds}} + \frac{G_m C_{gd}}{C_{gs} + C_{gd}}\right)^{-1} \tag{3.9}$$

$$R_{in} = R_g + \frac{1}{j\omega C_{gs}} + R_s + R_i \cong R_g + R_s + R_i \tag{3.10}$$

hence substituting (3.9) and (3.10) in (3.8) and using (3.6), we can equate G_{max} to 1 and solve for f_{max}, we get:

$$f_{\max} \cong \frac{1}{2} \frac{f_t}{\sqrt{2\pi f_t C_{gd}(R_g + R_s + R_i) + G_{ds}(R_g + R_s + R_i)}} \tag{3.11}$$

Figure 3.5 Small-signal model for f_{max} formulation.

We may surmise from the expressions in (3.5) and (3.11) that f_t and f_{max} are reduced due to the extrinsic series resistances and to the finite output channel conductance. f_{max} is also affected by the series gate resistance, which can be reduced by adding more gate fingers in parallel.

3.3 Extrinsic parameters extraction techniques

In order to achieve high accuracy in extracting the intrinsic network of GaN HEMT, we must guarantee accurate reliable extraction of the extrinsic network. There are two different techniques used to extract the extrinsic network.

3.3.1 Extraction using open, short and thru test structures.

Test structures fabricated under different connections are used to simulate different branches of the extrinsic network of the GaN HEMT. These tests are open, short and thru structures [12]. Figure 3.6 shows all possible test structures of GaN HEMT with their equivalent circuit models in Figure 3.7. The open test structure (Figures 3.6b and 3.7b) is patterned in a way such that all terminals of the GaN HEMT are isolated from each other, hence under such conditions, only the capacitive admittances will be measured by the RF probes [12]. In short test structure (Figures 3.6c and 3.7c), the gate, the drain, and the source are shorted together. This test structure includes all inductive and resistive impedances and capacitive admittances of the extrinsic network [12]. For the open structure, we may perform *S*-parameters measurements and convert them to *Y*-parameters in order to extract Y_{P1}, Y_{P2} and Y_{P3} by using two-port network techniques. The extracted parameters then get de-embedded from the short structure by converting them from *Y*-parameters to *Z*-parameters and removing Z_{P1}, Z_{P2} and Z_{P3} effects. This is known as two steps de-embedding technique [13]. Two-port network formulas can be used to determine the series impedances Z_{L1}, Z_{L2} and Z_{L3}. In order to improve the extracted parameters, thru structure may be used (Three steps de-embedding technique) [12]. Figures 3.6d and 3.7d show the thru structure. Thru structures occur when shorting the gate with the drain while leaving the source open. After being extracted, the parameters may be embedded together to produce the final extrinsic network for the GaN HEMT, as shown in Figure 3.7a.

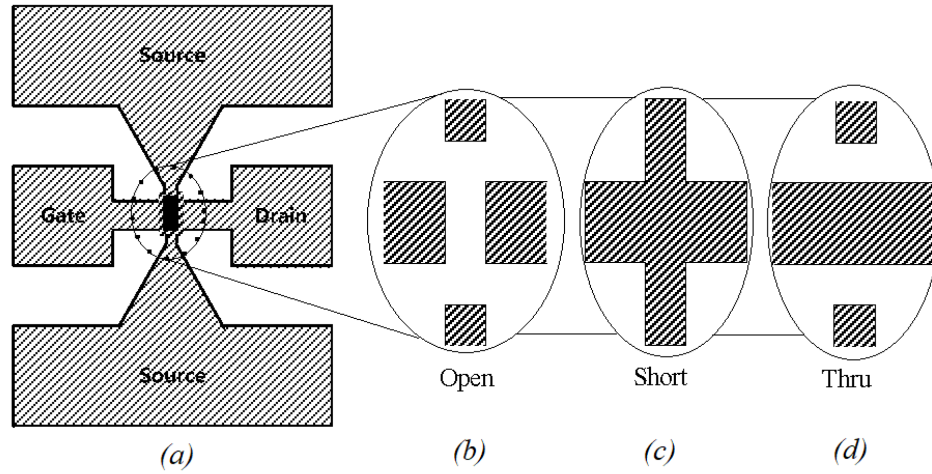

Figure 3.6 Different test structures for GaN HEMT: (a) normal, (b) open, (c) short and (d) thru structures [12].

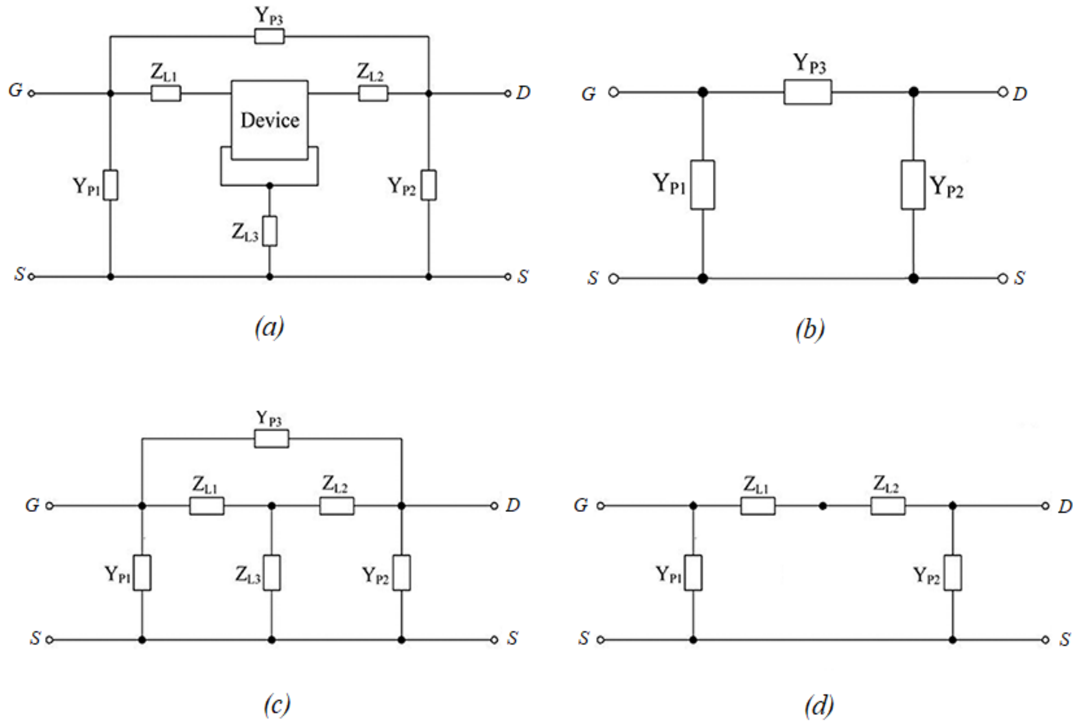

Figure 3.7 Circuit models for test structures of GaN HEMT: (a) normal, (b) open, (c) short and (d) thru structures [13].

This technique provides high accuracy for the extracted extrinsic network due to the isolation feature of the test structures. However, test structures might have to be customized in order to characterize each fabricated device, which is costly.

3.3.2 Extraction using cold pinch-off and cold forward *S*-parameters measurements

In this technique, we can extract the extrinsic parameters by splitting the extrinsic network into two different networks. We have the *Y*-parameters network consisting of the pad capacitances and possibly the substrate model and the *Z*-parameters network consisting of the series extrinsic resistances and inductances. The values of the elements used to construct the *Y*-network can be extracted under conditions of low frequency and cold pinch-off point (i.e. V_{GS} at minimal value and $V_{DS} = 0V$) [14]. After extracting the *Y*-network, we can de-embed the *Y*-network from the *Z*-network by converting the *Y*-parameters into *Z*-parameters and then subtracting their influence. The elements of the *Z*-network can be determined under the conditions of high frequency and cold pinch-off point [14]. The *Y*-network extracted earlier is embedded into the *Z*-network to build the extrinsic network of the GaN HEMT.

The accuracy of the elements of the *Z*-network can be improved by having cold forward *S*-parameters measurements of the device [14], [15]. By de-embedding the *Y*-network from the *Z*-network, we can extract the series inductances and series resistances at cold forward *S*-parameters measurements (i.e. $V_{GS} = 0V$ and $V_{DS} = 0V$). However, involving forward *S*-parameters measurements will increase the complexity of the extractor without significant improvement in accuracy [16]. The advantage of such an extraction technique is that it can rely only on one set of *S*-parameters measurements (cold pinch-off) in order to extract all the extrinsic components; furthermore, it does not require test structures for each fabricated device, which facilitates automation for different devices.

3.4 Proposed extrinsic parameters extraction technique

Because different substrates imply different effects on GaN HEMT performance (for example parasitic conduction at lower frequencies for GaN/Si, buffer-trapping effects in GaN/D and self-heating effects in GaN/SiC), multiple circuit topologies were developed

as was seen in subsection 3.1.2. Each circuit topology requires a unique extraction technique in order to extract the extrinsic parameters of the GaN HEMT [2]. This approach makes it difficult to automate the extraction process by having a library of different models with different extraction techniques. In addition to that, most existing extraction techniques do not take into account the asymmetry between C_{gs} and C_{gd} due to asymmetrical GaN structure, buffer-trapping effects, and passivation layer inclusion [17].

Our proposed extraction technique uses only one extraction technique and one single EC-SSM that can be applied to GaN HEMTs built on different substrates. It helps to automate the extraction technique, a key issue in CAD approaches. Another advantage of this extraction technique is that it takes into account the effects of GaN asymmetrical structure, charge-trapping, and passivation layer deposition on the asymmetry between C_{gs} and C_{gd} values. It also takes into account the substrate conduction effect. The extraction technique can be divided into two parts: the first is related to the reliable extraction of C_{gs} and C_{ds} values and the second is related to the substrate parameters extraction. Figure 3.8 shows the proposed EC-SSM.

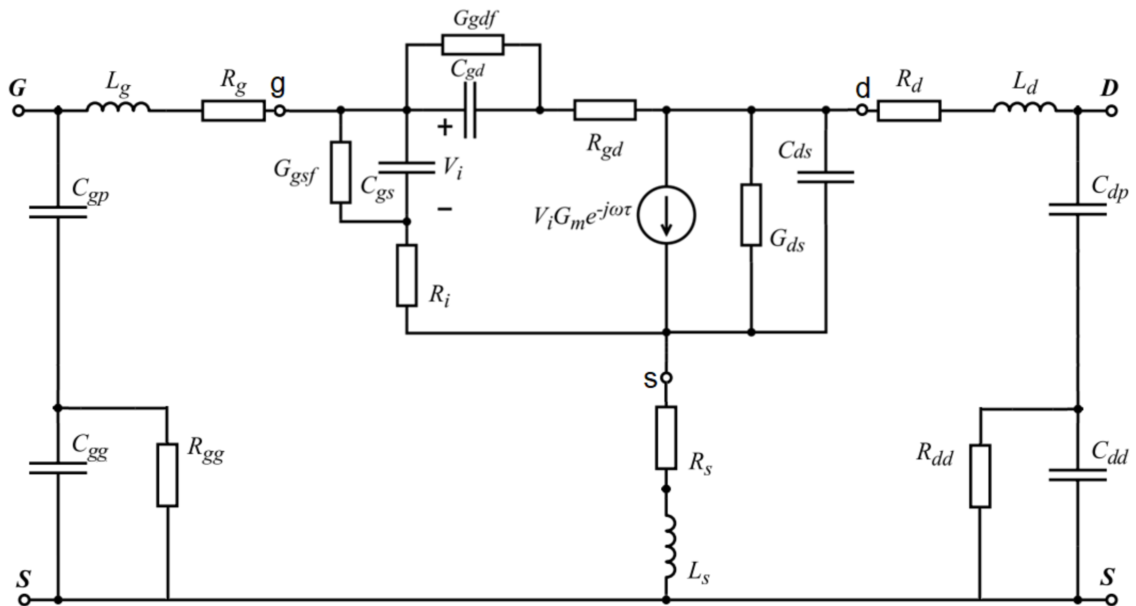

Figure 3.8 Proposed equivalent circuit-small-signal model [2].

Before going into the proposed extraction technique, it is very important to determine at which frequencies some of the extrinsic parameters may be neglected. This is very important for the reasons of simplifying the extraction technique. Figure 3.9 shows a generic plot of the imaginary part of the *Y*-parameters over ω vs. ω. This plot is taken under the conditions of cold pinch-off bias point, meaning that all conduction elements inside the intrinsic network can be neglected; hence we are left off with the extrinsic network and intrinsic capacitances [14].

We may notice from the plot that there are three regions at which the Im[*Y*]/ω changes dramatically. The first region is at low frequencies. In this region, the pad capacitances C_{pg} and C_{pd} with the substrate model C_{gg}, R_{gg}, C_{dd} and R_{dd} and the intrinsic capacitances C_{gs}, C_{gd} and C_{ds} are most dominant [2]. The inductances and series resistances have extremely small contributions at lower frequencies and hence they may be ignored [2]. The second region is the intermediate frequency region. In this region, R_{gg} and R_{dd} can be neglected and hence C_{gg} and C_{pg} (C_{dd} and C_{pd}) may be combined as one element (as will be seen later). In the third region of high frequencies, the inductive effects and series resistances are most dominant and hence they must be considered. It should be noted that the intrinsic capacitances are existent at all frequencies [2]. It should also be noted that some devices that do not exhibit parasitic conduction through the substrate have indistinguishable Im[*Y*]/ω at regions I and II (constant with frequency) as in GaN/SiC.

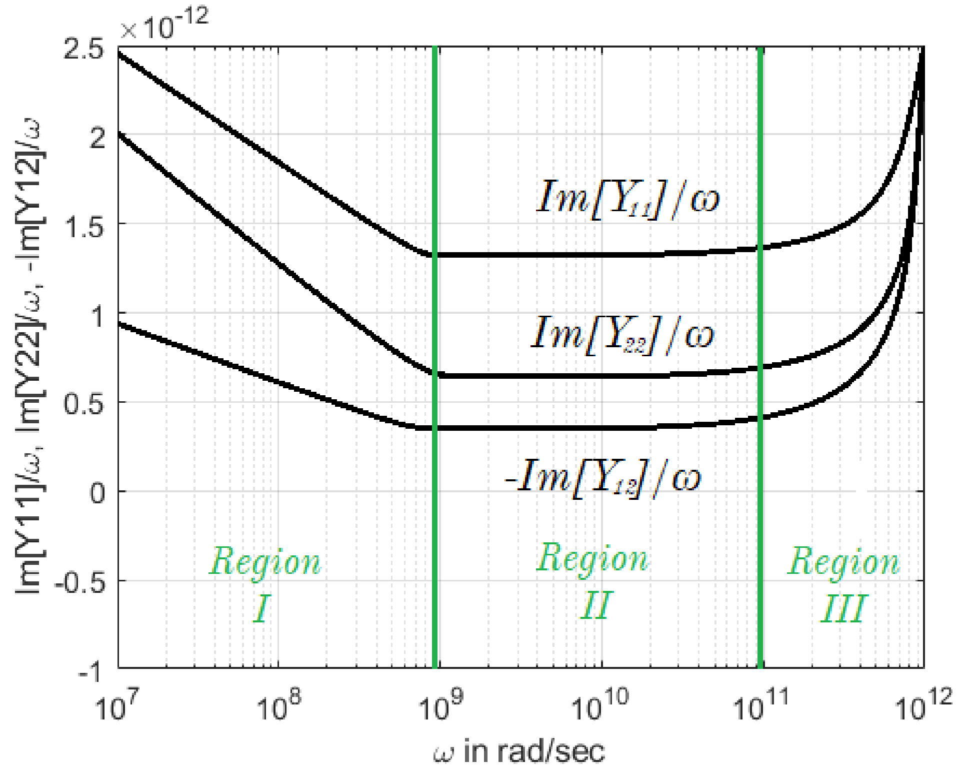

Figure 3.9 Imaginary of Y over ω plot showing three different regions of interest.

While extracting the extrinsic capacitances below the pinch-off point at cold conditions, we will be presented with more variables than the number of Y-parameters' equations necessary for describing them [18]. It is a common approach to scan the pad capacitances C_{gp} and C_{dp} until a minimal error is reached while making assumptions on the other extrinsic and intrinsic capacitances [18-22]. These assumptions are made based on the physics and the structure of the device. Few references, for example, have set $C_{gs} = C_{gd}$ and $C_{ds} = 0$ assuming a symmetrical GaN HEMT structure [19][20], while others assumed equivalent pad capacitances [21][22]. In our case, we have minimized such assumptions and depended mainly on the scanning of C_{gp} and C_{dp} to extract the extrinsic parameters. Therefore, our extraction technique will be suitable for both symmetrical and asymmetrical devices regardless of the type of substrate used.

3.4.1 Phase 1: C_{gs} and C_{ds} estimation

The first phase is concerned with extracting reliable values for C_{gs} and C_{ds}. Under cold-pinch off bias voltages and low frequencies (Region I), the circuit in Figure 3.8 may be simplified as shown in Figure 3.10. All conduction elements in the intrinsic network are neglected with the extrinsic series inductances and resistances. We may write Y-parameters expressions as follows [23]:

$$Y_{11} = Y_{gg} + j\omega(C_{gs} + C_{gd}) \tag{3.12}$$

$$Y_{22} = Y_{dd} + j\omega(C_{ds} + C_{gd}) \tag{3.13}$$

$$Y_{12} = Y_{21} = -j\omega C_{gd} \tag{3.14}$$

where

$$Y_{gg} = \frac{j\omega C_{gp}(1 + j\omega C_{gg} R_{gg})}{1 + j\omega R_{gg}(C_{gp} + C_{gg})} \tag{3.15}$$

$$Y_{dd} = \frac{j\omega C_{dp}(1 + j\omega C_{dd} R_{dd})}{1 + j\omega R_{dd}(C_{dp} + C_{dd})} \tag{3.16}$$

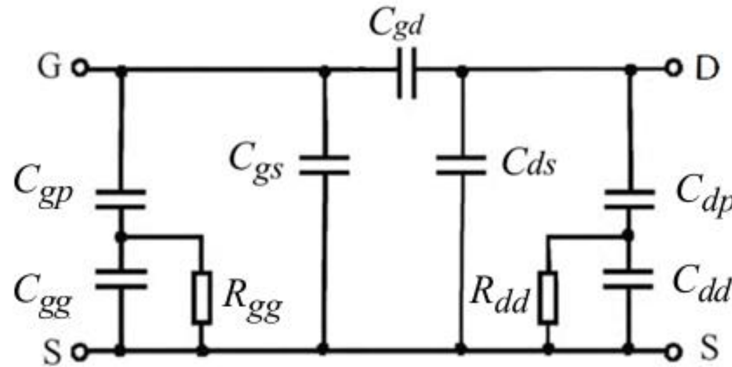

Figure 3.10 GaN HEMT extrinsic network at Region I [23].

The basis of the extraction technique is to scan the values of C_{gp} and C_{dp} (as detailed later) in order to determine the remaining values of the extrinsic parameters of the EC-SSM. However, the values of C_{gg} and C_{dd} require extracted values of both C_{gs} and C_{ds}, which are difficult to estimate. Consequently, we should extract first the values of C_{gs} and C_{ds} using a simpler model (Figure 3.11) valid at Region II (R_{gg} and R_{dd} are both neglected) and, then, by combining the series combinations of both C_{gp} and C_{gg} (C_{dp} and C_{dd}) into a single capacitance. We confirm that this approach is valid and can be verified by taking the limits of (3.15) and (3.16) as ω approaches infinity. Another way to verify this simplification is by observing the plot that was shown in Figure 3.9; where at Region II, the $\omega\text{Im}[Y]$ plots are constant with a frequency indicating that the admittance is purely capacitive. The corresponding new simplified equations can be set as [4]:

$$Y_{11} = j\omega(C_{gp} + C_{gs} + C_{gd}) \tag{3.17}$$

$$Y_{22} = j\omega(C_{dp} + C_{ds} + C_{gd}) \tag{3.18}$$

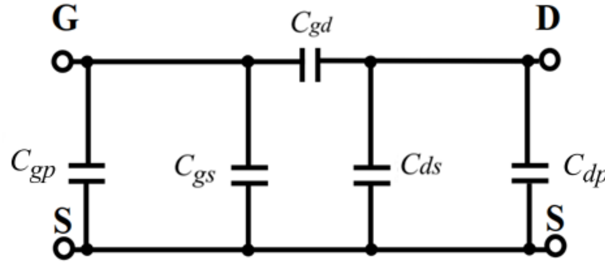

Figure 3.11 GaN HEMT extrinsic model at Region II [4].

It is clear that the expressions have been simplified greatly compared to (3.12) and (3.13). C_{gd} can be calculated by taking the imaginary part of ($-Y_{12}/\omega$). C_{gs} and C_{ds} can be calculated from the imaginary part of (3.17) and (3.18) divided by ω while C_{gp} and C_{dp} are already defined through the scanning process [4]. After extracting the extrinsic and intrinsic capacitances, C_{gp} and C_{dp} are de-embedded from the overall circuit by converting the Y-parameters into Z-parameters and then subtracting their effects from the

overall *Z*-expressions. By moving the extraction into high frequencies (Region III), the inductance effects will appear (Figure 3.12), where C_g, C_s and C_d result from converting C_{gs}, C_{gd} and C_{ds} from delta- to wye-network for simplification purposes. From Figure 3.12, we have [4]:

$$Z_{11} = R_g + R_s + j\omega(L_g + L_s) + \frac{1}{j\omega}\left(\frac{1}{C_g} + \frac{1}{C_s}\right) \tag{3.19}$$

$$Z_{22} = R_d + R_s + j\omega(L_d + L_s) + \frac{1}{j\omega}\left(\frac{1}{C_d} + \frac{1}{C_s}\right) \tag{3.20}$$

$$Z_{12} = Z_{21} = R_s + j\omega L_s + \frac{1}{j\omega C_s} \tag{3.21}$$

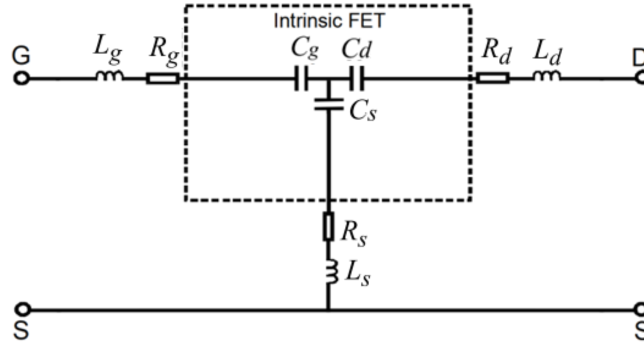

Figure 3.12 GaN HEMT at Region III after de-embedding the extrinsic capacitances.

We can then obtain the values of the inductances by multiplying by ω the *Z*-expressions in (3.19)-(3.21) and then taking the imaginary part [4]:

$$\mathrm{Im}[\omega Z_{11}] = \omega^2(L_g + L_s) - \left(\frac{1}{C_g} + \frac{1}{C_s}\right) \tag{3.22}$$

$$\mathrm{Im}[\omega Z_{22}] = \omega^2(L_d + L_s) - \left(\frac{1}{C_d} + \frac{1}{C_s}\right) \tag{3.23}$$

$$\mathrm{Im}[\omega Z_{12}] = \omega^2 L_s - \frac{1}{C_s} \tag{3.24}$$

As seen from (3.24), we can get the value of L_s by plotting the Im[ωZ_{12}] vs. ω^2 and then calculating the slope using the linear regression technique. Similarly for L_g and L_d by using (3.22) and (3.23), respectively. The next step is to de-embed the impedance of the inductances from the stripped Z-parameters. This can be achieved directly by subtracting the impedance of the inductors from the stripped impedances. After that, the series resistances can be extracted using the same technique as for the inductances; however, the impedance expressions should be multiplied by ω^2 in order to reduce the nonlinearities caused by the incomplete de-embedding of the extrinsic capacitances and inductances [4]. After multiplying the impedances by ω^2 and then taking their real part, we get:

$$\mathrm{Re}[\omega^2 Z_{11}] = \omega^2 (R_g + R_s) \tag{3.25}$$

$$\mathrm{Re}[\omega^2 Z_{22}] = \omega^2 (R_d + R_s) \tag{3.26}$$

$$\mathrm{Re}[\omega^2 Z_{12}] = \omega^2 R_s \tag{3.27}$$

To get R_s, we plotted Re[$\omega^2 Z_{12}$] vs. ω^2 and then used linear regression to get its value. Similarly for R_g and R_d by using (3.25) and (3.26), respectively. Up to this point, all the extrinsic components are extracted except R_{gg}, R_{dd}, C_{gg}, C_{dd}, and the intrinsic capacitances.

The main point behind the above extractions is to reach a good estimation of the values of C_{gs} and C_{ds} before including the remaining extrinsic components. To do so, as mentioned above, both C_{gp} and C_{dp} are incrementally scanned from 0 up to the maximum allowable values in (3.17) and (3.18). At each iteration, using the new incremental values for C_{gs} and C_{ds}, the resultant simulated S-parameters S^{Sim} are compared with measured data S^{Meas} until reaching a user-defined minimum error value, which expression has been set as [24]:

$$\varepsilon = \frac{1}{N} \sum_{i,j=1}^{2} \sum_{k=1}^{N} \frac{|\mathrm{Re}(S_{ij}^{Sim} - S_{ij}^{Meas})|}{\max|\mathrm{Re}(S_{ij}^{Meas})|} + \frac{|\mathrm{Im}(S_{ij}^{Sim} - S_{ij}^{Meas})|}{\max|\mathrm{Im}(S_{ij}^{Meas})|} \tag{3.28}$$

The values that provide the minimum error will be used to estimate the final values of C_{gs} and C_{ds}. In the above equation, N is the number of data points. A plot of the scanning process using (3.28) for the case of GaN/D and GaN/SiC can be seen in Figure 3.13. As seen from the figure, there is a broad range of values at which the minimum value occurs. However, the only reliable value is the one that gives us both the minimal error and close values between C_{gp} and C_{dp} to take into account the symmetry of the pad capacitances.

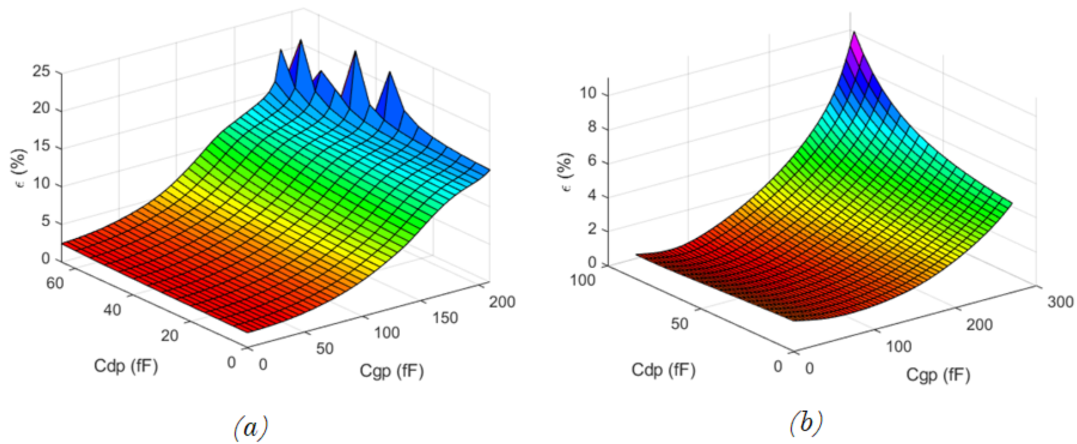

Figure 3.13 C_{gp} and C_{dp} scanning plots to determine the minimum error for (a) GaN/D and (b) GaN/SiC.

3.4.2 Phase 2: Substrate model extraction

After extracting the reliable values of C_{gs} and C_{gd}, R_{gg}, R_{dd}, C_{gg} and C_{dd} are re-inserted, as shown in Figure 3.10. Knowing the values of C_{gs} and C_{gd}, (3.12) and (3.13) can be re-expressed in terms of (3.14) as:

$$Y_{gg} = Y_{11} + Y_{12}(1+\alpha) \tag{3.29}$$

$$Y_{dd} = Y_{22} + Y_{12}(1+\beta) \tag{3.30}$$

where

$$\alpha = \frac{C_{gs}}{C_{gd}}, \beta = \frac{C_{ds}}{C_{gd}} \tag{3.31}$$

In order to extract C_{gg} and C_{dd}, we have to consider the imaginary part of Y_{gg} and Y_{dd}, respectively. This should be achieved at Region II where the influences of R_{gg} and R_{dd} are negligible. Under such conditions, we can substitute (3.15) and (3.16) into (3.12) and (3.13), respectively, leading to:

$$\frac{\mathrm{Im}(Y_{11})}{\omega} = \frac{C_{gg}C_{gp}}{C_{gg}+C_{gp}} + C_{gs} + C_{gd} \tag{3.32}$$

$$\frac{\mathrm{Im}(Y_{22})}{\omega} = \frac{C_{dd}C_{dp}}{C_{dd}+C_{dp}} + C_{ds} + C_{gd} \tag{3.33}$$

The values of C_{gg} and C_{dd} can be then extracted. R_{gg} and R_{dd} can be calculated by substituting (3.15) and (3.16) into (3.29) and (3.30), respectively, and then by taking the inverse of the real part of both sides and multiplying them by ω^2:

$$\frac{\omega^2}{\mathrm{Re}[Y_{11}+Y_{12}(1+\alpha)]} = \frac{1}{R_{gg}C_{gp}^2} + \omega^2 R_{gg}\left(\frac{C_{gp}+C_{gg}}{C_{gp}}\right)^2 \tag{3.34}$$

$$\frac{\omega^2}{\mathrm{Re}[Y_{22}+Y_{12}(1+\beta)]} = \frac{1}{R_{dd}C_{dp}^2} + \omega^2 R_{dd}\left(\frac{C_{dp}+C_{dd}}{C_{dp}}\right)^2 \tag{3.35}$$

from these equations, the values of R_{gg} and R_{dd} can be deduced by plotting (3.34) and (3.35) vs. ω^2 and determining the slopes of the curves at Region I.

After extracting the pad capacitances and the substrate network of the circuit shown in Figure 3.10, the *Y*-parameters will be converted into *Z*-parameters and then de-embedded from the overall *Z*-parameter relations where the *Y*-network contribution will be removed. The resultant circuit will be as in Figure 3.12, and hence the remaining extractions of the series resistances and inductances can be completed in the same way as

described above in phase 1. C_{gp} and C_{dp} will be scanned again from 0 to max(Im[Y_{11}]/ω) and from 0 to max(Im[Y_{22}]/ω), respectively. The extracted values of all extrinsic parameters are chosen based on the minimal error calculated by (3.28). After extracting the extrinsic components and the intrinsic capacitances, we can determine the resultant *S*-parameters and compare them to measurements. However, it is recommended to optimize the obtained values using an optimization technique in order to improve accuracy and fine-tune them, as will be shown in the following section. A summary of the extraction technique is shown in the flow chart in Figure 3.14.

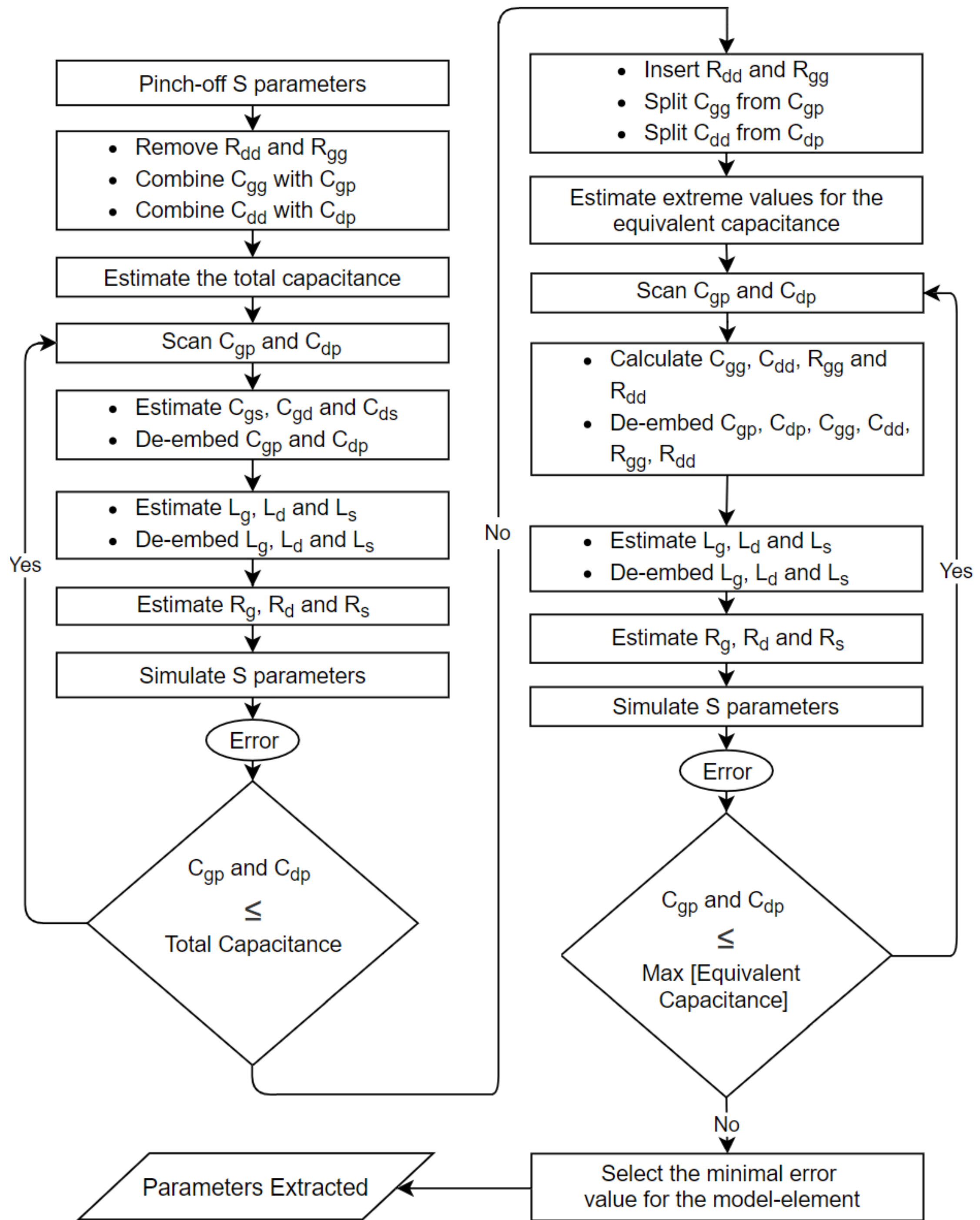

Figure 3.14 Flow chart of the extrinsic parameters extraction technique.

3.5 Proposed optimization technique

In order to improve the accuracy of our extracted parameters, we ran an efficient optimization tool, i.e., the Grey Wolf Optimizer (GWO) [25]. The reasons for choosing this particular optimization technique are its high accuracy, high convergence, and local optima avoidance capabilities [8][26]. In our extraction technique, we got the possible initial values for the extracted parameters, which minimize the probability of an optimized value being trapped in a local optimum; it also simplifies the operation of the optimization technique, leading to a high convergence rate.

In GWO, wolves are sent to hunt for multiple preys (feasible solutions) and then their social behavior is utilized to find the best prey (optimal solution) among the existing multiple preys [8]. There are three phases for the operation of GWO:

1. Tracking, chasing, and approaching the prey.
2. Encircling and forcing the prey to stop moving by harassing it.
3. Moving forward and attacking the prey.

In order to mathematically model the three phases of GWO, the wolf packs (search agents) were divided into four different groups namely, alpha (α_w), beta (β_w), delta (δ_w) and omega (ω_w) [8]. Here α_w is the leader of the wolf pack, which resembles the optimal solution. β_w and δ_w represent the second and third best solutions, respectively. The remaining of the solutions are defined by ω_w. The mathematical model of encircling the prey is given as follows [25]:

$$\vec{D} = |\vec{C}\overrightarrow{X}_p - \overrightarrow{X}(t)| \tag{3.36}$$

$$\overrightarrow{X}(t+1) = \overrightarrow{X}_p(t) - \vec{A}\vec{D} \tag{3.37}$$

where the coefficient vectors A and C are given by:

$$\vec{A} = 2\vec{a}\vec{r}_1 - \vec{a} \tag{3.38}$$

$$\vec{C} = 2\vec{r}_2 \tag{3.39}$$

where t the current iteration, X the wolf's position vector, and X_p the prey's position vector. r_1 and r_2 are random vectors ranging from 0 to 1, while the parameter a is linearly decreasing from 2 to 0 after each iteration [25]. The vector A representing the coefficient vector of the updated location of the search agents with respect to the prey also decreases with each iteration [8]. When $|A|$ becomes less than 1, the grey wolves attack the prey. On the other hand, if $|A|$ becomes greater than 1, the grey wolves diverge from the prey hoping to find a better prey [8]. The adaptive values of a and A allow a good balance between exploration and exploitation [8]. a, A, and C are initially generated based on an initial population random generator.

The hunt in GWO is led by alpha, beta, and delta wolves. Since the optimum solution is not known at the beginning of the algorithm, the alpha will be assumed as the best candidate solution while beta and delta wolves are considered second and third-best solutions, respectively. Consequently, random values are assigned to these wolves. The other wolves ω_w depend on their leaders α_w, β_w, and δ_w locations around the pray [25]. The ω_w change their values according to (3.40). It can be noted from (3.40) and (3.41) the effect of the α_w, β_w, and δ_w on the positions of the other search agents (or ω_w). In summary, the α_w, β_w, and δ_w wolves estimate the location of prey and the search agents update their locations around the prey. The formulas used for the wolves' location update mechanism are as follows [25]:

$$\vec{X}(t+1) = \frac{\vec{X}_1 + \vec{X}_2 + \vec{X}_3}{3} \tag{3.40}$$

where

$$\begin{aligned} &\vec{X}_1 = \vec{X}_{\alpha_w} - \vec{A}_1 \cdot \vec{D}_{\alpha_w}, \vec{X}_2 = \vec{X}_{\beta_w} - \vec{A}_2 \cdot \vec{D}_{\beta_w}, \\ &\vec{X}_3 = \vec{X}_{\delta_w} - \vec{A}_3 \cdot \vec{D}_{\delta_w} \end{aligned} \tag{3.41}$$

where

$$\begin{aligned} &\vec{D}_{\alpha_w} = \left|\vec{C}_1 \cdot \vec{X}_{\alpha_w} - \vec{X}\right|, \vec{D}_{\beta_w} = \left|\vec{C}_2 \cdot \vec{X}_{\beta_w} - \vec{X}\right|, \\ &\vec{D}_{\delta_w} = \left|\vec{C}_3 \cdot \vec{X}_{\delta_w} - \vec{X}\right| \end{aligned} \tag{3.42}$$

Figure 3.15 shows how the α_w, β_w and δ_w estimate the location of the prey while the other wolves update their locations randomly around the prey.

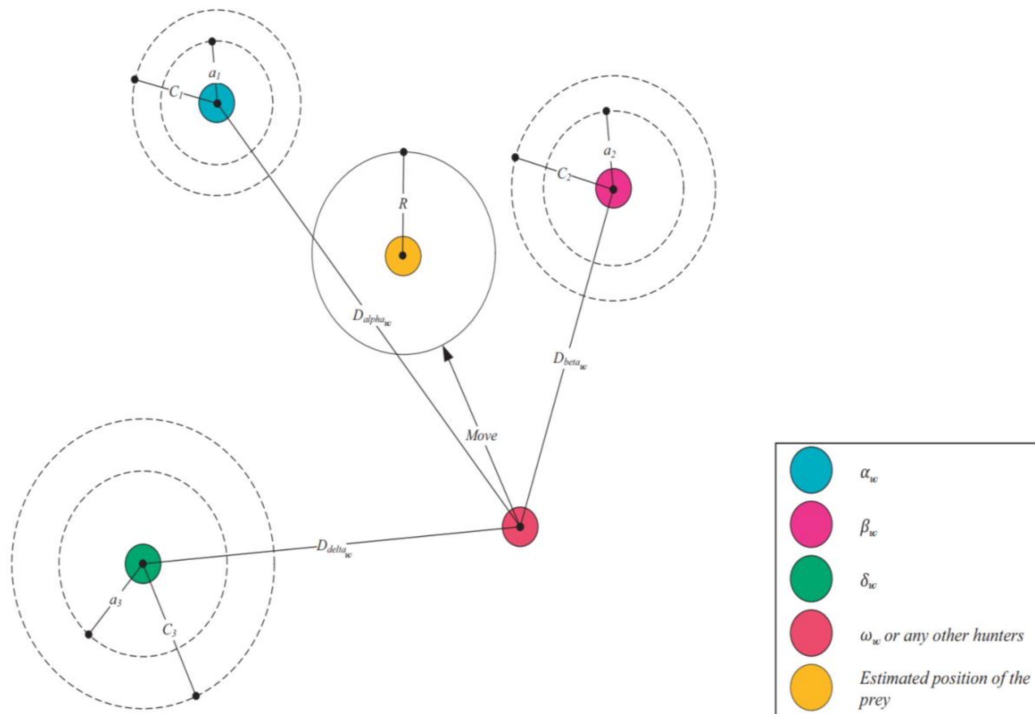

Figure 3.15 Position Updates in GWO [25].

It is of great importance to guarantee reliable parameters in the EC-SSM that can describe the physics and the parasitics of the device. Hence the GWO should only be used for fine-tuning the parameters around their initial extracted values (from the previous section). The purpose of the fine-tuning is to improve the accuracy of the extracted parameters since the scanning procedure for both C_{gp} and C_{dp} depends on a limited step-size (e.g. incremental value of Δ5 fF) which might cause the scanning procedure to skip the optimal values. The reason for such limitation is the computational cost attributed to the small step size and the large range of values to scan. For instance, scanning step sizes Δ5 fF, Δ2 fF and Δ1 fF have computational times of 46 seconds, 5.05 minutes and 19.27 minutes, respectively. So by choosing an appropriate step-size that reduces the computational time (i.e. Δ5 fF) and using GWO to optimize the values, we

guarantee optimal and physically reliable parameters that have low computational time (≈ 2 minutes). Figure 3.16 shows the fast convergence toward the minimum error for both GaN/D and GaN/SiC exploited by the initial values, while Figure 3.17 shows improved *S*-parameters after running the optimizer on GaN/Si.

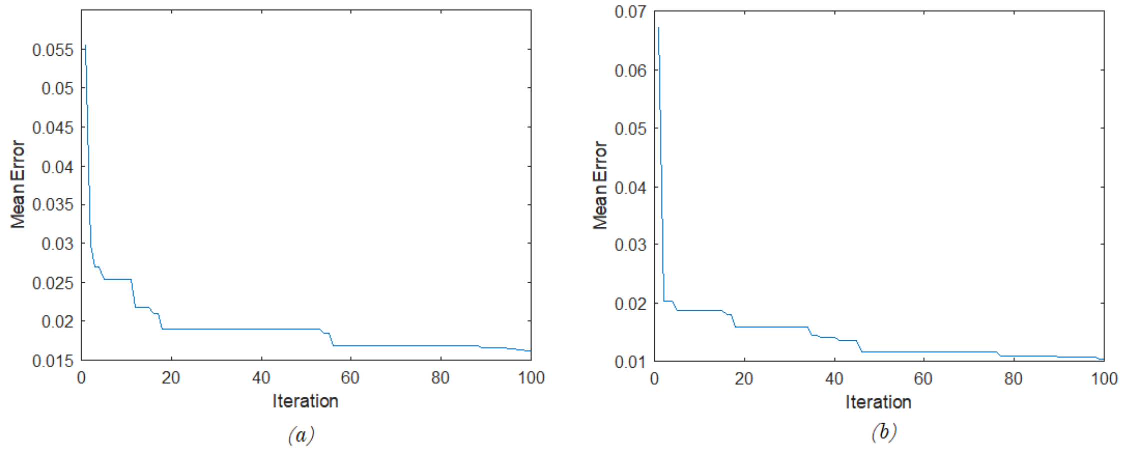

Figure 3.16 Convergence of GWO for optimizing the (a) GaN/D and (b) GaN/SiC parameters.

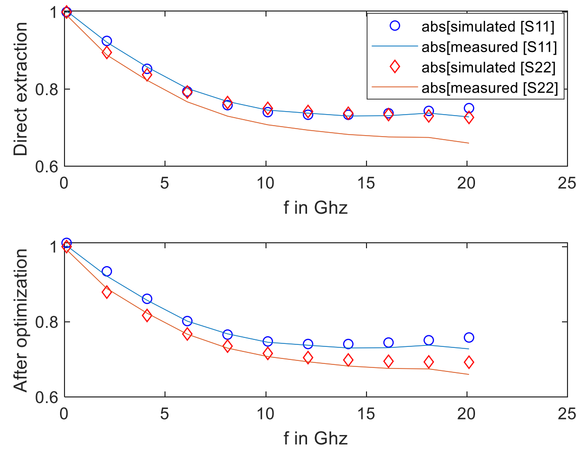

Figure 3.17 Comparison between S_{11} and S_{22} for GaN/Si before and after optimization.

3.6 Intrinsic parameters extraction

After extracting the extrinsic parameters and de-embedding them from the overall EC-SSM, we can extract the intrinsic parameters of the GaN HEMT. Unlike the extrinsic parameters, the intrinsic parameters are bias dependent and hence they must be extracted at multiple bias points. We may use the circuit shown in Figure 3.2 to aid us in writing the equations for the intrinsic network. The admittance of the intrinsic gate-to-source Y_{gs} can be written as [27]:

$$Y_{gs} = Y_{i,11} + Y_{i,12} = \frac{G_{gsf} + j\omega C_{gs}}{1 + R_i G_{gsf} + j\omega R_i G_{gsf}} \tag{3.43}$$

By defining a new variable D_1 as [27]:

$$D_1 = \frac{\left|Y_{gs}\right|^2}{\mathrm{Im}[Y_{gs}]} = \frac{G_{gsf}{}^2}{\omega C_{gs}} + \omega C_{gs} \tag{3.44}$$

hence, C_{gs} can be determined by finding the slope of ωD_1 vs. ω^2 through linear regression. By defining another D_2 as follows [27]:

$$D_2 = \frac{Y_{gs}}{\mathrm{Im}[Y_{gs}]} = \frac{G_{gsf}(1 + R_i G_{gsf})}{\omega C_{gs}} + \omega R_i C_{gs} - j \tag{3.45}$$

we can calculate the value of R_i by finding the real part of ωD_2 vs. ω^2 through linear regression. G_{gsf} can be found from the real part of Y_{gs} at low frequencies (below 1 GHz). The remaining elements C_{gd}, R_{gd} and G_{gdf} can be extracted in similar manners to the previous intrinsic elements by writing an equation for Y_{gd} as [27]:

$$Y_{gd} = -Y_{i,12} = \frac{G_{gdf} + j\omega C_{gd}}{1 + R_{gd} G_{gdf} + j\omega R_{gd} C_{gd}} \tag{3.46}$$

In order to extract G_m and τ, we need to write an equation of the admittance of the intrinsic transconductance as follows [27]:

$$Y_{gm} = Y_{i,21} - Y_{i,12} = \frac{G_m e^{-j\omega\tau}}{1 + R_i G_{gsf} + j\omega C_{gs}} \tag{3.47}$$

we can define D_3 as follows [27]:

$$D_3 = (G_{gsf} + j\omega C_{gs})\frac{Y_{gm}}{Y_{gs}} = G_m e^{-j\omega\tau} \tag{3.48}$$

G_m can be found by finding the magnitude of ωD_3 vs. ω through linear regression. τ may be found by plotting the phase of $-D_3$ vs. ω through linear regression. Finally, we can write an equation to describe the drain-to-source admittance as follows [27]:

$$Y_{ds} = Y_{i,22} + Y_{i,12} = G_{ds} + j\omega C_{ds} \tag{3.49}$$

G_{ds} can be determined by plotting $\omega\text{Re}[Y_{ds}]$ versus ω and finding the slope by linear regression. C_{ds} can be found by taking the imaginary part of Y_{ds} vs. ω and determining the slope.

3.7 Results and discussion

After extracting all the intrinsic and extrinsic parameters, we embedded them back together to build the EC-SSM, hence we can compare the simulated circuits with measurements obtained from technical literature. The first subsection shows the results of the extrinsic extraction technique and the optimizer that were applied on a 2x100 µm GaN/D and a 4x50 µm GaN/SiC [28][29]. The second subsection is about the results of the intrinsic parameters extraction.

3.7.1 Extrinsic parameters extraction results

To get the extrinsic parameter values, we first plotted $\text{Im}[Y_{11}]/\omega$, $\text{Im}[Y_{22}]/\omega$ and $-\text{Im}[Y_{12}]/\omega$ to extract the pad capacitances and the substrate model parameters, as shown in Figure 3.18 for both GaN/D and GaN/SiC. We may note from the figure that GaN/D exhibits small parasitic conduction at lower frequencies due to the difference in values of

the *Y*-parameters between low and intermediate frequency ranges. GaN/SiC also exhibits parasitic conduction at the drain side; however, through our extraction technique, it was found that the substrate model has negligible effects on GaN/SiC, and hence, it can be removed. This was validated by the literature [2] and, therefore, taken into account automatically by our extractor. Equations (3.12 – 3.18) were used to extract the extrinsic network parameters.

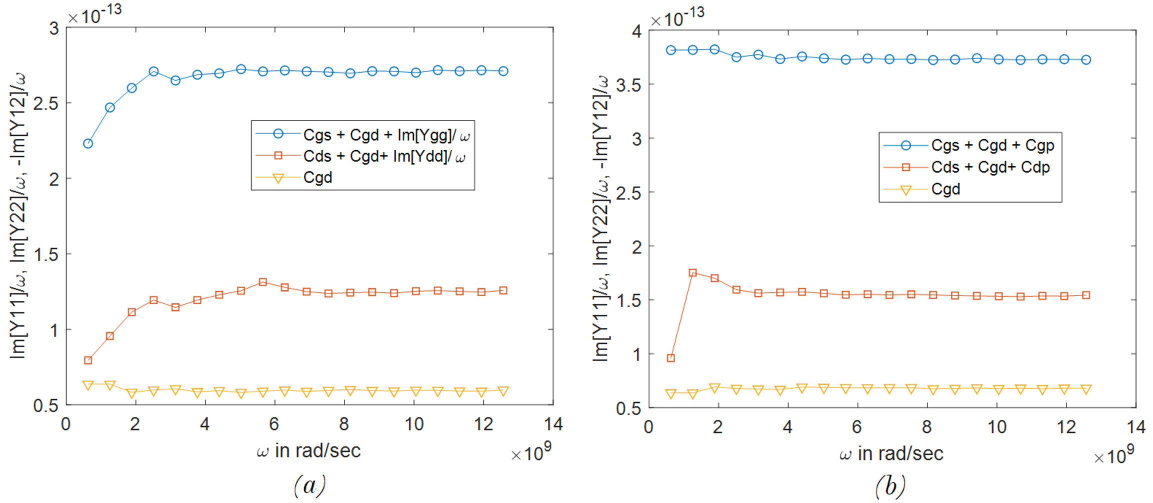

Figure 3.18 Extrinsic capacitances and substrate parameters extraction for (a) GaN/D and (b) GaN/SiC.

As already mentioned, extrinsic capacitances and the substrate model were first de-embedded from the total circuit. We then plotted $\omega\text{Im}[Z_{11}]$, $\omega\text{Im}[Z_{22}]$ and $\omega\text{Im}[Z_{12}]$ in order to determine the values of the inductances L_g, L_d and L_s, as shown in Figure 3.19. We may notice the high accuracy achieved by the linear regression with the de-embedded structure. Equations used to determine the values of the inductances were (3.22 – 3.24). Next, the inductances were de-embedded from the stripped structure to obtain the values of the resistances R_g, R_d, and R_s. Due to the incomplete de-embedding of the parameters of the GaN HEMT, nonlinearity occurred after de-embedding the inductances, while extracting the extrinsic series resistances. The reduction of such nonlinearity can be done by multiplying the stripped *Z*-parameters by ω^2. Hence, the intrinsic series resistances

were extracted through plotting $\omega^2\text{Re}[Z_{11}]$, $\omega^2\text{Re}[Z_{22}]$ and $\omega^2\text{Re}[Z_{12}]$ and using equations (3.25 – 3.27), as shown in Figure 3.20.

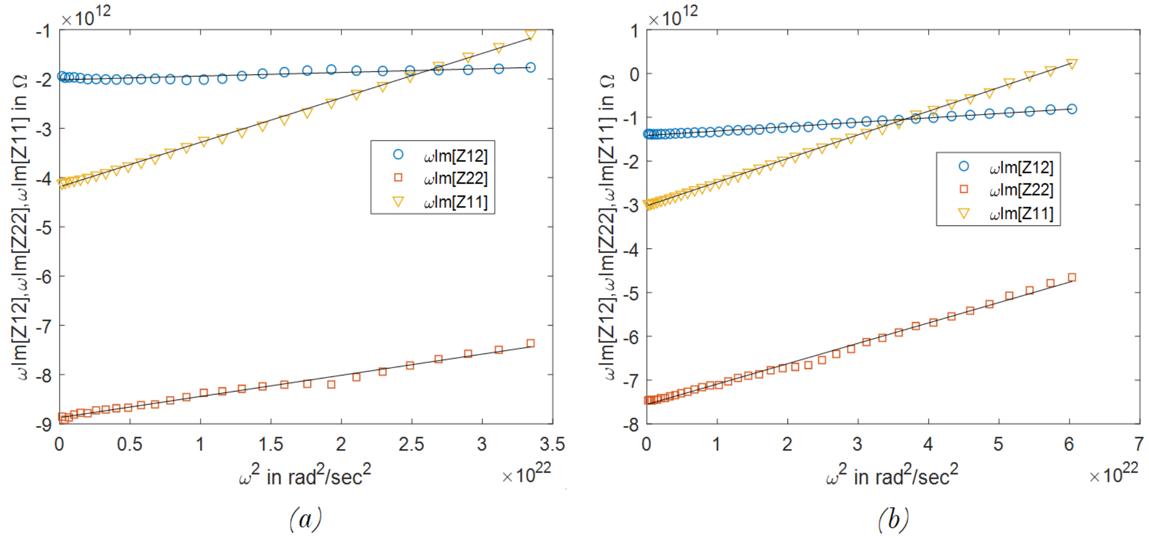

Figure 3.19 Extrinsic inductances extraction for (a) GaN/D and (b) GaN/SiC.

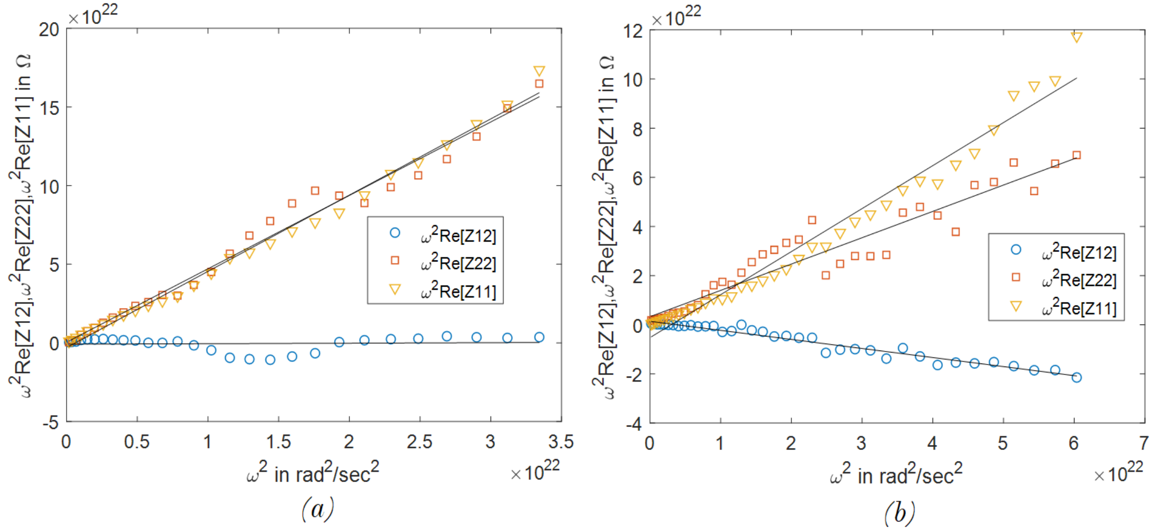

Figure 3.20 Extrinsic series resistances extraction for (a) GaN/D and (b) GaN/SiC.

The extrinsic networks were embedded together in order to compare the simulations and measurements, as shown in Figure 3.21. The extracted extrinsic parameters of GaN/D and GaN/SiC are shown in Table 3.1 and compared with the literature. From Table 3.1, we may see that during phase 1 for both devices, the substrate network was not

considered for simplification purposes and, hence, denoted (N/A). The values extracted from phase 1 for the intrinsic capacitances were then used in phase 2, with the substrate model included (as discussed in section 3.4). We may notice from the table that, after optimization, the extrinsic capacitances are very close to each other in both phase 1 ($C_{gp} \approx C_{dp}$) and phase 2 ($C_{gp} // C_{gg} \approx C_{dp} // C_{dd}$), provided R_{gg} and R_{dd} are extremely large. This was expected since the capacitances of the pad should be close to each other, as confirmed with literature results. Although the values of R_{gg} and R_{dd} are finite for GaN/D, they may be ignored due to their large values. However, their existence can be related to buffer-trapping effects, which will be discussed in Chapter 4. GaN/SiC showed divergent values for both R_{gg} and R_{dd} showing that the parasitic conduction is at minimal due to the reduced lattice mismatch between the GaN buffer, SiN nucleation layer, and SiC substrate.

For the extrinsic series resistances and inductances, R_g and R_d are very close to each other for both GaN/D and GaN/SiC in all phases and after optimization, showing equal metallization resistances, which is reasonable. L_g and L_d are not very far from each other for both GaN/D and GaN/SiC similar to previously extracted parameters in literature. R_s and L_s should be smaller in comparison to the other series resistances and inductances due to their feedback nature and small metallization effects [1].

We may notice the ratio of C_{gs} to C_{gd} is 3.2 and 4.2 for GaN/D and GaN/SiC, respectively, which successfully models the asymmetrical structure of both devices. Another point to address is the close values between C_{gd} and C_{ds} for both GaN/D and GaN/SiC. This may be attributed to the increased distance between the drain and the gate electrodes, causing the contribution of the gate to C_{gd} to be minimal compared to the drain electrode parasitics. In other words, C_{gd} and C_{ds} should have similar values associated with the drain electrode parasitics. This can be verified by looking at the extracted values in [28]-[30], where the extracted parameters of C_{gd} and C_{ds} were very close to each other for the case of asymmetrical devices.

The proposed extraction technique provided not only results with high accuracy but also reliable values for the extrinsic parameters that are related to the physics of the device. The extraction technique can be applied to different GaN HEMT devices with

different types of substrates, making it suitable for automating the extraction technique. Additional validations are presented in section 3.8 where the extrinsic parameters of GaN/Si and Graphene-based FET were extracted and compared with the literature.

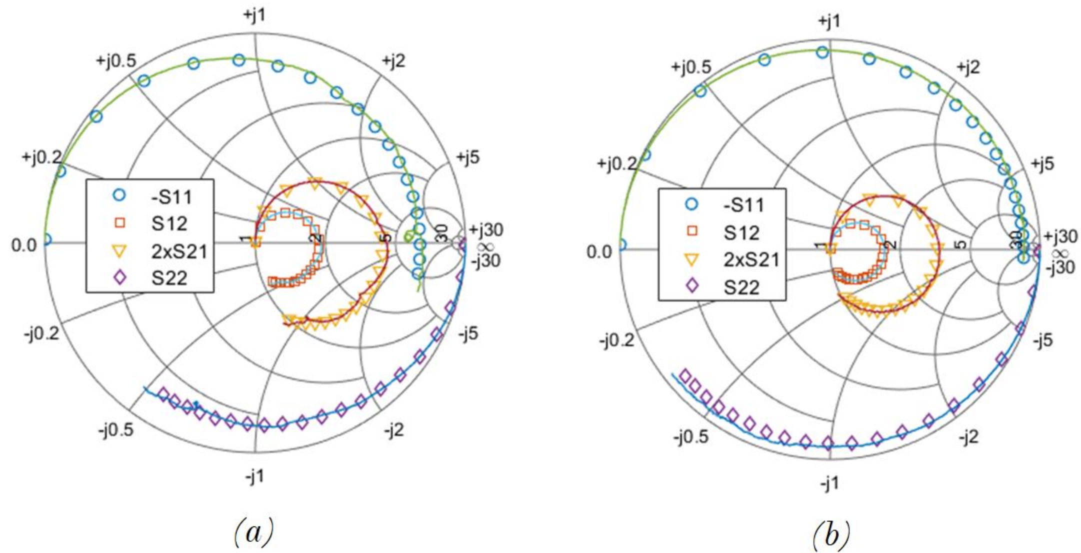

Figure 3.21 Comparison between measurements (lines) and optimized *S*-parameters simulations (symbols) for the extrinsic network of (a) GaN/D and (b) GaN/SiC for frequencies from 0.1 to 40 GHz.

3.7.2 Intrinsic parameters extraction results

Once the extrinsic parameters are de-embedded from the EC-SSM, we are left with the intrinsic circuit of the GaN HEMT. We then used equations (3.43 – 3.49) to extract all the parameters of the intrinsic GaN HEMT for both diamond and SiC substrates. The extraction procedure depends highly on the accuracy of the linear regression used to find the slopes of the curves. Figure 3.22 shows the curves needed to extract the intrinsic part of GaN/D and similarly for GaN/SiC in Figure 3.23. We may notice that the linear regression works well for C_{gs}, R_i, C_{gd}, R_{gd}, G_m, τ, C_{ds} and G_{ds} for GaN/SiC. However, for GaN/D, R_i and R_{gd} accuracy got affected by measurement errors discussed in subsection 2.4.4. Regardless, the accuracy of the model was not affected greatly by these measurement errors as will be seen later on when comparing the simulated *S*-parameters with measurements at different bias points.

Table 3.1 Extracted parameters for GaN/D and GaN/SiC under cold pinch-off condition (*: "N/A" implies the component is ignored in phase 1, "∞" implies simplification of the model from that of Figure 3.10 to Figure 3.11 and "–" implies result not recorded).

Model element	2x100 um GaN on Diamond				4x50 um GaN on SiC			
	Phase 1 values	***Phase 2 values***	***Optimized values***	***Ref [29] values***	***Phase 1 values***	***Phase 2 values***	***Optimized values***	***Ref [28] values***
C_{gp} (fF)	0	270	269.1	0.3	5.6	1	16.408	24.378
C_{dp} (fF)	0	126	109.42	0.37	6.9	7	4.5639	14.908
C_{gg} (fF)	N/A*	0.00432	11.024	∞*	N/A*	∞*	∞*	∞*
C_{dd} (fF)	N/A*	0	3.914	∞*	N/A*	∞*	∞*	∞*
C_{gs} (fF)	210.27	210.27	197.52	209.27	299.6	299.6	283.29	212.270
C_{gd} (fF)	59.70	59.70	61.52	59.70	67.77	67.77	67.94	60.39
C_{ds} (fF)	65.56	65.56	61.63	64.56	78.705	78.705	80.19	65.91
R_{gg} (kΩ)	N/A*	88.28	97.713	∞*	N/A*	∞*	∞*	∞*
R_{dd} (kΩ)	N/A*	142.46	144.18	∞*	N/A*	∞*	∞*	∞*
L_g (pH)	83.41	83.42	84.07	98.16	43.92	43.22	43.23	41.31
L_d (pH)	35.66	35.66	32.52	77.76	36.91	33.065	36.4	35.49
L_s (pH)	7.39	7.4	9.65	7.6	9.91	8.66	10	10.22
R_g (Ω)	4.87	4.87	4.68	4.88	1.7672	1.44	1.49	2.11
R_d (Ω)	4.76	4.76	4.72	4.72	1.0943	1.13	1.75	1.4
R_s (Ω)	0.06	0.06	0.08	0.03	0	0	0.018	0.36
ε	0.0202	0.0204	0.0162	-*	0.0173	0.0142	0.0104	-*

Since the large-signal model is dependent on the intrinsic parameters extracted at multiple bias points, we extracted the intrinsic parameters at 20 different bias points for GaN/D and at 63 different bias points for GaN/SiC. It is important to study each intrinsic element map in order to verify the extraction procedure, physics of the device, and potentially key insights.

Figure 3.24 shows a plot of C_{gs} at different bias points for both GaN/D and GaN/SiC. It can be noted that C_{gs} increases with V_{GS}. Below pinch-off point (≈ -3V), C_{gs} is constant and depends only on the width of the depletion region and hence the minimum capacitance value occurs. When V_{GS} reaches -3V, there will be a sudden increase in C_{gs} value due to the formation of 2DEG and the decrease in the depletion width. Any increase in the value of V_{GS} after that point increases C_{gs} by a small amount, indicating insensitive source edge-to-gate to depletion region. This observation is confirmed with subsection 2.3.2.

Figure 3.25 shows a plot of R_i for both GaN/D and GaN/SiC. R_i is the resistance associated with charging and discharging the depletion region in the gate-to-source side, R_i is equal to the ratio of the potential drop in that part of the channel and the current; since the current decreases with V_{DS} due to increase in self-heating and charge trapping effects, R_i increases [3].

For both G_{gsf} and G_{gdf}, we have not gotten important insights from their distribution because of the nature of the gate-to-source and gate-to-drain Schottky diodes within the device. Forward and breakdown conductions of parasitic Schottky diodes occur at high gate voltage (V_{GS} > 1.5V) and hence for operation below the V_{GS} value of 0V, G_{gsf} and G_{gdf} can be neglected due to their very small values [3]. Figure 3.26 and Figure 3.27 show the distribution of both G_{gsf} and G_{gdf} for both devices, respectively.

Figure 3.28 shows C_{gd} distribution for both GaN/D and GaN/SiC. C_{gd} increases with increasing V_{GS}, but decreases with increasing V_{DS}. The electric field has a peak value at the drain end and decreases along the gate-to-drain length in the saturation region, which leads to a drop in charge. As V_{DS} increases, the peak electric field point will be shifted along the space between the drain and the source, causing a reduction in the channel

charge and, hence, C_{gd} decreases. These observations are confirmed with subsection 2.3.2. Since the charge distribution is uniform in the ohmic region and channel is not pinched off at the drain side, C_{gd} increases dramatically with high V_{GS} and low V_{DS}.

R_{gd} represents the charging and discharging of the depletion layer underneath the gate-to-drain region. Since the depletion region is slightly dependent on V_{DS}, R_{gd} should not change dramatically with V_{DS}. R_{gd} should have the same characteristics with V_{GS} as in R_i. We may notice the difference between GaN/D and GaN/SiC in Figure 3.29 due to measurement errors [3].

The G_m plot is shown in Figure 3.30. G_m is highly dependent on the channel charge density and the electron velocity [3]. The sharp increase in G_m close to the pinch-off point is due to the linearity between the high mobility of GaN HEMT and the low electric field by the gate voltage. We can also notice from the plot the linear relationship between the G_m and V_{DS} at the ohmic region. When V_{GS} is increased greatly, the electric field increases and the mobility of electrons saturates, causing G_m to become constant with V_{GS} [3].

τ is the transit time of electrons to cross the channel. τ is expected to increase as we increase the drain voltage due to mobility degradation and velocity saturation, as shown in Figure 3.31. It should also increase with increasing gate-to-source voltage due to the vertical electric field that causes mobility degradation [3].

Because the drain electrode is widely spaced from the gate electrode in an asymmetrical device, C_{ds} should be very similar to C_{gd} distribution as shown in Figure 3.32. The only difference is that C_{ds} is constant in the saturation region due to its electric field linkage between the drain and the source electrodes [3]. Due to drain-to-source channel length modulation, we expect G_{ds} to decrease as V_{DS} increases. As expected, we may observe also very small values for G_{ds} when the device is in the saturation region. When the device enters the ohmic region, G_{ds} increases dramatically to take into consideration the increase in the current values caused by the reduction of the depletion layer. A plot of G_{ds} at different bias points is shown in Figure 3.33.

Equations (3.5) and (3.11) were used to plot f_t and f_{max} for both devices as shown in Figures 3.34 and 3.35, respectively. f_t and f_{max} plots should be somewhat similar in shape to G_m plot and that is the case for the utilized equations. We may notice that f_t and f_{max} are nearly constant with V_{DS}, a major advantage when dealing with GaN HEMT devices. A recorded maximum f_t for a 250 um GaN/D was 27.4 GHz [31], which is very close to our maximum f_t = 29.2 GHz for 200 um GaN/D. Figure 3.36 shows the calculated error using (3.28). We may notice that the minimum error occurs around the pinch-off point for both devices. This is because the extrinsic parameters extraction technique is based on cold pinch-off *S*-parameters measurements; hence, high accuracy should be expected in this region. We may also notice the high accuracy for both devices in the saturation region. The error spikes up when the device is on with V_{DS} = 0 (around the cold-forward condition). This error could be attributed to the usage of cold-pinch off *S*-parameters measurements only to extract the extrinsic parameters of GaN HEMT. Possible improvements could be achieved by using cold-forward *S*-parameters measurements to simulate the *S*-parameters in the linear region since they occur around the same bias point. Extraction using cold-forward measurements was avoided to simplify the extraction automation process. However, this error would not greatly affect devices operating in the saturation region.

Since we obtained the extrinsic and the multi-bias intrinsic parameters, we embedded all the parameters together to build the overall EC-SSM. We then compared simulated *S*-parameters with measurements, as shown in Figure 3.37. The Figure shows high accuracy with measurements across multiple bias points for both devices.

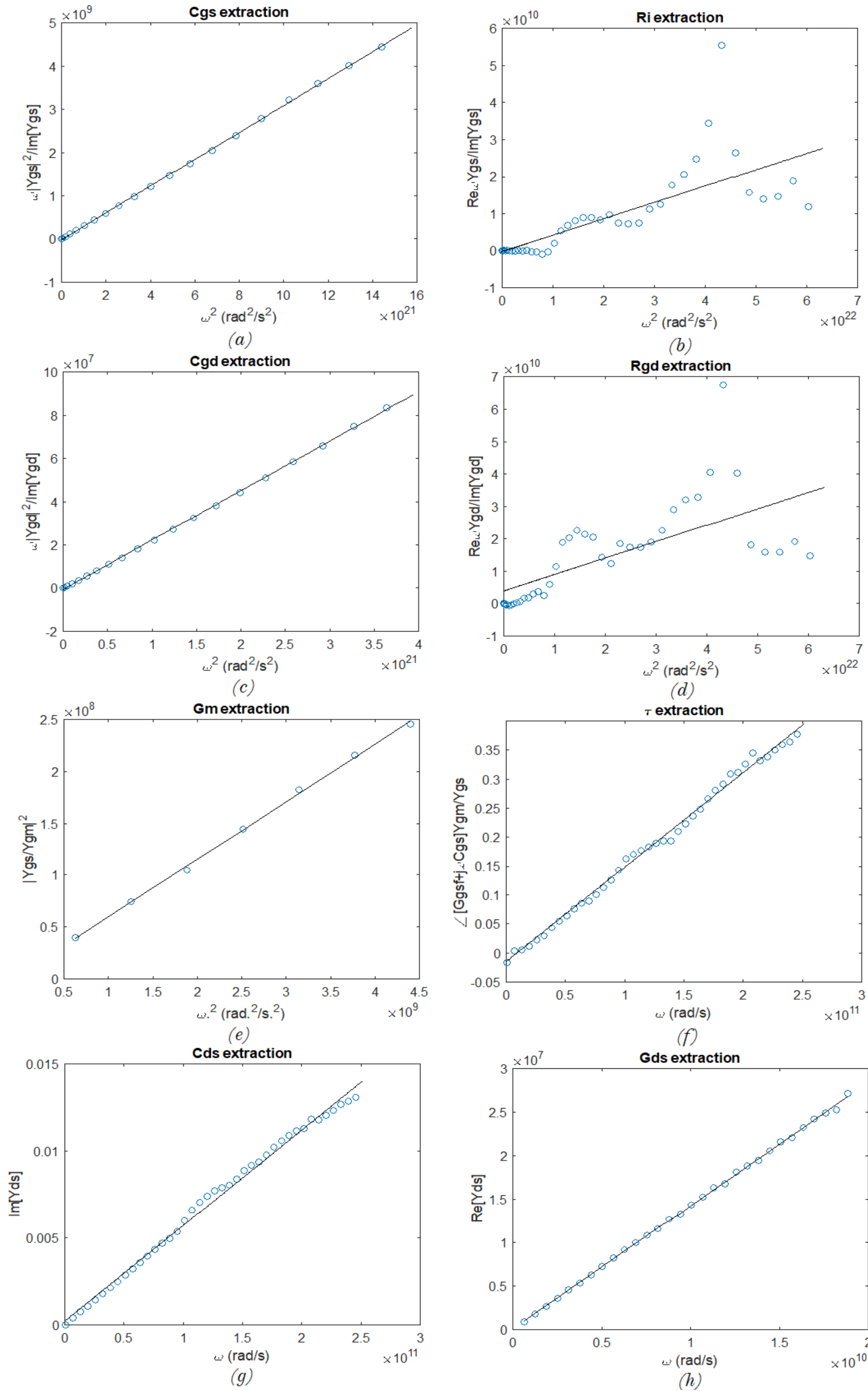

Figure 3.22 Intrinsic parameters extraction using linear regression for GaN/D at V_{GS} = -2 V and V_{DS} = 20 V showing (a) C_{gs}, (b) R_i, (c) C_{gd}, (d) R_{gd}, (e) G_m, (f) τ, (g) C_{ds} and (h) G_{ds} extraction.

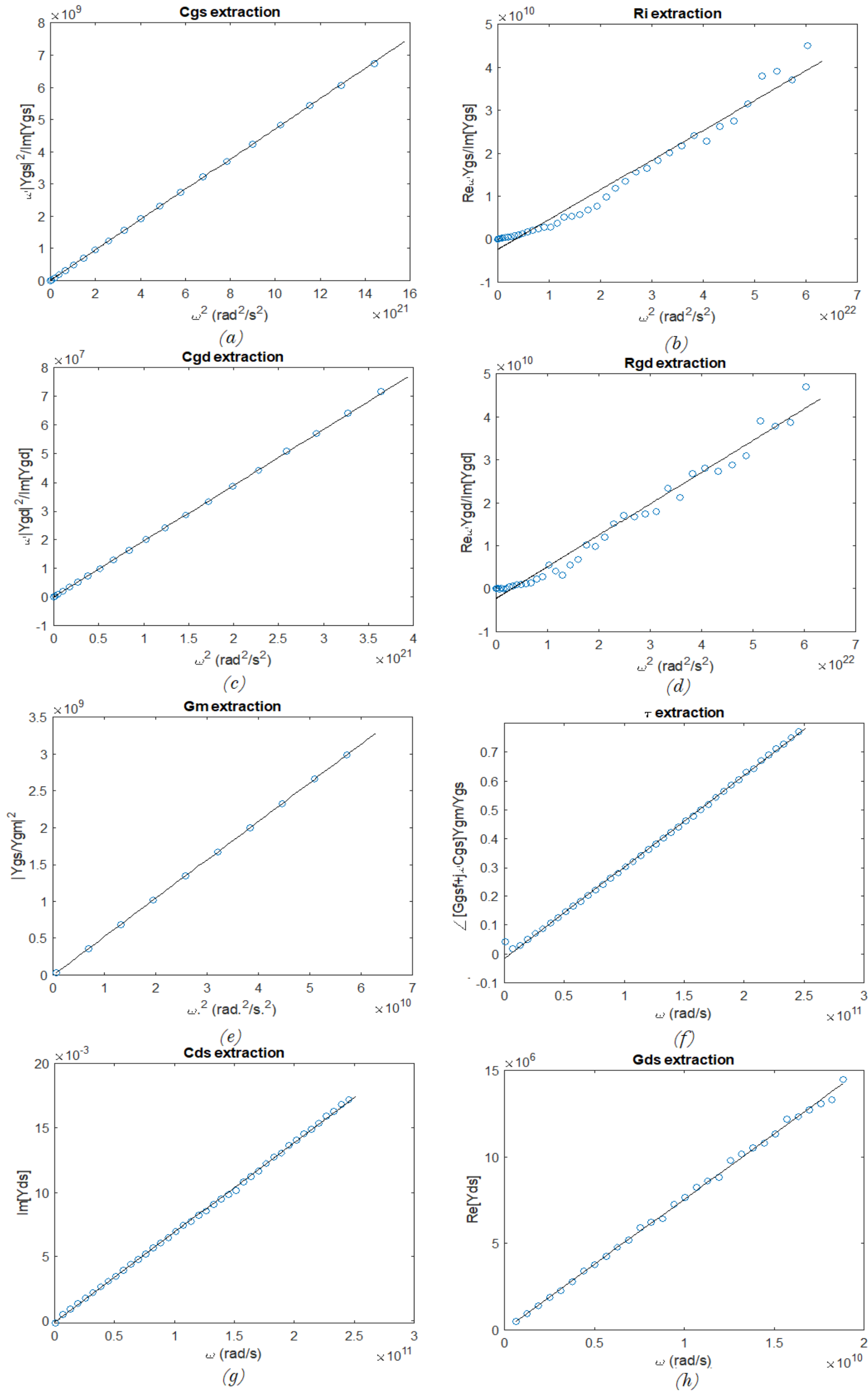

Figure 3.23 Intrinsic parameters extraction using linear regression for GaN/SiC at V_{GS} = -1 V and V_{DS} = 30 V showing (a) C_{gs}, (b) R_i, (c) C_{gd}, (d) R_{gd}, (e) G_m, (f) τ, (g) C_{ds} and (h) G_{ds} extraction.

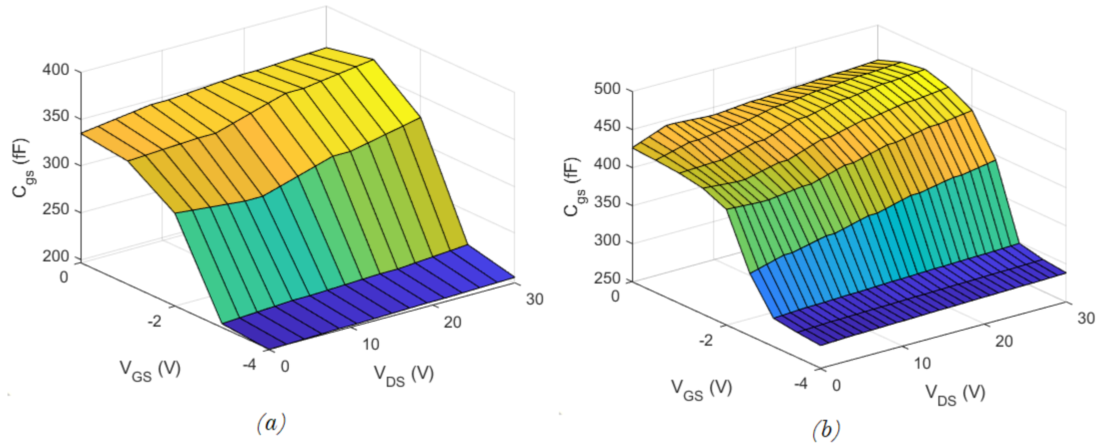

Figure 3.24 C_{gs} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

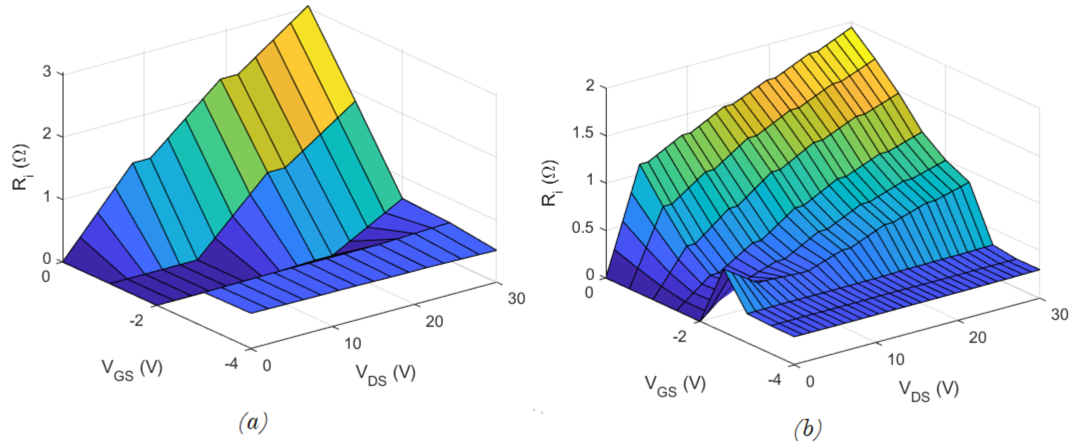

Figure 3.25 R_i at multiple bias points for (a) GaN/D and (b) GaN/SiC.

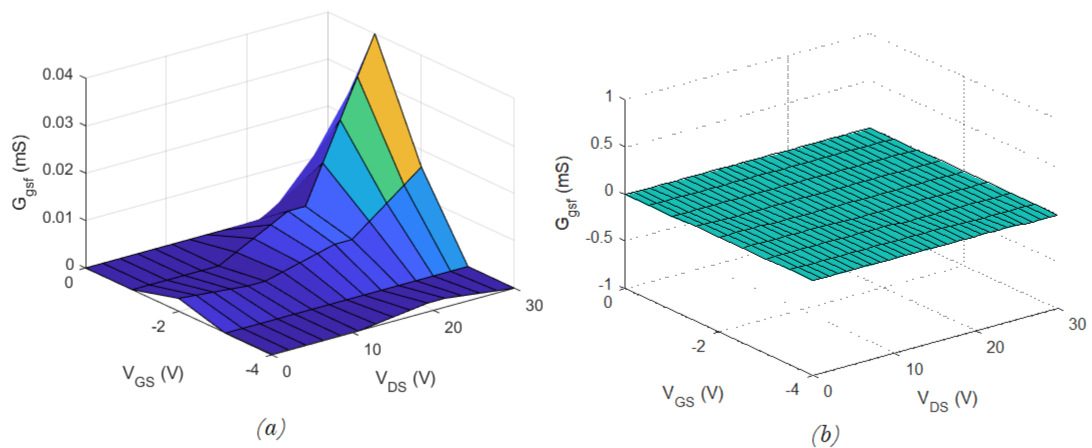

Figure 3.26 G_{gsf} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

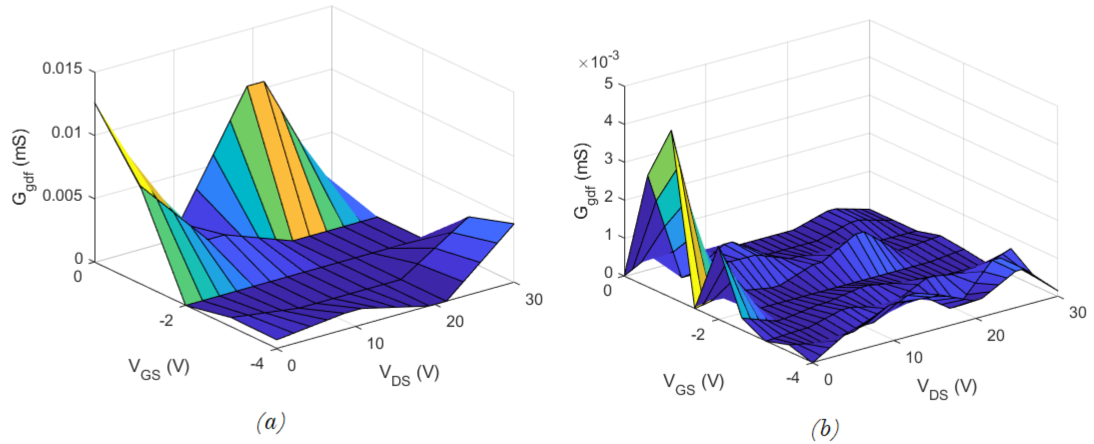

Figure 3.27 G_{gdf} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

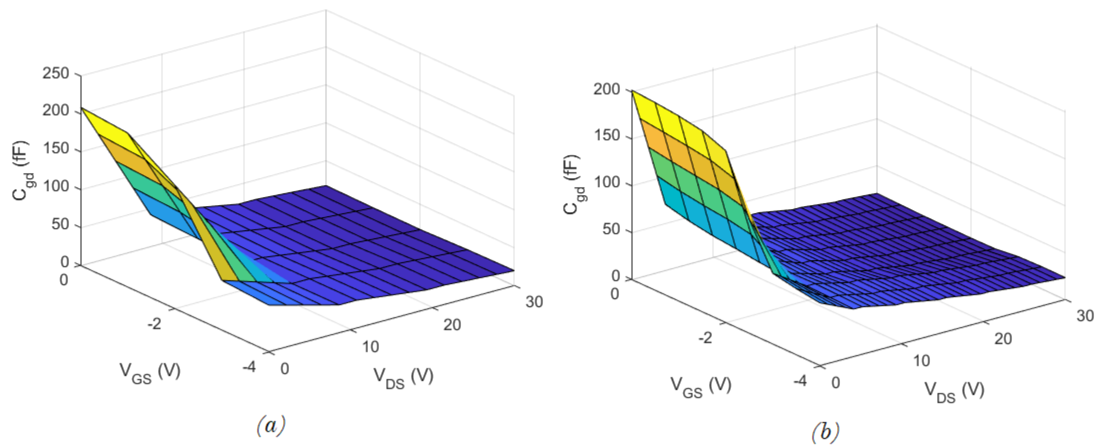

Figure 3.28 C_{gd} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

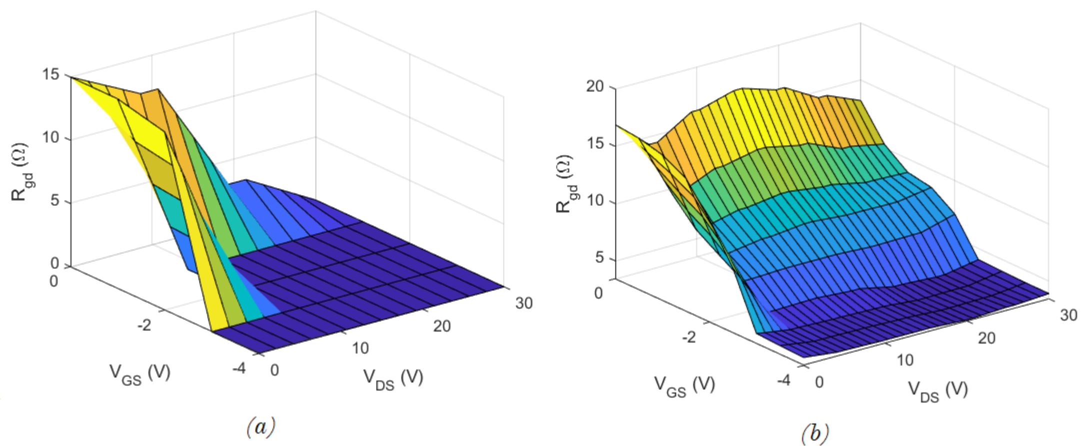

Figure 3.29 R_{gd} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

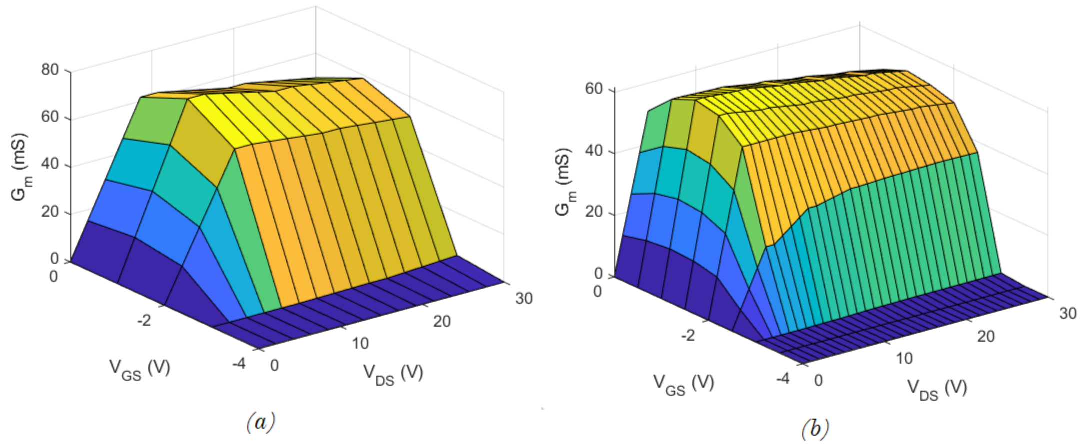

Figure 3.30 G_m at multiple bias points for (a) GaN/D and (b) GaN/SiC.

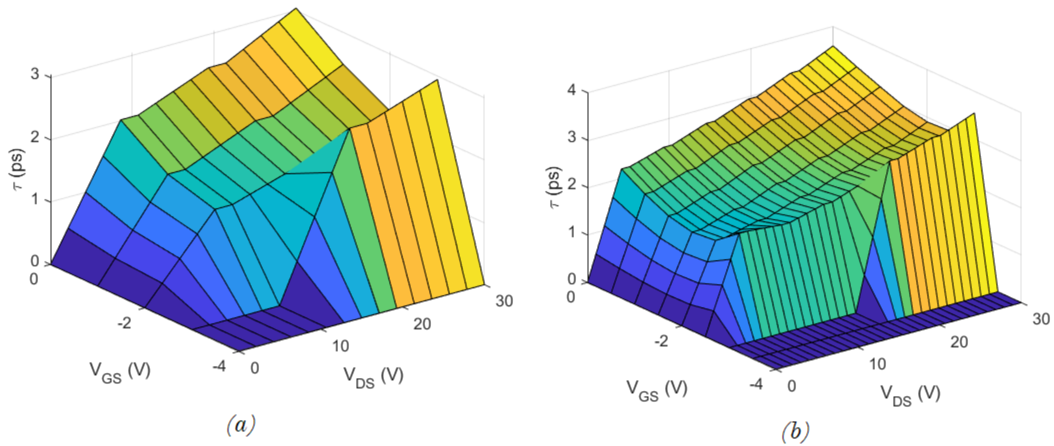

Figure 3.31 τ at multiple bias points for (a) GaN/D and (b) GaN/SiC.

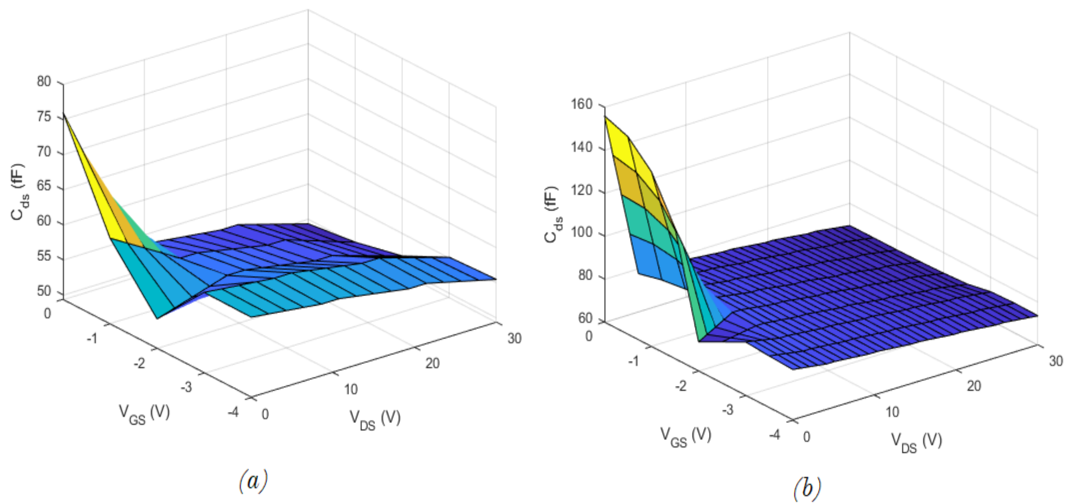

Figure 3.32 C_{ds} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

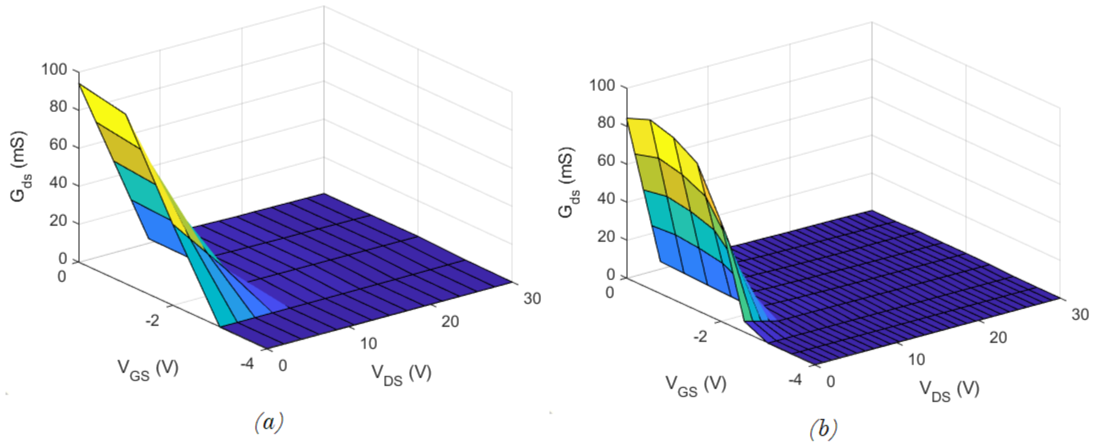

Figure 3.33 G_{ds} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

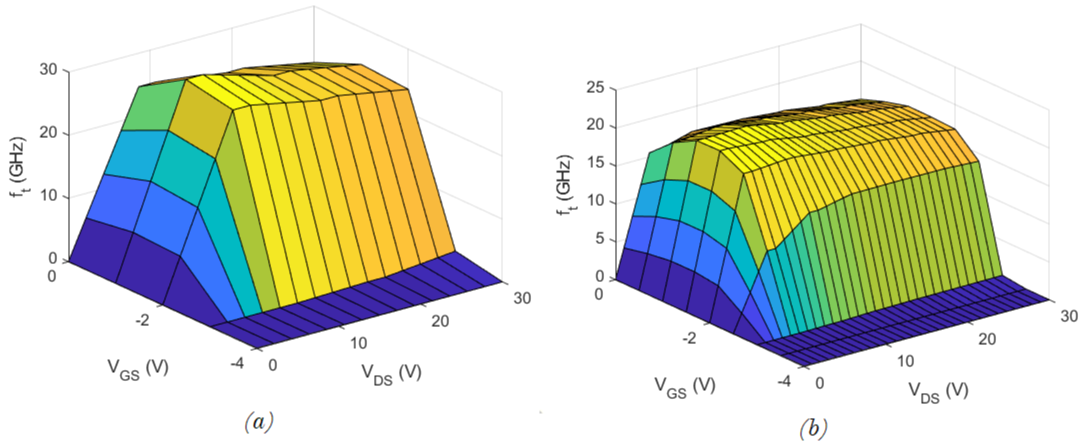

Figure 3.34 f_t at multiple bias points for (a) GaN/D and (b) GaN/SiC.

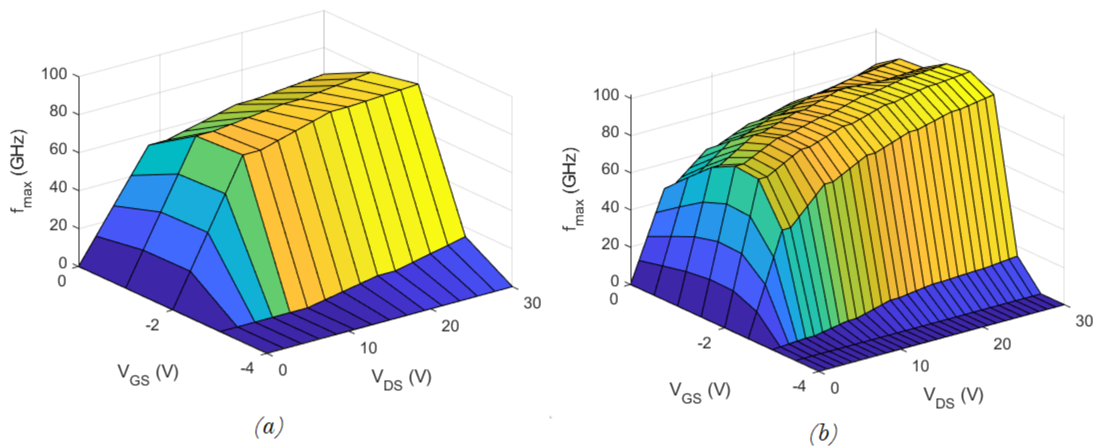

Figure 3.35 f_{max} at multiple bias points for (a) GaN/D and (b) GaN/SiC.

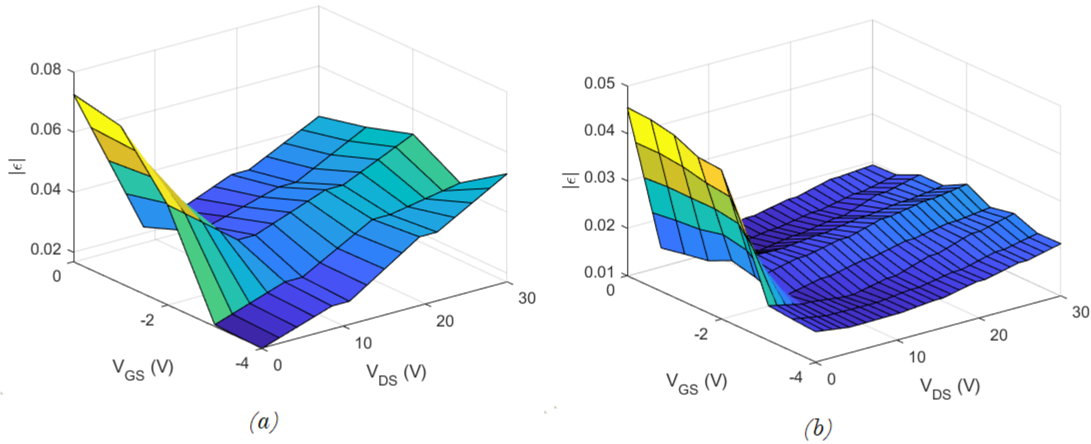

Figure 3.36 |ε| at multiple bias points for (a) GaN/D and (b) GaN/SiC.

3.8 Additional model validations

In order to validate our extraction technique, we tested it on two devices that exhibit different characteristics than the previously studied GaN HEMTs. The first device is a symmetrical 2x200 um GaN/Si [6] and the second a Graphene-Based FET [32], where the *S*-parameters measurements for both devices were obtained from technical literature.

3.8.1 GaN HEMT on Silicon substrate

GaN/Si devices exhibit moderate substrate resistivity and lattice mismatch with the GaN buffer. This leads to tremendous parasitic conduction through the substrate at lower frequencies and hence, we expect the values of R_{gg} and R_{dd} to be significantly smaller than that of GaN/D [6].

Starting from phase 1, we can get the scanned values of C_{gp} and C_{dp} that will determine the reliable values of C_{gs} and C_{ds} for such device. The scanned values are shown in Figure 3.38, highlighting the minimum error point. From our knowledge of GaN/Si, we know that such a device will exhibit parasitic conduction through the substrate. Phase 1 has R_{gg} and R_{dd} removed for simplicity and hence such effect cannot be modeled. Figure 3.39 shows how the removal of the substrate model affects the accuracy of the extraction, which is solved during phase 2 of the extraction technique.

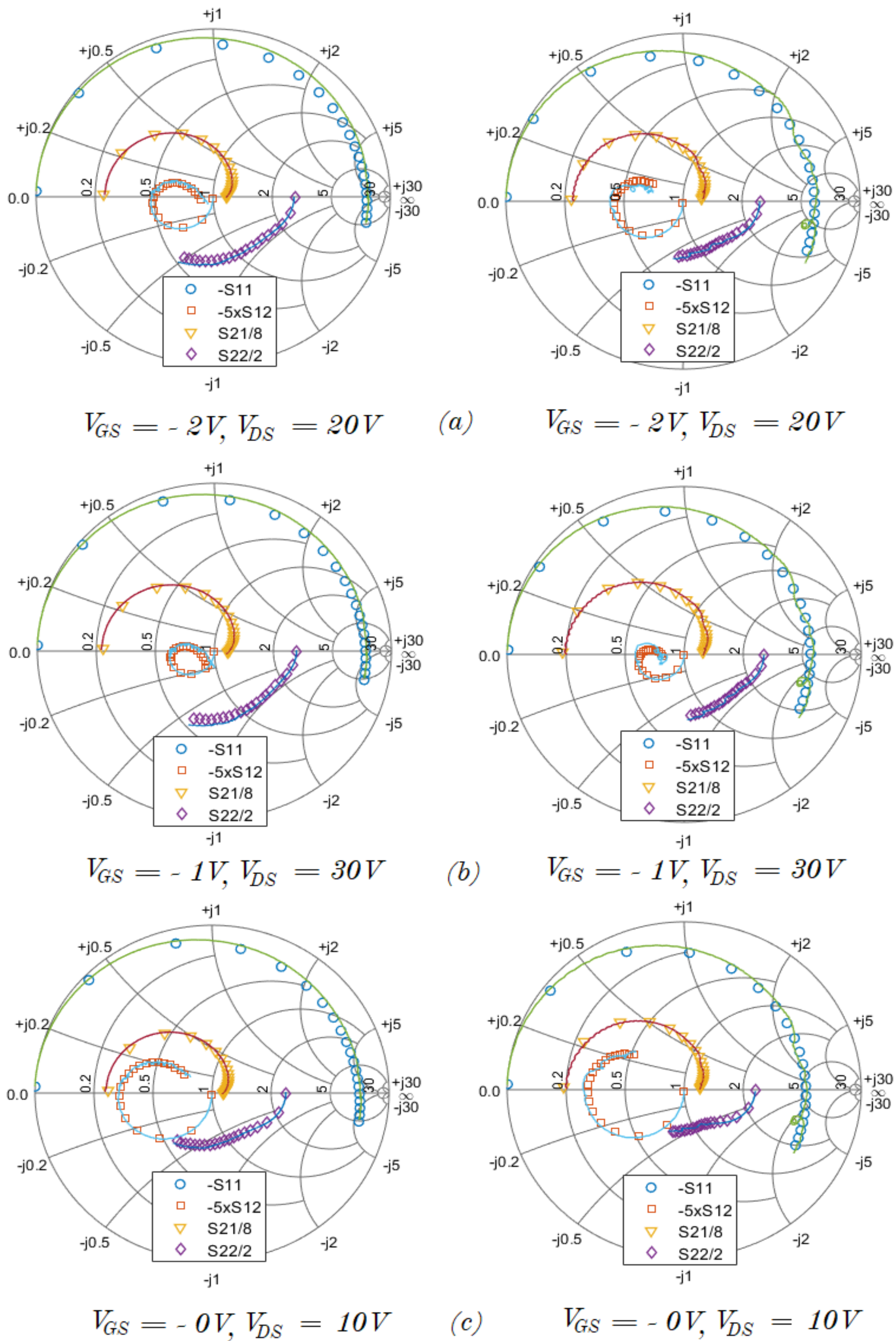

Figure 3.37 *S*-parameter measurements (lines) and simulations (symbols) for GaN/D (left charts) and GaN/SiC (right chart) at frequencies ranging from 0.1 GHz to 40 GHz at bias points of: (a) V_{GS} = -2V and V_{DS} = 20V, (b) V_{GS} = -1V and V_{DS} = 30V, and (c) V_{GS} = -0V and V_{DS} = 10V.

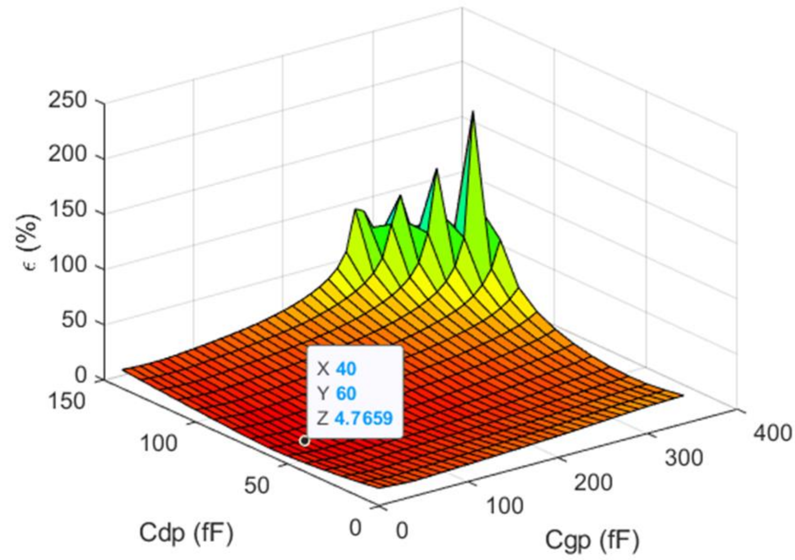

Figure 3.38 C_{gp} and C_{dp} scan for GaN/Si during phase 1.

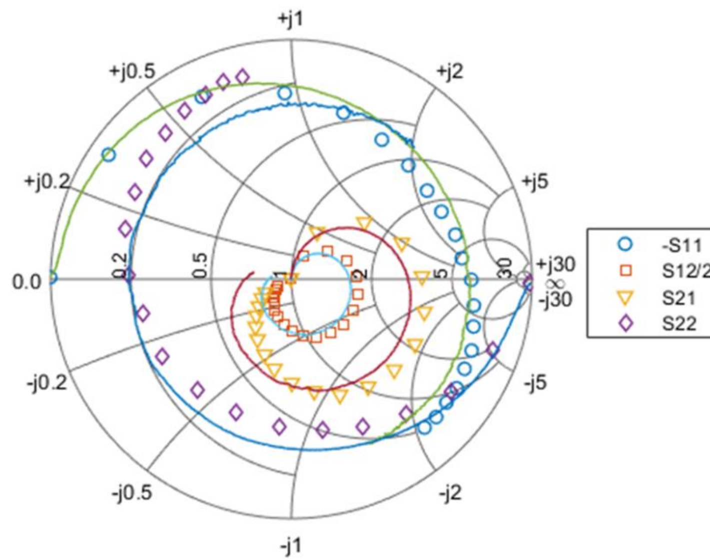

Figure 3.39 Inaccurate extraction due to the need of a substrate model for GaN/Si.

After extracting reliable values for C_{gs} and C_{ds}, we can start phase 2 that re-includes the substrate model (R_{gg}, R_{dd}, C_{gg} and C_{dd}). We have scanned the values of C_{gp} and C_{dp} in order to find the minimal error (Figure 3.40).

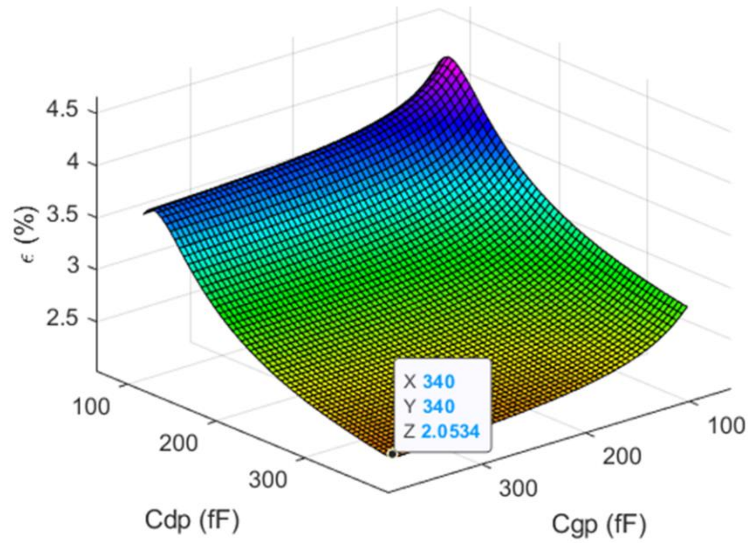

Figure 3.40 C_{gp} and C_{dp} scan for GaN/Si during phase 2.

In phase 2, we can extract all the remaining extrinsic parameters as we have shown in section 3.4. Figure 3.41 is used to extract the pad capacitances and the substrate parameters, Figure 3.42 shows the extracted series inductances and Figure 3.43 shows the extracted series resistances. We can also see the high accuracy of the linear regression technique in extracting such parameters. Figure 3.44 shows the convergence of GWO used for fine-tuning the extracted parameters. High convergence and low chances of encountering local minima is achieved by the initial values extracted by phase 2.

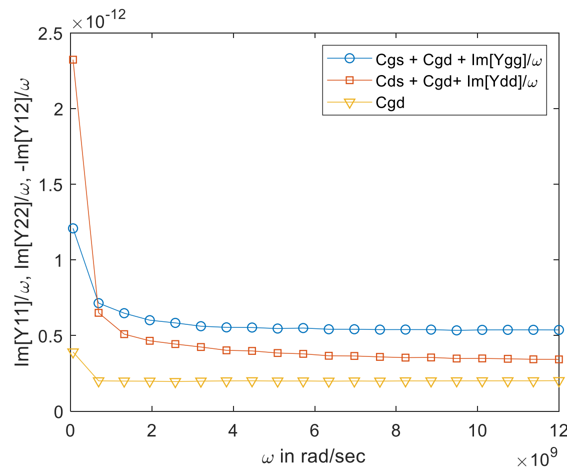

Figure 3.41 Plot for extracting the pad capacitances and the substrate parameters of GaN/Si.

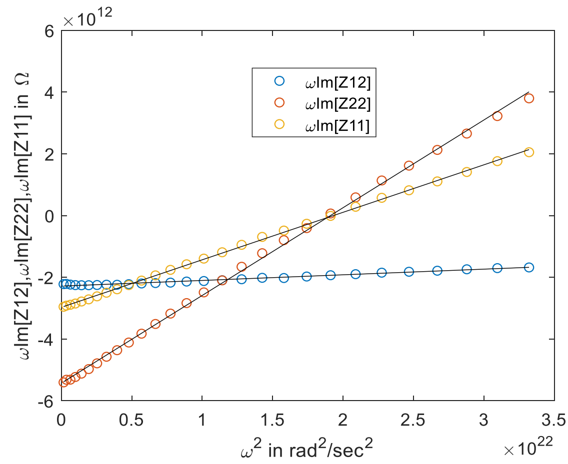

Figure 3.42 Extracted series inductances of GaN/Si

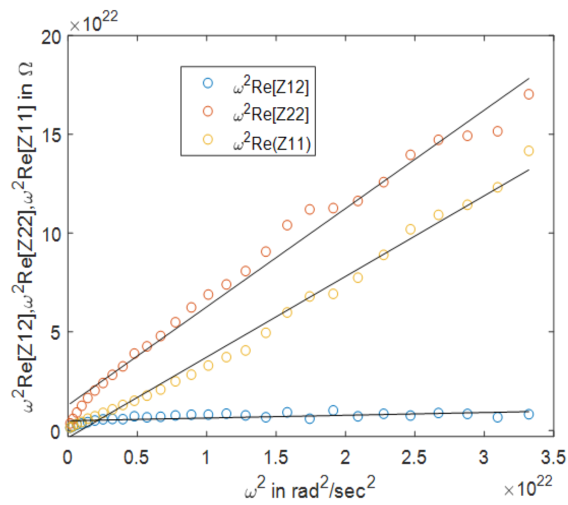

Figure 3.43 Extracted series resistances of GaN/Si.

The optimized values are used to simulate the *S*-parameters of the EC-SSM. Figure 3.45 shows the extrinsic *S*-parameters simulations, highlighting a great improvement in accuracy compared to the previously simulated *S*-parameters shown in Figure 3.39. This is mainly due to the inclusion of an accurate substrate model in phase 2. Table 3.2 shows all the extracted extrinsic parameters of GaN/Si during all phases and after running the optimization technique. We can notice very similar results obtained after the second phase, the optimized values, and the data reported in [6].

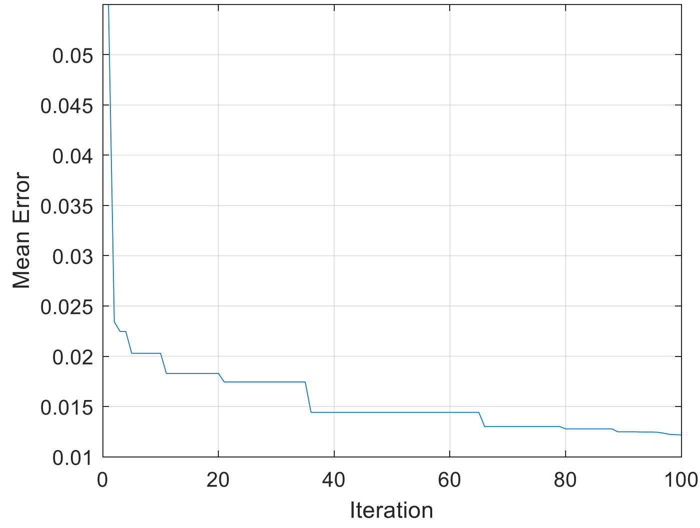

Figure 3.44 Convergence of GWO during the optimization of GaN/Si parameters.

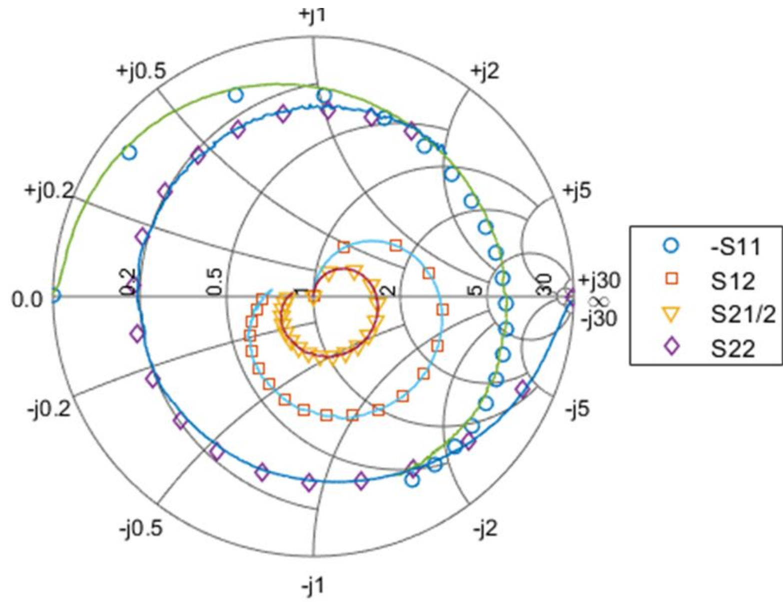

Figure 3.45 Optimized *S*-parameters simulations (symbols) and measurements (lines) for GaN/Si at frequencies from 0.1 GHz to 40 GHz under cold pinch-off condition.

Table 3.2 Extracted extrinsic parameters of 2x200 um GaN/Si (*: "N/A" means elements not involved in phase 1 and "-" means data not available in the reference).

Model element	**GaN on Si**			
	Phase 1 values	***Phase 2 values***	***Optimized values***	***Ref [6] values***
C_{gp} *(fF)*	41	340	332.70	340
C_{dp} *(fF)*	58	340	321.75	340
C_{gg} *(fF)*	N/A*	46.62	39.326	96
C_{dd} *(fF)*	N/A*	69.93	51.276	96
C_{gs} *(fF)*	292.49	292.49	293.68	260
C_{gd} *(fF)*	200.77	200.77	205.82	200
C_{ds} *(fF)*	89.52	89.52	70	48
R_{gg} *(kΩ)*	N/A*	2.03	1.11	1.49
R_{dd} *(kΩ)*	N/A*	0.83	0.71	0.82
L_g *(pH)*	128.48	134.95	140	145.8
L_d *(pH)*	241.22	264.73	270	293.3
L_s *(pH)*	17.12	18.53	12.42	18.9
R_g *(Ω)*	4.29	3.95	3.47	2.91
R_d *(Ω)*	4.12	4.728	5	7.93
R_s *(Ω)*	0.56	0.11	0.27	2.9
ε	0.048	0.066	0.012	-*

3.8.2 Graphene-Based FET

In order to further test-bench the capability of our proposed extrinsic parameters extraction technique, we applied it on a completely different device, i.e., a Graphene-based FET. Graphene is a two-dimensional single layer of crystalline allotrope of carbon [33]. It has hybridized carbon atoms connected together to form extended benzene ring structure [33]. As a result, Graphene exhibits high electron mobility and large saturation velocity, suitable for RF applications [32].

The main difference between Graphene-based FET and GaN/Si is that the first does not exhibit high parasitic conduction through the substrate, and hence we expect high accuracy from phase 1 [32]. During phase 1, we scanned the values of C_{gp} and C_{dp} in order to determine the minimal error, as shown in Figure 3.46.

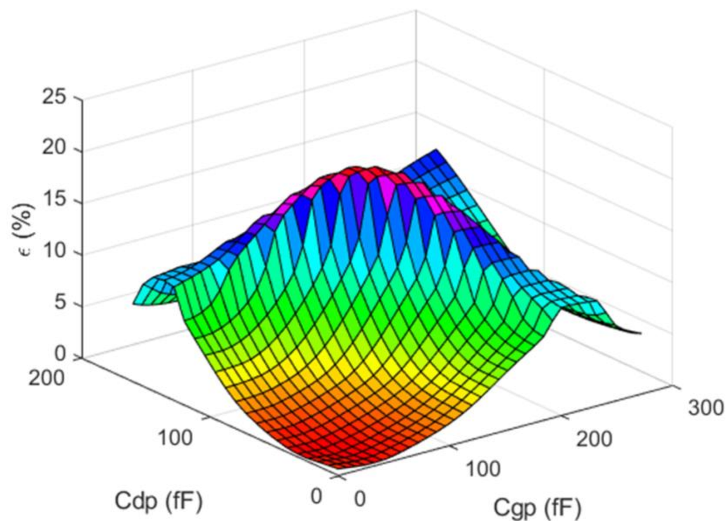

Figure 3.46 C_{gp} and C_{dp} scan for Graphene-Based FET.

During the second phase, R_{gg} and R_{dd} values diverged dramatically from the linear slope and hence their contribution was minimal and can be ignored. It can also be shown from Figure 3.47 that the plotted curves are almost independent of frequency (low/intermediate frequency ranges). Series inductances and series resistances are extracted using Figures 3.48 and 3.49, respectively. As was shown for GaN/Si, the GWO

achieves high convergence rate when optimizing the extrinsic parameters, as shown in Figure 3.50.

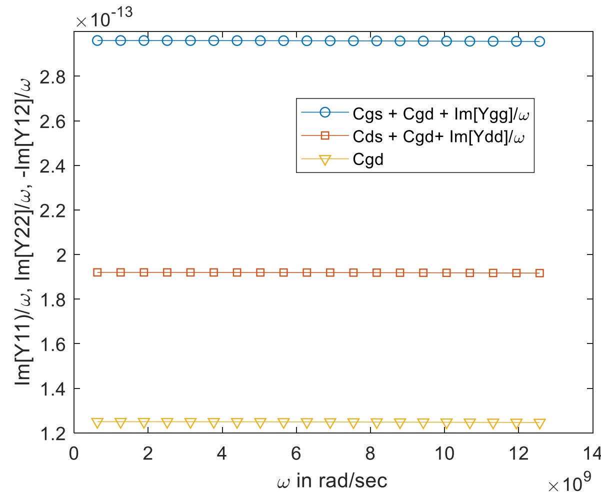

Figure 3.47 Pad capacitances and substrate parameters extraction for Graphene-Based FET.

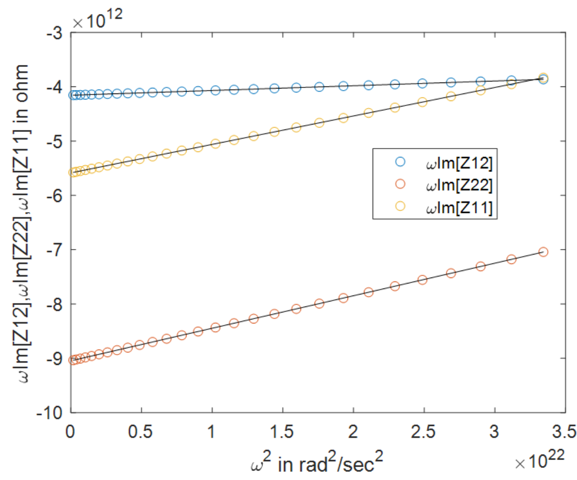

Figure 3.48 Extrinsic series inductances extraction for Graphene-Based FET.

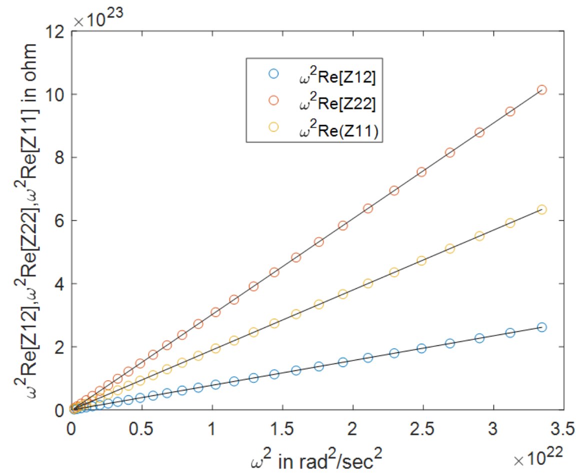

Figure 3.49 Extrinsic series resistances extraction for Graphene-Based FET.

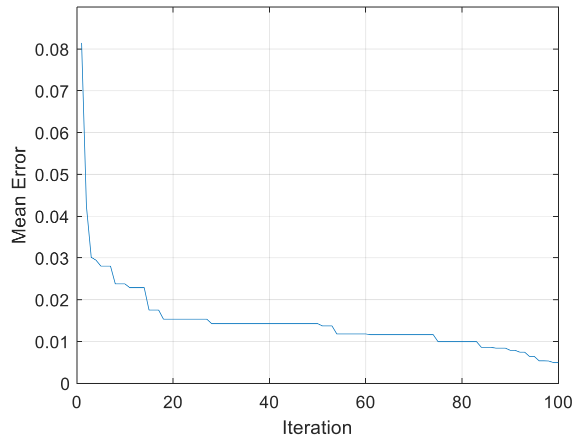

Figure 3.50 Error convergence using GWO for optimizing the extracted parameters of Graphene-Based FET.

The optimized extrinsic parameters are embedded together to simulate the *S*-parameters and compare them with the measured ones. As can be seen from Figure 3.51, high accuracy is achieved even without the need of a substrate model. Table 3.3 also shows very close values between our extraction technique and the extraction technique from [32].

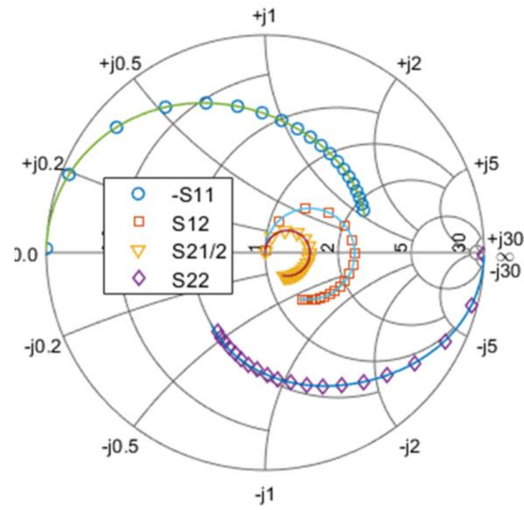

Figure 3.51 Optimized *S*-parameters simulations (symbols) and measurements (lines) for the Graphene-Based FET at frequencies from 0.1 GHz to 40 GHz under cold pinch-off condition.

Table 3.3 Extracted extrinsic parameters of Graphene-Based FET (*: "N/A" means elements not present during phase 1, "-" means data was not given in literature, "∞" implies neglected components and hence the circuit can be simplified from Figure 3.10 to 3.11).

Model element	**Graphene Based-FET**			
	Phase I values	***Phase II values***	***Optimized values***	***Ref [32] values***
C_{gp} *(fF)*	24	290	305.73	23
C_{dp} *(fF)*	24	190	170.47	25
C_{gg} *(fF)*	N/A*	26.17	39.326	N/A*
C_{dd} *(fF)*	N/A*	27.47	51.276	N/A*
C_{gs} *(fF)*	147	147	150.31	148
C_{gd} *(fF)*	124.78	124.78	124.94	125
C_{ds} *(fF)*	43.01	43.01	38.13	42
R_{gg} *(kΩ)*	N/A*	∞*	∞*	N/A*
R_{dd} *(kΩ)*	N/A*	∞*	∞*	N/A*
L_g *(pH)*	43.68	43.68	41.91	42.8
L_d *(pH)*	51.17	51.17	57.65	52.8
L_s *(pH)*	8.74	8.75	6.55	8.9
R_g *(Ω)*	11.16	11.16	9.89	11
R_d *(Ω)*	22.49	22.49	25.24	22.8
R_s *(Ω)*	7.83	7.83	9.16	7.9
ε	0.0056	0.0056	0.005	-*

3.9 Conclusion

In this chapter, the small-signal model and the proposed extraction technique were presented. The EC-SSM is composed of an intrinsic part and an extrinsic part. The intrinsic part usually has a general topology while the extrinsic part can have different topologies depending on the size of the device and its parasitic conduction phenomena. Each extrinsic network differs in terms of complexity, extraction techniques, assumptions, and the parasitics they model. RF performance metrics namely, the unity current-gain and the unity power-gain cutoff frequencies were derived. Different extrinsic network extraction techniques were presented. The first uses the open, short, and thru test structures to estimate the values of the extrinsic part of GaN HEMT. The second uses cold-pinch off *S*-parameters measurements with or without the cold-forward *S*-parameters measurements. The former extraction technique may have high accuracy but is costly, while the latter is less complicated and easy to automate. The proposed extraction technique was applied to a single EC-SSM and was developed to take into account the different substrates of GaN HEMT described in the previous chapter. By avoiding using multiple extraction approaches for multiple EC-SSMs, it allows the automation of such a technique. Another advantage is that it takes into consideration the asymmetrical structure of GaN HEMT, passivation layer deposition, and buffer-traps and their effects on the intrinsic capacitances as well as parasitic conduction through the substrate.

The proposed extraction technique involves two phases. Phase 1 is concerned with finding reliable values of C_{gs} and C_{ds} while neglecting the substrate network for simplification purposes. The second phase is related to the extraction of the substrate network. Grey Wolf Optimizer was used to fine-tune the extracted parameters due to its high accuracy and high convergence rate. The intrinsic parameters were extracted as well for both GaN/D and GaN/SiC. The extrinsic extraction techniques were applied to four different devices (2x100 um GaN/D, 4x50 um GaN/SiC, 2x200 um GaN/Si, and Graphene based-FET). High accuracy was achieved for all devices by simulating the *S*-parameters and comparing them with measurements. It was shown that for GaN/D, the parasitic conduction is very small, which in turn, might indicate possible buffer-trapping effects. GaN/SiC showed excellent lattice matching between the GaN buffer and the SiC

substrate. GaN/Si showed high parasitic conduction at lower frequencies, as expected. The extraction technique was able to model efficiently both symmetrical and asymmetrical GaN HEMT structures with the passivation layer and buffer-traps effects. The results from the intrinsic parameter extraction were validated by plotting all the intrinsic components at multiple V_{GS} and V_{DS}, and comparing our insights with technical literature for both GaN/D and GaN/SiC.

Since that, we extracted and validated the extrinsic parameters and the intrinsic parameters at multiple bias points for both GaN/D and GaN/SiC. We can now move to the large-signal modeling in order to model the non-linear drain current of the device with its dispersive effects.

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Chapter 4: Large-Signal Modeling

Small-signal models can accurately predict the parasitics of the device. However, they cannot model the nonlinear characteristics of the drain current and its dispersive effects. A large-signal model can, in fact, help to predict and model the isothermal trapping-free current and the dispersive effects such as charge-trapping and self-heating effects. In this chapter, we will be showing the topologies and the techniques used to model the large-signal characteristics of the device. After determining the topology, the isothermal trapping-free drain current will be analytically calculated using the Quasi-Physical Zone Division modeling technique. Finally, fitting parameters will be used to empirically model the self-heating and charge-trapping effects of both GaN/D and GaN/SiC. The results will be discussed based on these fitting parameters.

4.1 Large-signal model topologies

In this section, we will be discussing the different topologies used to model the large-signal characteristics of GaN HEMT. The first model, the quasi-static, is the simplest EC-LSM that is based solely on the intrinsic parameters extracted at multiple bias points during the small-signal modeling technique; the second topology is similar to the first topology but takes into account the quadratic frequency dependency of Y-parameters and the time delay of the electrons to pass the channel. The last topology is the proposed one.

4.1.1 Quasi-Static Large-signal topology

In this topology, the dynamic characteristics of GaN HEMT are derived from the static behavior of the device; hence the intrinsic elements are voltage-dependent only [1]. The static behavior of the device means that any time related component in the EC-SSM should be neglected. We can write Y-parameters representation of the intrinsic EC-SSM in Figure 3.2 as follows [2]:

$$Y = \begin{bmatrix} G_{gsf} + G_{gdf} + j\omega(C_{gs} + C_{gd}) & -G_{gdf} - j\omega C_{gd} \\ G_m - G_{gdf} - j\omega C_{gd} & G_{ds} + G_{gdf} + j\omega(C_{ds} + C_{gd}) \end{bmatrix} \tag{4.1}$$

where R_i, R_{gd} and τ are neglected due to their time constants contribution. We may notice that the representation in (4.1) can be split into real parts related to the conductances and

imaginary parts related to the intrinsic capacitances. Hence by integrating the real parts of the *Y*-parameters and integrating the intrinsic capacitances along the appropriate voltages, we can get lumped currents ($dI=GdV$), and charge components ($dQ=CdV$). The relations are calculated as follows [2]:

$$I_g(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} [G_{gsf}(V_{gs},V_{ds}) + G_{gdf}(V_{gs},V_{ds})]dV_{gs} - \int_{V_{dso}}^{V_{ds}} G_{gdf}(V_{gs},V_{ds})dV_{ds} \tag{4.2}$$

$$Q_g(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} [C_{gs}(V_{gs},V_{ds}) + C_{gd}(V_{gs},V_{ds})]dV_{gs} - \int_{V_{dso}}^{V_{ds}} C_{gd}(V_{gs},V_{ds})dV_{ds} \tag{4.3}$$

$$I_d(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} [G_m(V_{gs},V_{ds}) - G_{gdf}(V_{gs},V_{ds})]dV_{gs} + \int_{V_{dso}}^{V_{ds}} [G_{ds}(V_{gs},V_{ds}) + G_{gdf}(V_{gs},V_{ds})]dV_{ds} \tag{4.4}$$

$$Q_d(V_{gs},V_{ds}) = -\int_{V_{gso}}^{V_{gs}} C_{gd}(V_{gs},V_{ds})dV_{gs} + \int_{V_{dso}}^{V_{ds}} [C_{ds}(V_{gs},V_{ds})dV_{ds} + C_{gd}(V_{gs},V_{ds})]dV_{ds} \tag{4.5}$$

where V_{gs} and V_{ds} are the intrinsic gate-to-source and drain-to-source bias voltages. V_{gso} and V_{dso} are the initial (lowest) bias voltages [3]. The topology then can be drawn as shown in Figure 4.1. The quasi-static model fails in estimating the high frequency dispersion in G_m as well as the charging and discharging time constants associated with gate-to-source and gate-to-drain regions, which help in modeling, in an essence, the trapping effects of the transistor [2].

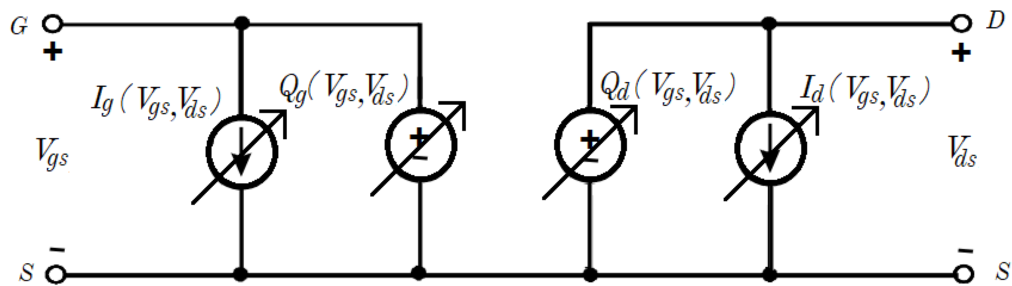

Figure 4.1 Quasi-Static Large-Signal topology [2].

4.1.2 Non Quasi-Static Large-signal topology

In this model, R_i and R_{gd} are inserted to model the quadratic frequency dependency of Y_{11} and Y_{22} at high frequencies, this is caused by the time delay related to charging and discharging the area underneath the gate from the source and the drain sides [2][4]. τ has been included as well to model the high frequency reduction in G_m. The Y-parameters representation of such a network can be extracted from the intrinsic Y-parameters in (3.43)–(3.49). We can find the current and charge components as follows [4-5]:

$$I_{gs}(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} G_{gsf}(V_{gs},V_{ds})dV_{gs} \tag{4.6}$$

$$Q_{gs}(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} C_{gs}(V_{gs},V_{ds})dV_{gs} + \int_{V_{dso}}^{V_{ds}} C_{ds}(V_{gs},V_{ds})dV_{ds} \tag{4.7}$$

$$I_{gd}(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} G_{gdf}(V_{gs},V_{ds})dV_{gs} - \int_{V_{dso}}^{V_{ds}} G_{gdf}(V_{gs},V_{ds})dV_{ds} \tag{4.8}$$

$$Q_{gd}(V_{gs},V_{ds}) = \int_{V_{gso}}^{V_{gs}} C_{gd}(V_{gs},V_{ds})dV_{gs} - \int_{V_{dso}}^{V_{ds}} [C_{ds}(V_{gs},V_{ds})dV_{ds} + C_{gd}(V_{gs},V_{ds})]dV_{ds} \tag{4.9}$$

$$I_{ds}(V_{gs},V_{ds}) = \frac{1}{1+j\omega\tau} I_{ds}^{DC}(V_{gs},V_{ds}) + \frac{j\omega\tau}{1+j\omega\tau} I_{ds}^{RF}(V_{gs},V_{ds}) \tag{4.10}$$

Where I_{ds}^{DC} is the measured DC the I_{ds}^{RF} is modeled with the same expression as in (4.4). The topology for this large-signal model is shown in Figure 4.2. The main disadvantage of such topology is the numerical integration of all the intrinsic capacitances and conductances, which fails to model the initial charge and leakage currents existent within the device. Another disadvantage of this model is the inability to model the DC and RF transitions at low-frequency operation [5].

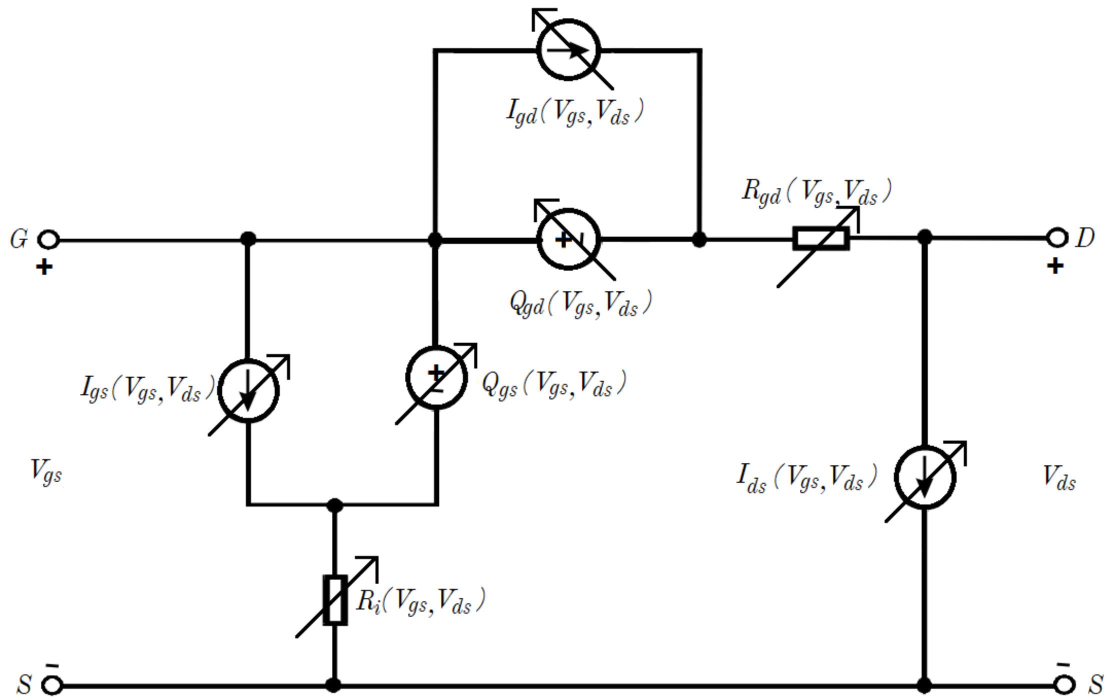

Figure 4.2 Non Quasi-Static Large-Signal topology [4].

4.1.3 Proposed Large-signal topology

The proposed large-signal topology uses the intrinsic network as in the EC-SSM without any integration, which simplifies the model without the necessity of integrating the intrinsic conductances and capacitances. We have neglected G_{gsf} and G_{gdf} due to their very small contribution as discussed in the previous chapter. We have included a series of RC branches at both the input and the output to improve the low-frequency transition between DC and RF [2]. These branches are also important in modeling charge-trapping effects, as will be seen later in section 4.4. Figure 4.3 shows the proposed large-signal model. The details on I_{ds} will become clearer by the end of this chapter.

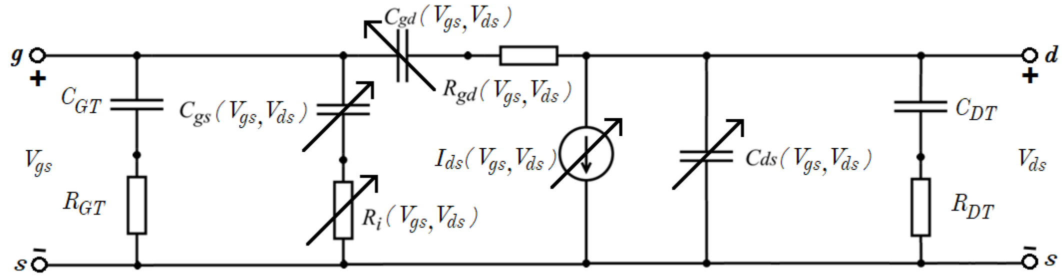

Figure 4.3 Proposed large-signal model.

4.2 Isothermal trapping-free drain current extraction

In order to model the effects of non-idealities of GaN HEMT on the current dispersion, one should first develop a drain current that is a function of only the gate and drain voltages. For simplicity, we will be calling this current as an isothermal trapping-free current since it does not depend on second-order non-idealities such as charge-trapping and self-heating effects. It could, however, depend on first-order non-idealities such as channel length modulation. The isothermal trapping-free drain current can be derived either through empirical ways through static DC measurements with the help of pulsed IV measurements, or through analytical expression through recently implemented Surface Potential model or Quasi-Physical Zone Division model.

4.2.1 Empirical model

The empirical model requires both the static and pulsed IV measurements, where the pulsed IV measurements are taken at certain quiescent bias points describing different phenomena of the GaN HEMT [3]. In the empirical model, the drain current is composed of the isothermal trapping-free current plus three fitting parameters describing the non-idealities found in GaN HEMT. This equation, with the help of the static IV measurements, and 4 pulsed IV measurements taken at different quiescent bias points, can help in superimposing each non-ideal effect alone and hence, by solving linearly the equation 4 times for each parameter in the equation, we can determine all the fitting parameters including the isothermal trapping-free current [3]. This method, however, extracts the isothermal trapping-free current without any relation to the physics of the

device, hence a closed-form solution is not derivable when choosing this model as appose to the Surface Potential model and Quasi-Physical Zone Division model.

4.2.2 Surface Potential model

The Surface Potential (SP) model is a physical-based model used to model the drain current of the transistor based on the surface potential of the GaN HEMT [6]. In order to extract the GaN HEMT's isothermal trapping-free drain current, the position of the Fermi level (E_f) and the density of the 2DEG (n_s) should be first solved. Their expressions are given as follows [6][7]:

$$E_f = V_{eff}\left(1 - \frac{V_{eff} + v_t[1 - \ln(\xi V_{eff_n})] - \frac{\gamma_0}{3}\left(\frac{C_{eff}V_{eff}}{q}\right)^{\frac{2}{3}}}{V_{eff}\left(1 + \frac{v_t}{V_{eff_d}}\right) + \frac{2\gamma_0}{3}\left(\frac{C_{eff}V_{eff}}{q}\right)^{\frac{2}{3}}}\right) \tag{4.11}$$

$$n_s = \left(\frac{1}{q}\right)V_{eff}C_{eff}\frac{V_{eff} + v_t[1 - \ln(\xi V_{eff_n})] - \frac{\gamma_0}{3}\left(\frac{C_{eff}V_{eff}}{q}\right)^{\frac{2}{3}}}{V_{eff}\left(1 + \frac{v_t}{V_{eff_d}}\right) + \frac{2\gamma_0}{3}\left(\frac{C_{eff}V_{eff}}{q}\right)^{\frac{2}{3}}} \tag{4.12}$$

where

$$V_{eff} = V_{gs} - V_p\ ,\ V_{eff_n} = \frac{V_{eff}\eta_1}{\sqrt{(V_{eff}{}^2 + \eta_1{}^2)}}\ ,\ V_{eff_p} = \frac{V_{eff}\eta_2}{\sqrt{(V_{eff}{}^2 + \eta_2{}^2)}}\ ,\ \eta_1 = \frac{e}{\xi}\ ,\ \eta_2 = \frac{1}{\xi}\ ,\ \xi = \frac{C_{eff}}{qDv_t}\ .$$

and v_t is the thermal voltage (25mV at room temperature), C_{eff} is the effective gate capacitance per unit area, q is the electronic charge, V_p is the pinch-off voltage, D is the effective density of quantum states, and γ_o is a measurement-determined parameter.

After finding E_f and n_s, the SP at the source and drain can be found as $\phi_{ss} = E_f$ and $\phi_{sd} = E_f + V_{ds}$, respectively [6]. The average SP can also be calculated as $\phi_{sm} = \frac{\phi_{ss} + \phi_{sd}}{2}$.

The n_s is used to find the gate charge (Q_g) and the drain charge (Q_d), The derivation of the isothermal trapping-free drain current in terms of charge components is long and complicated [6], hence we will be presenting only the final expression as [6]:

$$I_{dso} = \frac{\mu_{eff} C_{eff} W}{\delta L}(V_{eff} + v_t - \phi_{sm})(\phi_{sd} - \phi_{ss})(1 + \lambda V_{ds}) \quad (4.13)$$

where μ_{eff} is the effective electron mobility, W the width of the transistor, L the channel length, and λ the channel length modulation coefficient. δ takes into account the velocity saturation.

The advantages of the SP model are its high accuracy and physical relevance [6]. The major disadvantage is that it uses 27 parameters to develop the isothermal trapping-free drain current expression [8]. We may have not provided many details about the SP model here in this subsection because we will be paying more attention to the Quasi-Physical Zone Division model, which is a much simpler technique and accurate enough to describe the isothermal trapping-free current of the GaN HEMT.

4.2.3 Quasi-Physical Zone Division model

This model will be retained in this thesis work for building the isothermal trapping-free drain current. Quasi-Physical Zone Division (QPZD) model is a compact model that divides the channel into three zones based on the location of the gate, drain, and the source and then, by solving physics-based equations using boundary conditions, we can obtain the final isothermal trapping-free current expression [9]. The major advantage of such a technique it can be easily scaled and adjusted according to the fabricated device parameters [8].

First approach, as done in the previous subsection, is to find the E_f and n_s required to build the isothermal trapping-free drain current. Since the equations in (4.11) and (4.12) are very difficult to handle, we have decided to use the simplified formulas as follows [9][10]:

$$n_s = Dv_t\left[\ln\left(1+e^{\frac{E_f-E_o}{v_t}}\right)+\ln\left(1+e^{\frac{E_f-E_1}{v_t}}\right)\right] \tag{4.14}$$

$$E_o = \gamma_o n_s^{2/3} \tag{4.15}$$

$$E_1 = \gamma_1 n_s^{2/3} \tag{4.16}$$

$$n_s = \frac{C_{eff}}{q}(V_{eff} - E_f) \tag{4.17}$$

where E_o is the lowest quantized energy in the 2DEG, E_1 is the second lowest quantized energy in the 2DEG and γ_1 is experimentally-measured parameter.

After solving (4.14) – (4.17) to find E_f and n_s, we can now use the zone division model to find the isothermal trapping-free drain current. Under unsaturated operation, we can divide the channel into 3 different zones, the Source Neutral Zone Z_1, the Intrinsic FET Zone Z_2 and the Drain Neutral Zone Z_3, as shown in Figure 4.4 [9]. Under unsaturated conditions, the electrons in the quantum well will be filled with electrons, causing the space charge in the source and the drain neutral zones to be negligible [11]. This shows that there is a complete screening of the positive polarization charge above the AlGaN/GaN interface, which causes the electron density in the channel at the drain and source neutral zones to be constant and equal to the amount of positive polarization charge in the upper side of the AlGaN/GaN interface [11].

The vertical electric field is also constant in the drain and source neutral zones. Figure 4.4 illustrates such a condition. Hence at the Z_1, we can write the electron velocity taking into account the velocity saturation as [9]:

$$v = \frac{\mu_{eff} E}{\sqrt{1 + (\frac{E}{E_c})^2}} \tag{4.18}$$

which can be rewritten as:

$$E = \frac{E_c I_{dso}}{\sqrt{I_{sat}^2 - I_{dso}^2}} \tag{4.19}$$

where $E_c = v_{sat}/\mu_{eff}$ is the critical electrical field at which electron's velocity saturate, with v_{sat} the saturation velocity. I_{sat} is the current at velocity saturation conditions given by $I_{sat} = Wqn_s(V_{gs})v_{sat}$. It should be noted that $n_s(V_{gs})$ is the density of the 2DEG as a function of the gate-to-source voltage [9].

We can use (4.19) in order to find the values of V_{si} and V_{di} in Figure 4.4 as follows [9]:

$$V_{si} = \frac{E_c l_s I_{dso}}{\sqrt{I_{sat}^2 - I_{dso}^2}} \tag{4.20}$$

$$V_{di} = V_{ds} - \frac{E_c l_d I_{dso}}{\sqrt{I_{sat}^2 - I_{dso}^2}} \tag{4.21}$$

where l_s and l_d are the lengths of the source and drain access regions, respectively.

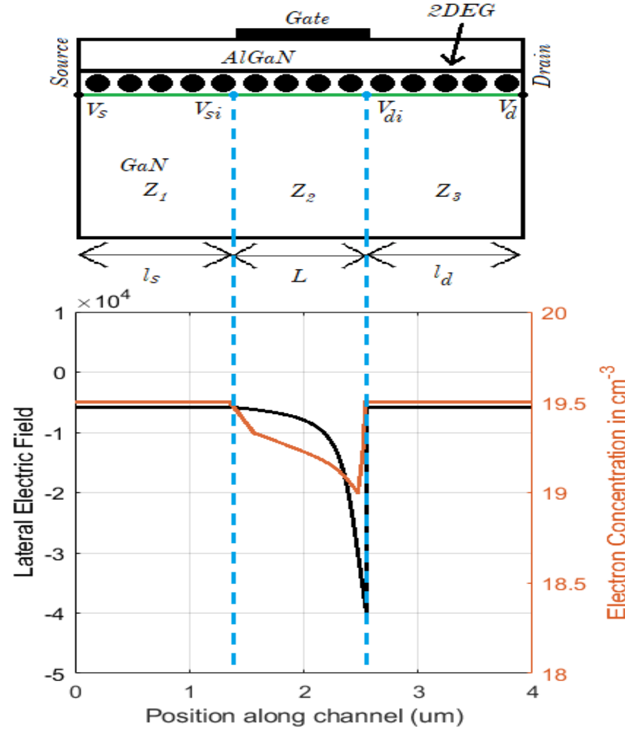

Figure 4.4 Quasi-Physical Zone Division model illustration using zone-divided GaN HEMT structure and highlighting electron concentration and lateral electric field of a generic GaN HEMT device in each region [9][11].

Moving to Z_2, we will have a gradual channel that can be described using the following expression [9]:

$$n_s(x) = \frac{C_{eff}}{q}(V_{eff} - V(x)) \tag{4.22}$$

where $n_s(x)$ is the electron charge density at position x in-between the positions of V_{si} and V_{di}. Using $E(x) = -dV/dx$ and substituting (4.18) and (4.22) in $I_{dso} = Wqn_s(x)v(x)$, we can get [9]:

$$\int_0^L I_{dso}dx = \int_{V_{si}}^{V_{di}} \sqrt{[W\mu_{eff} C_{eff} (V_{eff} - V(x)]^2 - (\frac{I_{dso}}{E_c})^2} dV \tag{4.23}$$

The integration in (4.23) can be solved numerically; however, a good approximation is to neglect the first term on the right side of the equation because it is very small compared to the second term. After substituting (4.20) and (4.21) into the resultant integration from (4.23) we get [9]:

$$I_{dso} = \frac{(E_c L + V_{ds}) I_{sat}}{\sqrt{E_c^{\,2} (l_s + l_d)^2 + (E_c L + V_{ds})^2}} \tag{4.24}$$

note that, because the above expression does not result in a zero current at $V_{ds} = 0$, $E_c L$ has been equated to zero to allow that [9]. A linear equation describing the channel length modulation has been added as well. The final expression is given as [9]:

$$I_{dso} = \frac{I_{sat} V_{ds} (1 + \lambda V_{ds})}{\sqrt{E_c^{\,2} (l_s + l_d)^2 + (E_c L + V_{ds})^2}} \tag{4.25}$$

The pinch-off voltage V_p and the effective mobility μ_{eff} are needed in the equations shown in this subsection. They can be calculated using the following expressions [8][12]:

$$V_p = \phi_B(x) - \Delta E_c(x) - \frac{q N_d d^2}{2\varepsilon_{AlGaN}} - \frac{q\sigma d}{\varepsilon_{AlGaN}} \tag{4.26}$$

$$\mu_{eff} = \frac{\mu_o}{1 + \Theta_1 V_{eff} + \Theta_2 V_{eff}^{\,2}} \tag{4.27}$$

where $\phi_B(x)$ is the Schottky barrier height, $\Delta E_c(x)$ is the conduction band discontinuity at the AlGaN/GaN interface, N_d is the doping concentration of AlGaN, ε_{AlGaN} is the permittivity of AlGaN, d is the thickness of AlGaN layer, σ is the polarization induced charge sheet density, μ_o is the low-field mobility of electrons, and Θ_1 and Θ_2 are fitting parameters for the effective mobility. $\phi_B(x)$ and $\Delta E_c(x)$ can be calculated from [13], while the remaining parameters are measured from the fabricated devices in [8] and [14].

4.3 Results of QPZD modeling technique

The equations (4.14) – (4.17) are highly non-linear and difficult to solve analytically, hence we have used a self-implemented non-linear solver in MATLAB that is based on a trial-and-error iterative approach. After solving these equations, we have plotted the energy levels as a function of V_{gs} as shown in Figure 4.5. We have also plotted n_s as a function of V_{gs} in Figure 4.6. The shape of these plots matches very well with previous literature on the QPZD model [7]-[10]. It can be shown from Figure 4.5 that the Fermi level exceeds the lowest energy in the quantum well E_0, generating a 2DEG around the pinch-off point (close to -3V), which is to be expected. To avoid using non-linear solver and to reduce computational costs, a fitting equation has been used to fit n_s to the results of the non-linear solver as follows [9]:

$$n_s = A_n \cdot \tanh(\alpha_n \cdot (V_{eff}) + b_n) + B_n \tag{4.28}$$

The values of the fitting parameters were obtained using GWO, as discussed previously. Figure 4.6 also shows the results of the fitting model.

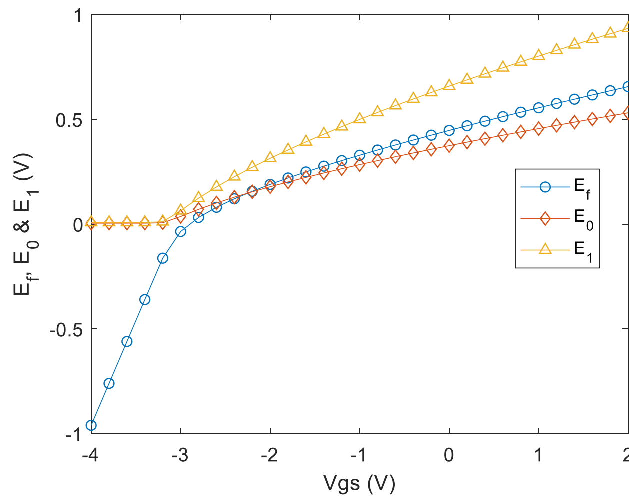

Figure 4.5 Energy levels vs. V_{gs} using numerical non-linear solver.

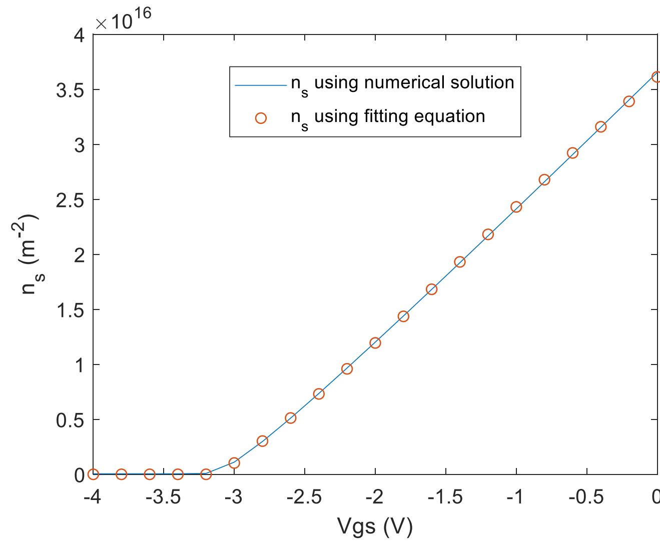

Figure 4.6 n_s vs. V_{gs} using non-linear solver and using fitting equation (4.28).

I_{sat} used in (4.25) has been plotted in Figure 4.7. This plot is very important since it allows us to verify the maximum current reached in the linear region of the device operation. The maximum current is 140 mA, very close to the maximum current reached during measurements before the device encounters current dispersion. A comparison between the isothermal trapping-free current and the measured static DC for both GaN/D and GaN/SiC is shown in Figure 4.8. We may notice how the peak currents of both devices in the linear region for the maximum V_{gs} (0V) are very close to the current given by I_{sat} at V_{gs} = 0V in Figure 4.7. In addition to that, the isothermal trapping-free current and the measurements are well matched at the linear region. The isothermal trapping-free current during saturation operation tracks well the measurements at intermediate values of V_{gs} where dispersive effects are at minimal. However, it fails to predict the dispersive effects at high V_{gs} during saturation conditions due to the high dispersive effects, which is expected. Dispersive effects will be modeled in the next section. The two GaN HEMT devices measured here were fabricated under the same operating conditions and hence, one model was enough to model their isothermal trapping-free currents. All the parameters used in the equations necessary to build the large-signal isothermal trapping-free current and their values are summarized in Table 4.1.

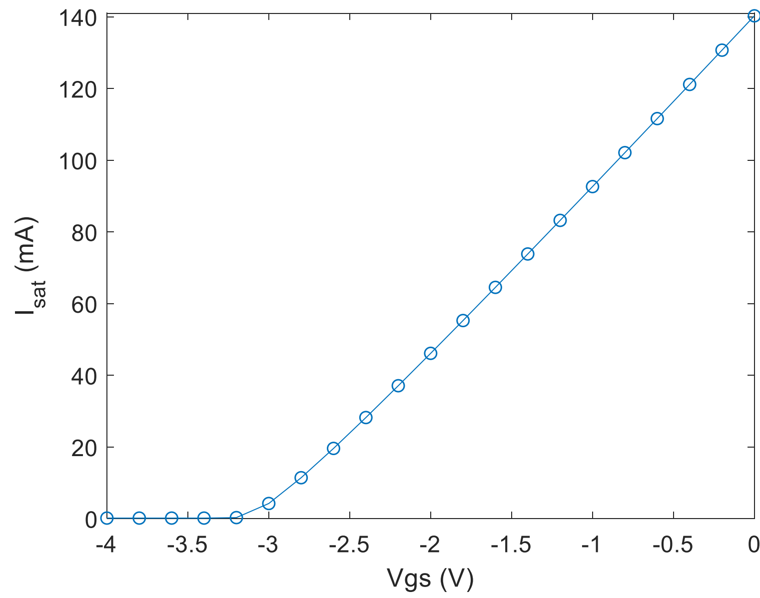

Figure 4.7 A plot of I_{sat} vs. V_{gs}.

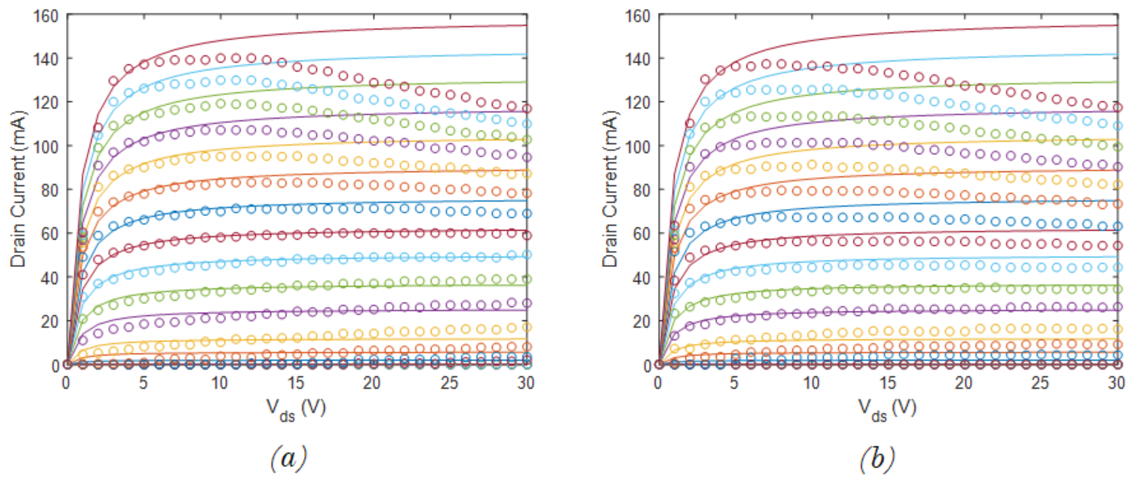

Figure 4.8 Static DC IV measurements (circles) and isothermal trapping-free current simulations (lines) at V_{gs} = -4 to 0 V at a step of 0.2 V and V_{ds} = 0 to 30 V at a step of 1V for (a) GaN/D and (b) GaN/SiC.

Table 4.1 Parameters used to model the isothermal free-trapping current of 200um/200nm GaN HEMT [8][13][14].

Parameter	200 um/ 200 nm GaN HEMT Parameters		
	Description	***Value***	***Unit***
D	Effective density of quantum states	1×10^{18}	$m^{-2}*V^{-1}$
v_t	Thermal voltage at room temperature	0.026	V
γ_0	Experimentally-measured value for E_0	2.12×10^{-12}	$m^{4/3}*V$
γ_1	Experimentally-measured value for E_1	3.73×10^{-12}	$m^{4/3}*V$
C_{eff}	Effective gate capacitance per unit area	0.0046	F/m
V_p	Pinch-off voltage	-3.0432	V
q	Electronic charge	1.6×10^{-19}	C
v_{sat}	Saturation Velocity	1.2×10^{5}	m/s
μ_0	Low-field electron mobility	0.035	$m^2/V*s$
W	Width of the channel	200	um
L	Length of the channel	200	nm
l_s	Source access region's length	100	nm
l_d	Drain access region's length	100	nm
$\phi_B(x)$	Schottky Barrier Height (V)	1.23	V
$\Delta E_c(x)$	Conduction band offset at the AlGaN/GaN interface	0.422	V
$\sigma(x)$	Polarization charge density	1.1×10^{17}	m^{-2}
N_d	Doping concentration of n-AlGaN layer	0	cm^{-3}

Table 4.1 (continued)

d	Thickness of AlGaN layer	20	nm
ε_{AlGaN}	Permittivity of the AlGaN layer	9.14×10^{-11}	F/m
Θ_1	First-order fitting parameter for the effective mobility	20×10^{-7}	1/V
Θ_2	Second-order fitting parameter for the effective mobility	15×10^{-14}	$1/V^2$
λ	Channel length modulation parameter	1×10^{-6}	V^{-1}
A_n	First fitting parameter for n_s equation	$4.2x10^{16}$	No unit
α_n	Second fitting parameter for n_s equation	0.298	No unit
b_n	Third fitting parameter for n_s equation	-0.53	No unit
B_n	Fourth fitting parameter for n_s equation	$2.1x10^{16}$	No unit

4.4 Charge-trapping and self-heating modeling

As was shown in section 4.3, the QPZD model cannot describe current dispersion due to charge-trapping and self-heating effects. Most models in literature if not all, describe such effects based on empirical fitting parameters that take into account such non-idealities [2][3][5][7]-[9][12][14].

In order to model such effects, we require pulsed IV measurements at certain quiescent bias points that allow us to describe each effect independently [2][3]. The equation used to describe the drain current including current dispersion may be written as [15]:

$$I_{ds} = I_{dso} + \alpha_G (V_{gs} - V_{gsq}) + \alpha_D (V_{ds} - V_{dsq}) + \alpha_T I_{dsq} V_{dsq} \tag{4.29}$$

where α_G, α_D and α_T are fitting parameters related to surface-trapping, buffer-trapping and self-heating effects, respectively. V_{gsq} and V_{dsq} are the quiescent bias points at the gate and the drain sides, respectively [15]. I_{dsq} is the quiescent bias drain current. The amount of trapping depends on the rate of dynamic changes of the applied voltages (V_{gs} and V_{ds}) with respect to the values V_{gsq} and V_{dsq} at the gate and drain sides, respectively [15].

In (4.29), we have four unknowns, namely α_G, α_D, α_T and I_{dsq}, where I_{dso} was extracted using QPZD in the previous section. As discussed in chapter 2, pulsed IV measurements have a quiescent bias point at which it is pulsed into a certain voltage. For example, by pulsing V_{gsq} at -4 V to multiple V_{gs} values and keeping V_{ds} fixed, we can obtain a family of curves for that particular value of V_{gsq}. Figures 4.9 and 4.10 show the pulsed IV measurements obtained from technical literature for GaN/D and GaN/SiC at the necessary quiescent bias points, where the pulsewidth is 500 ns and the duty cycle is 0.1% in order to neglect self-heating effects [8][16].

Since surface-trapping effects are mainly associated with the gate voltage (surface of the gate and the dislocations in the passivation layer), we will be choosing two extreme quiescent bias points for V_{gsq} (-4 and 0 V in our case) to simulate the surface traps [15]. V_{dsq}, however, must be 0V in order to remove the self-heating effects from (4.29). Since we are not evaluating the dynamic changes at the drain side, the third term on the right side of (4.29) can be removed (buffer-trapping can be neglected). By having two quiescent gate bias points, (4.29) can be solved twice for each quiescent bias point as follows [15]:

$$\alpha_G = \frac{I_{dsp}\Big|_{V_{gsq}=V_{gsqi}}^{V_{dsq}=V_{dsqi}}(V_{gs},V_{ds}) - I_{dsp}\Big|_{V_{gsq}=V_{gsqf}}^{V_{dsq}=V_{dsqf}}(V_{gs},V_{ds})}{V_{gsqf} - V_{gsqi}} \tag{4.30}$$

where I_{dsp} is the pulsed IV current from Figures 4.9 and 4.10 at such quiescent bias points. V_{gsqf} and V_{gsqi} are 0V and -4 V, respectively, and $V_{dsqi} = V_{dsqf} = 0$V. Figure 4.11 shows α_G values for both GaN/D and GaN/SiC.

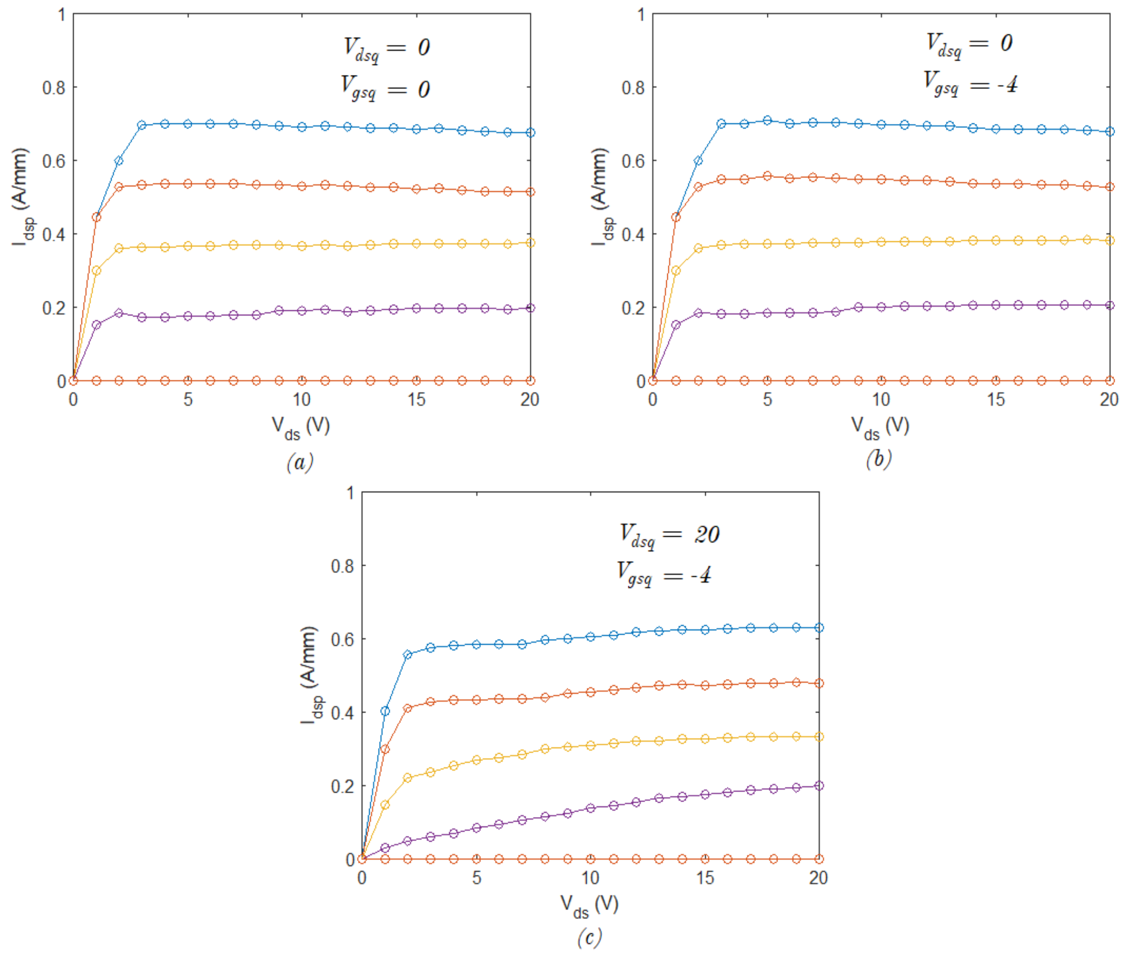

Figure 4.9 Pulsed IV-measurements for 2x100 um GaN/D at quiescent bias points of (a) V_{gsq} = 0V, V_{dsq} = 0V (b) V_{gsq} = -4V, V_{dsq} = 0V and (c) V_{gsq} = -4V, V_{dsq} = 20V [16].

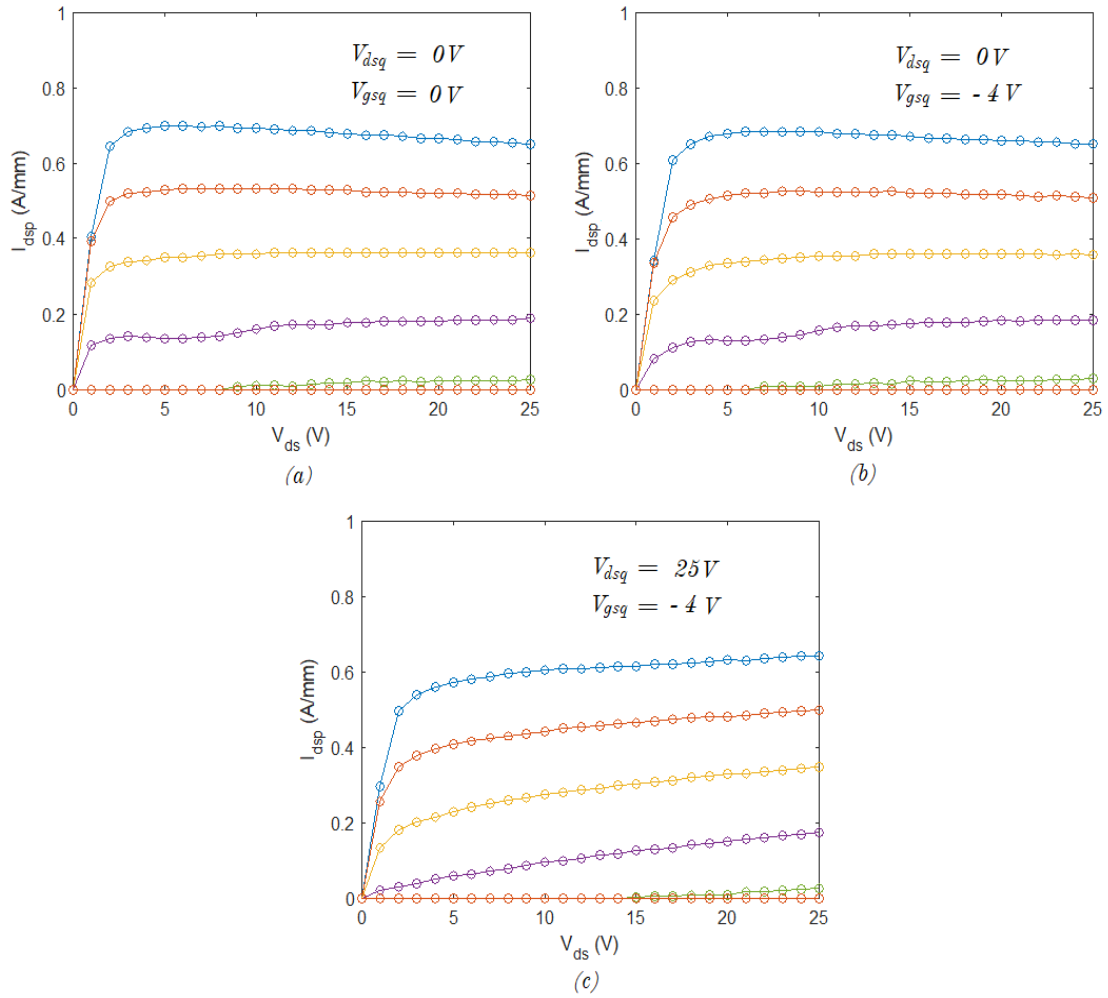

Figure 4.10 Pulsed IV-measurements for 4x50 um GaN/SiC at quiescent bias points of (a) V_{gsq} = 0 V, V_{dsq} = 0V (b) V_{gsq} = -4 V, V_{dsq}= 0V and (c) V_{gsq} = -4 V, V_{dsq} = 25V [8].

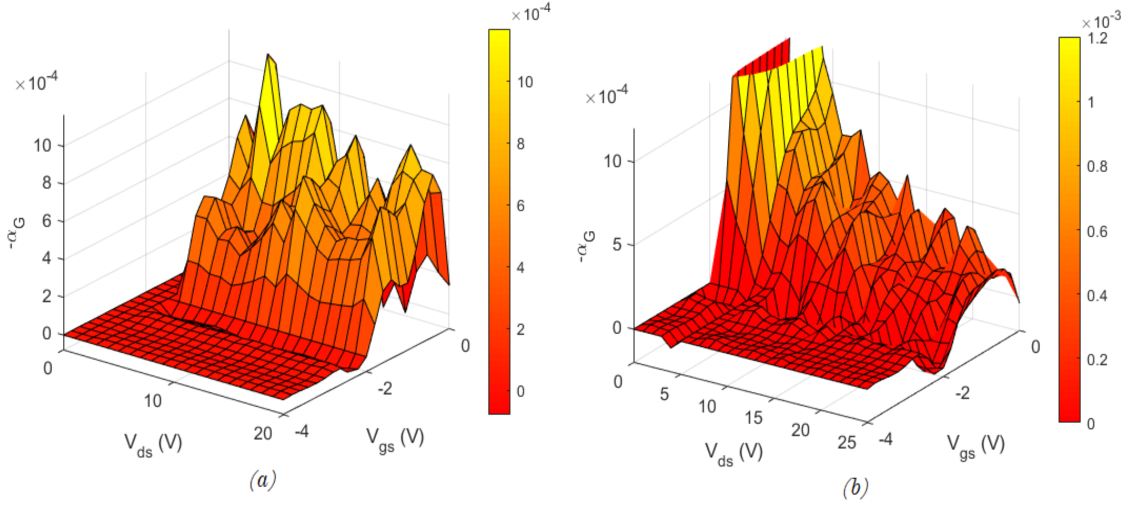

Figure 4.11 α_G at different V_{gs} and V_{ds} for (a) GaN/D, (b) GaN/SiC.

In order to estimate buffer-trapping effects, V_{dsq} must be chosen at two extreme points (e.g., 0V and 20V). Since these buffer-trapping effects are close to the channel, they are stimulated by the drain voltage [15]. V_{gsq} must be -4V to remove power dissipation and hence, self-heating effects are neglected. Similarly, V_{gsq} is a fixed value hence we are not evaluating the rate of dynamic changes at the gate, which results in the removal of the second term in (4.29). We can solve equation (4.29) twice for each V_{dsq} value and get the following expression [15]:

$$\alpha_D = \frac{I_{dsp}\Big|_{V_{gsq}=V_{gsqi}}^{V_{dsq}=V_{dsqi}}(V_{gs},V_{ds}) - I_{dsp}\Big|_{V_{gsq}=V_{gsqf}}^{V_{dsq}=V_{dsqf}}(V_{gs},V_{ds})}{V_{dsqf}-V_{dsqi}} \tag{4.31}$$

where V_{dsqi} = 0V, V_{dsqf} = 20V for GaN/D and 25V for GaN/SiC. $V_{gsqf} = V_{gsqi}$ = -4 V. α_D for various V_{gs} and V_{ds} values are plotted in Figure 4.12 for GaN/D and GaN/SiC.

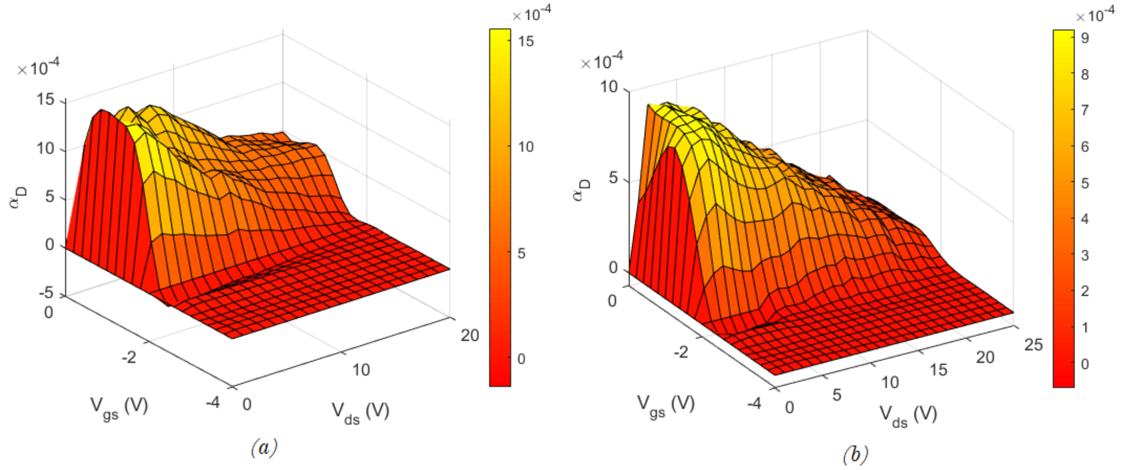

Figure 4.12 α_D at different V_{gs} and V_{ds} for (a) GaN/D, (b) GaN/SiC.

Under normal operating conditions (static), $V_{gsq}= V_{gs}$, $V_{dsq} = V_{ds}$, and $I_{dsq} = I_{ds}$ [15]. Hence, the second and third terms in (4.29) can be removed, which will allow us to write the expression for the self-heating fitting parameter as follows [15]:

$$\alpha_T = \begin{cases} \dfrac{I_{ds} - I_{dso}}{I_{ds}V_{ds}}, & \text{for } I_{ds}V_{ds} > 0 \\ 0, & \text{for } I_{ds}V_{ds} = 0 \end{cases} \tag{4.32}$$

A plot for α_T is shown in Figure 4.13.

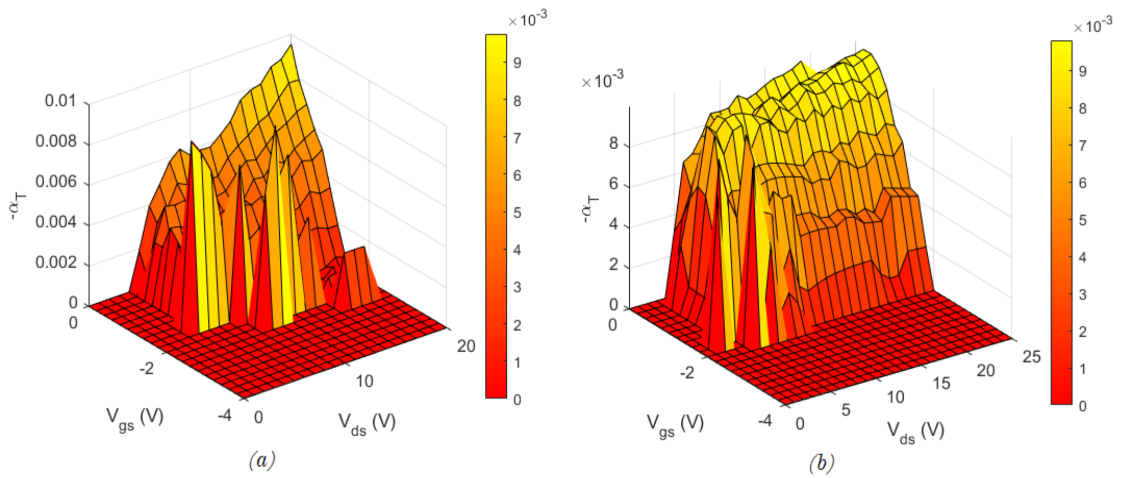

Figure 4.13 α_T at different V_{gs} and V_{ds} for (a) GaN/D, (b) GaN/SiC.

From Figure 4.11, we can notice that during saturated operation of the device, the values of α_G for both devices are very close to each other. This is related to the deposition of the passivation layer that minimizes surface traps. This can also be observed in the pulsed IV characteristics used to evaluate the surface traps, where the pulsed IV barely changed from V_{gsq} = 0V to V_{gsq} = -4V at V_{dsq} = 0V. Some errors are observed in the unsaturated region between the two devices.

In Figure 4.12, α_D showed an increase in GaN/D compared to GaN/SiC. This increase indicates increased buffer-traps in the GaN/D compared to GaN/SiC. This increase is mainly due to the wafer transfer process of the Diamond substrate during the fabrication of the device, which caused dislocations and contamination at the interface between the Diamond substrate, the nucleation layer and GaN buffer. This observation is verified with [14]. This effect will lead primarily to induced leakage current through the substrate and an increase in the pinch-off voltage, which deteriorates the PAE characteristics of the GaN/D as will be shown in chapter 5.

In Figure 4.13, self-heating should occur in regions of high V_{ds} and high V_{gs} values. We can notice that the self-heating effect in GaN/SiC is direr than that in GaN/D, the intensive yellow light in the plots underline this point. This is to be expected since Diamond substrates have a high thermal conductivity compared to SiC substrates. We can note some error pulses at different regions in Figure 4.13. This may be attributed to the fact that self-heating parameter fitting is based on empirical fitting by using the static DC measurements. In other words, the differences between the isothermal trapping-free current and the measured current (where self-heating effects are at minimal) were fitted together, appearing as error pulses in α_T; this disadvantage will be discussed in the last chapter.

Another point that should be discussed is another limitation in (4.29). The values (V_{gs} - V_{gsq}), (V_{ds} - V_{dsq}) and I_{dsq}, vary depending on the quiescent bias operating condition of the device, regardless if that bias was static or pulsed. Since we are measuring the dynamic characteristics of the device using these average voltages and currents, they need to be measured in real-time during the simulations of the model, which is difficult to do through MATLAB but easier in the ADS software. This requires a slight modification

to the proposed model in Figure 4.3. The final large-signal model is shown in Figure 4.14. The dynamic changes at the gate and drain sides are sensed by R_{GT} and R_{DT}, respectively [2]. A circuit has been added to measure $I_{dsq}V_{dsq}$ (or V_{th}), where R_{th} is the normalized thermal resistance, and C_{th} models the rate of dynamic changes on the drain side due to self-heating effects [2]. The trapping time constants τ_{GT} and τ_{DT} are chosen to be in the range of 1×10^{-4} - 1×10^{-5} and the trapping time constant τ_{th} is chosen around 1 ms [2].

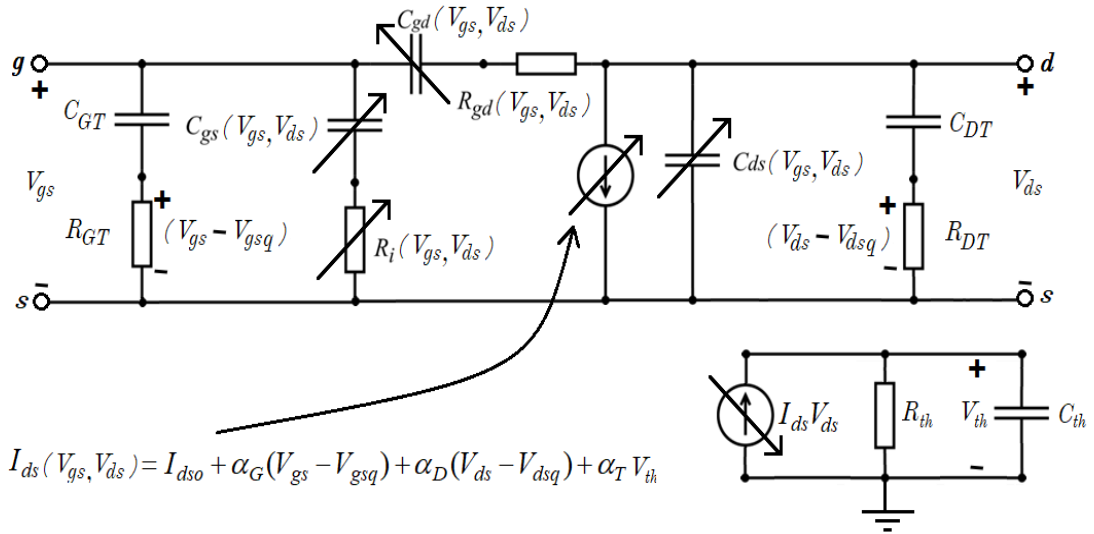

Figure 4.14 Large-signal model with self-heating and charge-trapping models included [2].

4.5 Conclusion

This chapter was devoted to modeling the non-linear drain current with its dispersive effects. We first, showed the circuit topologies used to model the drain current. Quasi-static topology is the simplest topology and depends solely on the intrinsic parameters extracted at multiple bias points. This topology, however, fails at modeling high-frequency dispersion in G_m and the time constants associated with charging/discharging the depletion region at the source and drain sides. This was solved, however, by using the non-quasi-static approach. Due to difficulties in modeling the intrinsic capacitances as charge components, we have decided to use the intrinsic capacitances from the EC-SSM as is, in the large-signal model. RC branches have been added as well to help in providing

a smooth transition between DC and RF operations. In order to develop a model for the drain current that describes the dispersive effects, we have to first model the isothermal trapping-free drain current.

Three approaches were discussed. The first was an empirical approach based on static and pulsed IV measurements, not directly related to the physics of the device. The second was the Surface Potential model, which was lengthy and had too many fitting parameters. The chosen technique was the Quasi-Physical Zone Division model, which is accurate and simple to implement. It is based on splitting the regions of the device based on geometry and solving physics-based equations taking into consideration the boundary conditions to derive the isothermal trapping-free drain current. Results of Quasi-Physical Zone Division model was presented with high relevance to the previous technical literature results. The isothermal trapping-free current was found to be highly accurate in the linear region and at intermediate values of V_{gs}. However, it failed to model the regions affected by the current dispersion. To solve this issue, an empirical modeling approach using pulsed IV measurements was used to model charge-trapping and self-heating effects. This approach has not only allowed us to model the drain current but also superimposed each individual effect, which allowed us to study each individual effect alone for both GaN/D and GaN/SiC. Based on the extracted results, it was found that GaN/SiC and GaN/D exhibit similar surface trapping effects in the saturation region due to the deposition of the passivation layer to both devices. GaN/D exhibited greater buffer-trapping effects compared to GaN/SiC. GaN/D but presented lower thermal resistivity compared to GaN/SiC. Further improvements to the model have been included to model charge-trapping and self-heating effects.

By the end of this chapter, we finished obtaining the data necessary to build the model in ADS and to validate all the work done so far. As will be seen in the next chapter.

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Chapter 5: ADS model, Overall Results and Validations

In this chapter, we will be validating the small- and large-signal characteristics of both GaN/D and GaN/SiC devices and compare them to measurements obtained from technical literature. This can be done by using the extracted small-signal parameters from the EC-SSMs and the drain currents from the EC-LSMs in implementing unified models in the Advanced Design System (ADS) circuit simulator. The *S*-parameters of the models, will first, be simulated and compared to the measurements at which they were extracted from. Static DC simulations will also be simulated and compared to measurements. Finally, load-pull and single-tone simulations will be conducted and compared to the measurements.

5.1 ADS model

In order to use the device models in different circuit designs such as LNAs and PAs, they should accurately describe the small-signal and large-signal characteristics using a unified model for each device. This can be done by implementing the model using ADS. The extrinsic extracted EC-SSM parameters are used as lumped components (resistors, capacitors, and inductors) each of them having a singular value. The intrinsic parameters, however, are described in CITIfile format, usually used by network analyzers such as Agilent 8510 [1][2]. This file format also supports multi-dimensional data, which is suitable for our case since the intrinsic parameters are mapped to multiple V_{GS} and V_{DS} values, as was seen in Figures 3.24 – 3.33. The intrinsic parameters and the large-signal parameters were read in ADS via Data Access Components or DAC as shown in Figure 5.1 for the case of GaN/D [3]. Variables were used to extract each individual data from the DAC based on the sensed V_{GS} and V_{DS} in the model, as shown in Figure 5.2.

The intrinsic parameters and the large-signal drain current were built using the Symbolically Defined Device (SDD) block. A 14-port network has been used to generate such a current in addition to auxiliary measurements such as the electron time delay used to model the high-frequency dispersion in G_m, average voltage measurements for trapping-effects, the power dissipation for self-heating effect, and differentiation for determining the capacitances' values. The first port is related to the voltage V_{gs} (_v1), and

the current in that port represents the capacitance C_{gs}. The second port is the gate-to-drain voltage (_v2) and its current represents the capacitance C_{gd}. Ports 3 and 4 represent the intrinsic resistances R_i and R_{gd}, respectively.

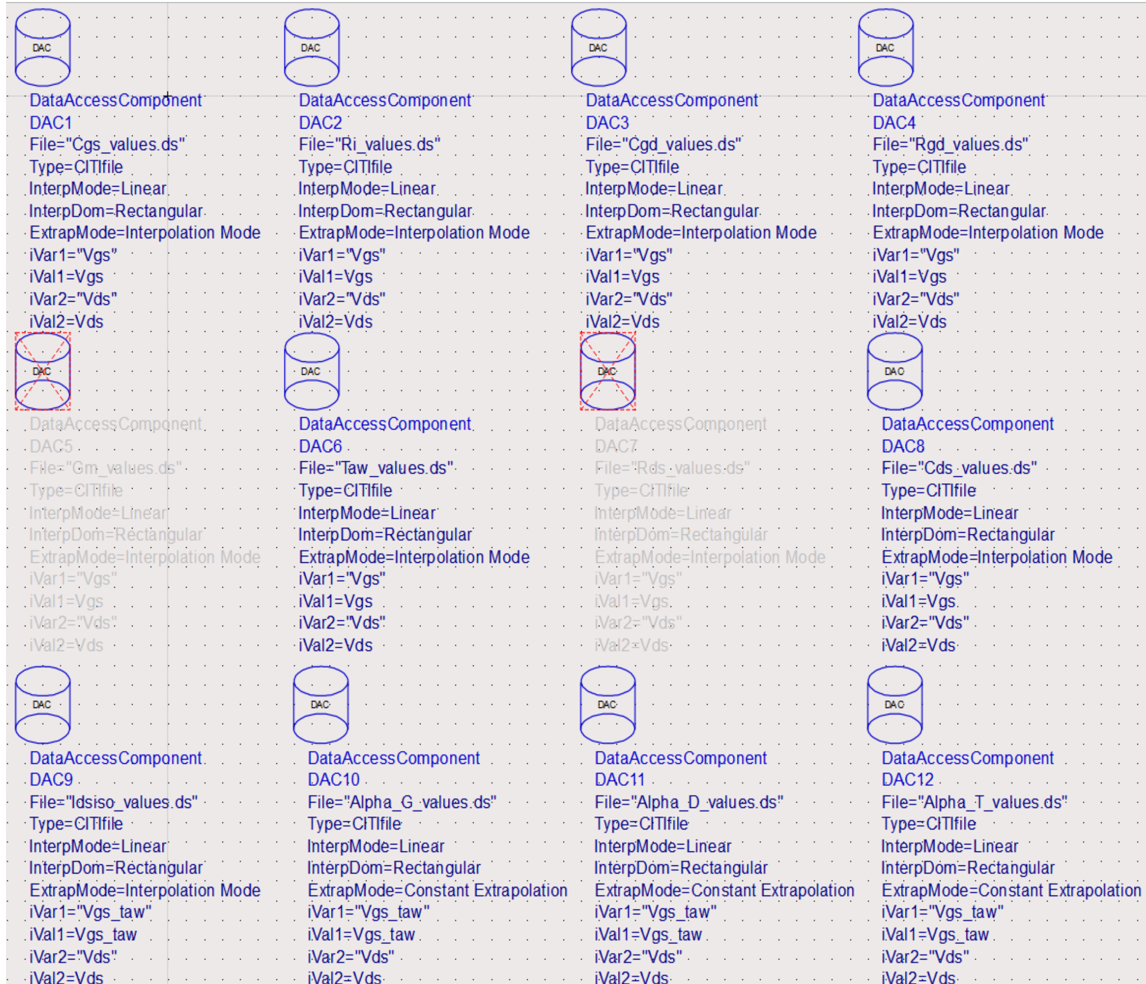


Figure 5.1 Data Access Components (DAC).

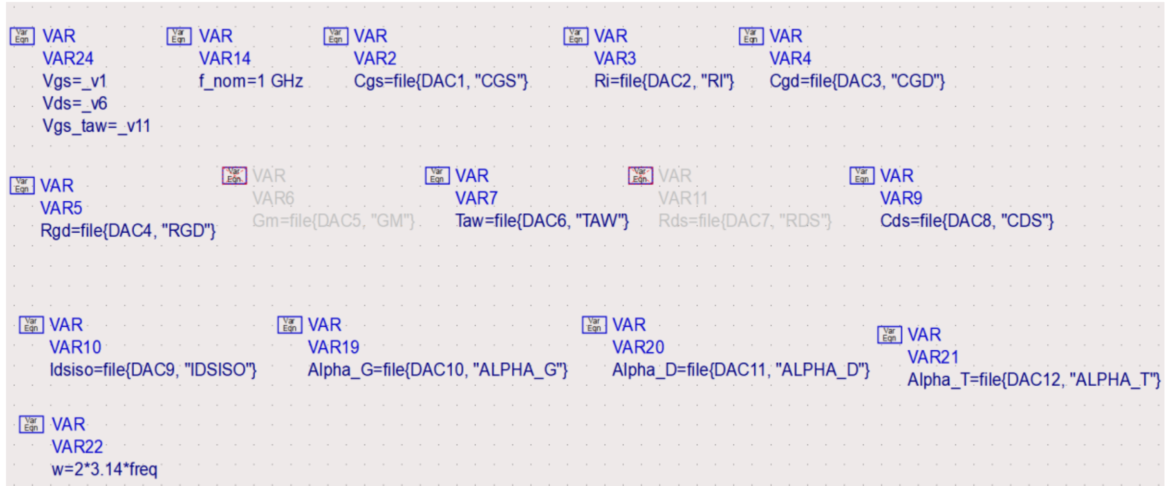


Figure 5.2 Variables in ADS.

Conditional statements were written to remove negative values of R_i and R_{gd} caused by interpolation [4]. The fifth port represents the capacitance C_{ds}. The 6th port represents the voltage V_{ds} (_v6) and its current is the drain-to-source current I_{ds}. Ports 7 and 8 measure respectively the average voltages across R_{GT} (_v7) and R_{DT} (_v8), which are used to estimate surface-trapping and charge-trapping effects [4][5]. The ninth port measures V_{th} (_v9) from the electrothermal model related to the self-heating effects while the tenth port measures the power dissipation (_v10) at the drain side [4][5]. Port 11 generates a voltage of $V_{gs}exp(-j\omega\tau)$ (_v11) used for the high-frequency dispersion in G_m [4][5]. Ports 12, 13 and 14 evaluate the differentiation required to find C_{gs}, C_{gd} and C_{ds}, respectively. The implemented model is shown in Figure 5.3. The GaN/SiC schematic model only differs in the extrinsic part but the intrinsic part is schematically exact, and hence it will not be shown.

In detail, each port in the SDD block can be represented by an explicit representation I[X,Y], or by an implicit representation F[X,Y], where X is the port number and Y the weighting function [6]. Explicit representation is used when generating a current that is a function of port voltages. Implicit representation is used when there are relationships between any ports' currents and voltages [6]. A third representation is the weighting function H[Z]. If Y = Z, then H[Z] will be used to indicate the frequency-dependent expression used to modify the port currents [6]. H[0] for example, represents the current

as-is with no modifications. H[1] is the time derivative. Any values for Z > 1 are user-defined. For our case, we defined the response H[2] to be the multiplication by $exp(-j\omega\tau)$.

A common way used to represent capacitances in ADS is by using charge elements Q_{gs} and Q_{gd} as in subsections 4.1.1 and 4.1.2 [4][5]. However, upon trying to integrate the capacitances manually, the simulated *S*-parameters were not accurate, probably due to the fact that there is an initial charge not taken into consideration while integrating [4]. Regardless, we fixed this issue by using the expression $I = C\ dV/dt$, which can be implemented as an explicit expression, as shown in Figure 5.3. However, the differentiation in ADS is treated as multiplication by $j\omega$ in the frequency domain and hence, if there are harmonics (as in large-signal models) at extremely high frequencies, they can cause a very sharp rate of change which causes the current to diverge [6]. This has been fixed, however, by multiplying the explicit current by f_{nom} = 1 GHz which makes the derivative less sensitive to harmonics [6].

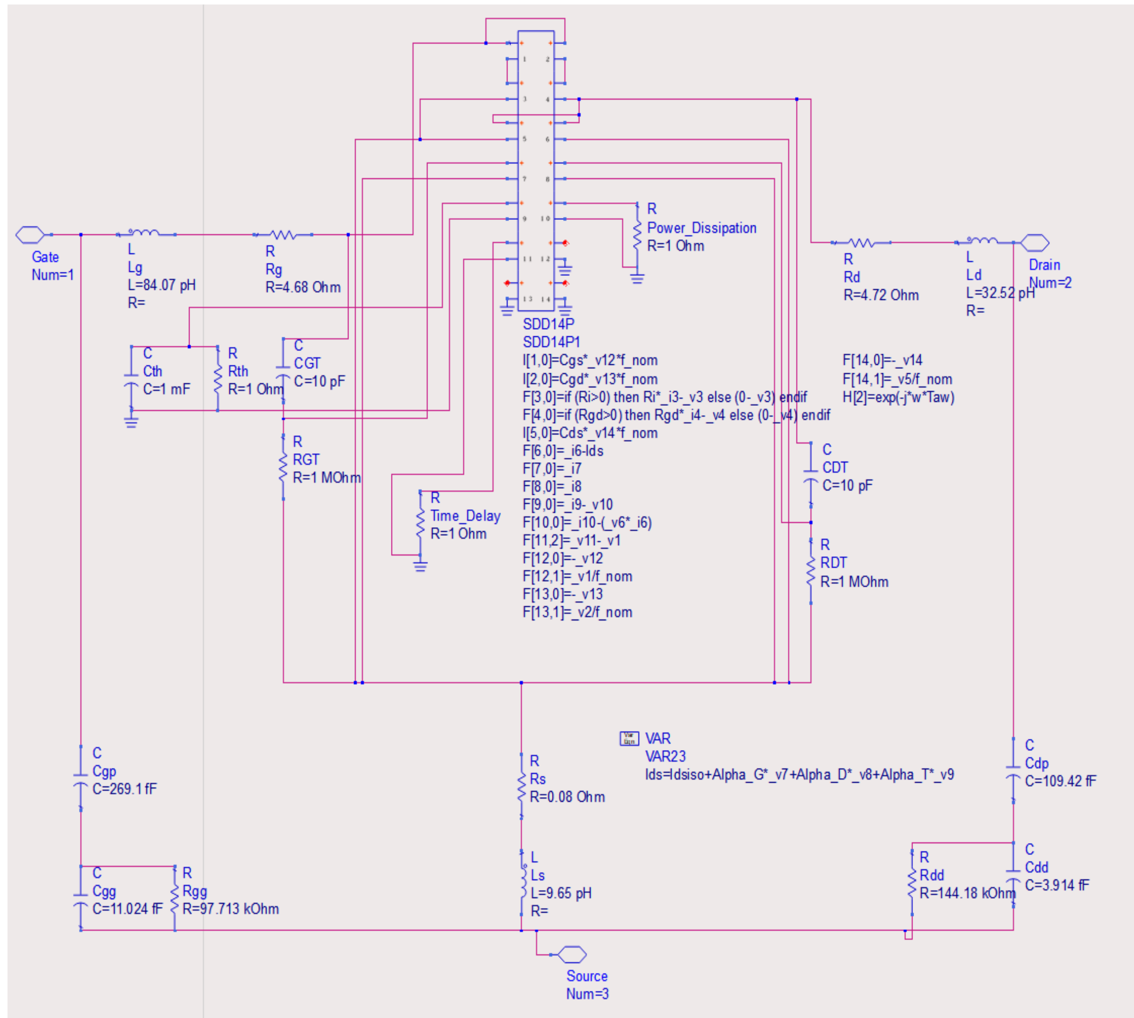


Figure 5.3 Full model in ADS for the case of GaN/D.

We can differentiate the voltages by using the weighting function “1” in Ports 12 – 14. For example, Port 1’s current is $C_{gs}\times$_v12$\times$fnom, where _v12 is the open-circuit voltage at port 12 and is differentiated using F[12,1].

Another interesting tool is that implicit representations can be used to generate useful expressions. For example, the power dissipation can be measured by multiplying the drain current and the drain voltage (as in port 10) and allowing the resultant current to flow through a one-Ohm resistance, which, in turn, saves the value of the power in that particular port voltage. This latter can be used in another port to perform certain tasks (i.e. thermal voltage measurements by port 9).

5.2 *S*-parameters simulations

To guarantee accurate large-signal simulations with respect to the measurements, it is necessary to guarantee accurate small-signal models. Figures 5.4 and 5.5 show the *S*-parameters extracted from the ADS model and compared to the measurements for GaN/D and GaN/SiC. As shown in the figures, simulated S_{11} and S_{12} parameters are very close to measurements. This is due to the fact that the input network of the model in ADS does not differ from that of the EC-SSM, hence the *S*-parameters should not differ [4][5]. S_{22} and S_{21} parameters are somewhat shifted due to the removal of G_{ds} and G_m [4][5]. The reason for such removal is that the large-signal drain current already takes into account channel length modulation and hence G_{ds} from the EC-SSM should be removed. Since the transconductance G_m is defined as the small-signal variations of the drain current to the small-signal input voltage variations, G_m from the EC-SSM must be neglected since it is, in an essence, part of the large-signal drain current expression. Due to the dependency of S_{21} on both the removed G_m and G_{ds}, the switching from the removed components to the large-signal drain current could cause discrepancies in S_{21} and S_{22} values.

Another point to discuss is that the models provide accurate results even on bias points that were not used in extracting the intrinsic parameters (e.g. V_{GS} = -1.5V and V_{GS} = -2.5V). This is due to the linear interpolator inside the DAC. We have not used cubic Spline interpolation because the number of bias points, from which we extracted the intrinsic part, were not sufficient; hence the Spline interpolation caused a huge error due to the large gaps in-between bias points. This issue was more apparent in GaN/D since *S*-parameters measurements at different bias points were much less than those measured for GaN/SiC.

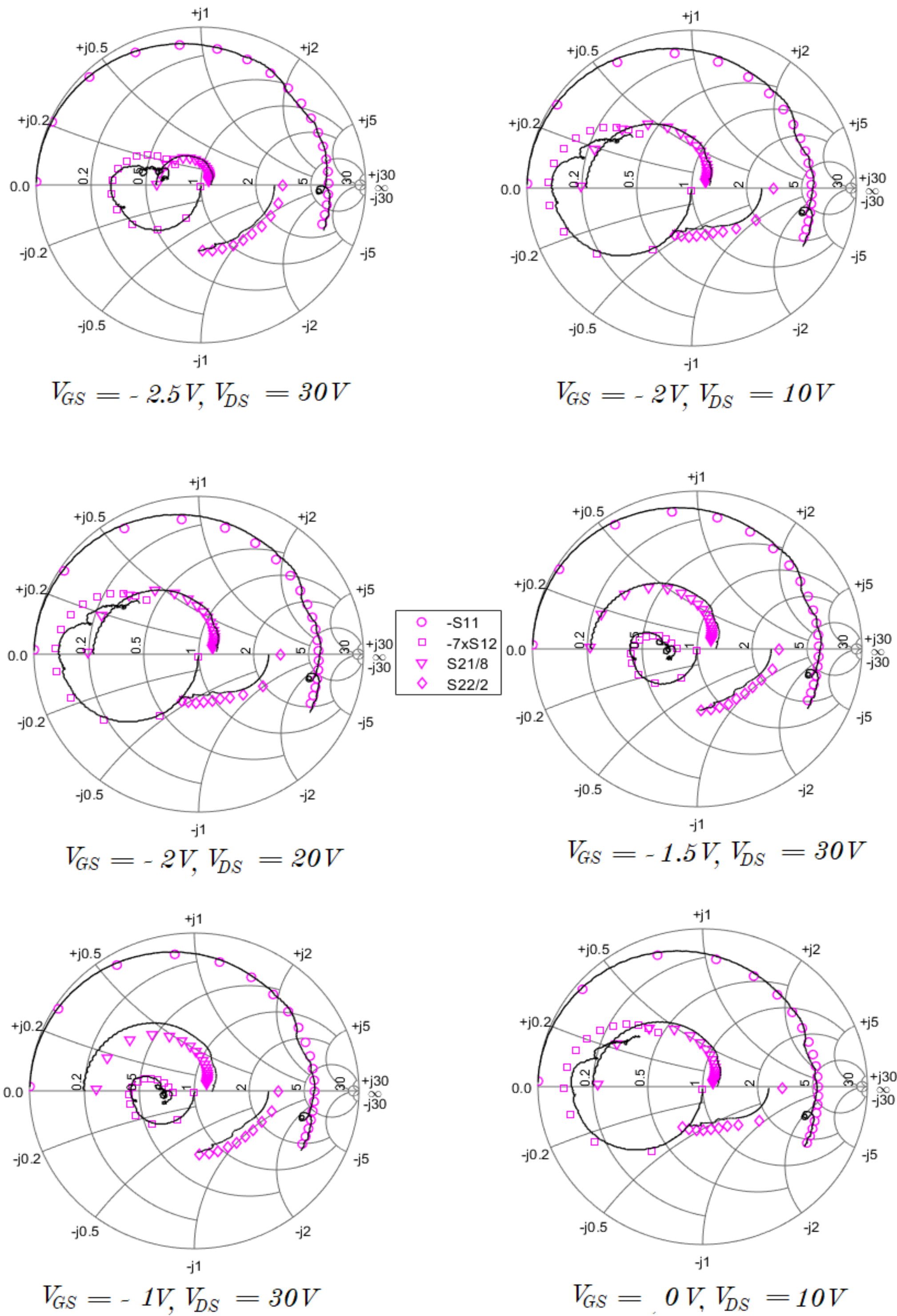


Figure 5.4 *S*-parameters simulations (symbols) using the model in ADS and compared with measurements (lines) of GaN/D at different bias points at frequencies from 0.1 GHz to 40 GHz.

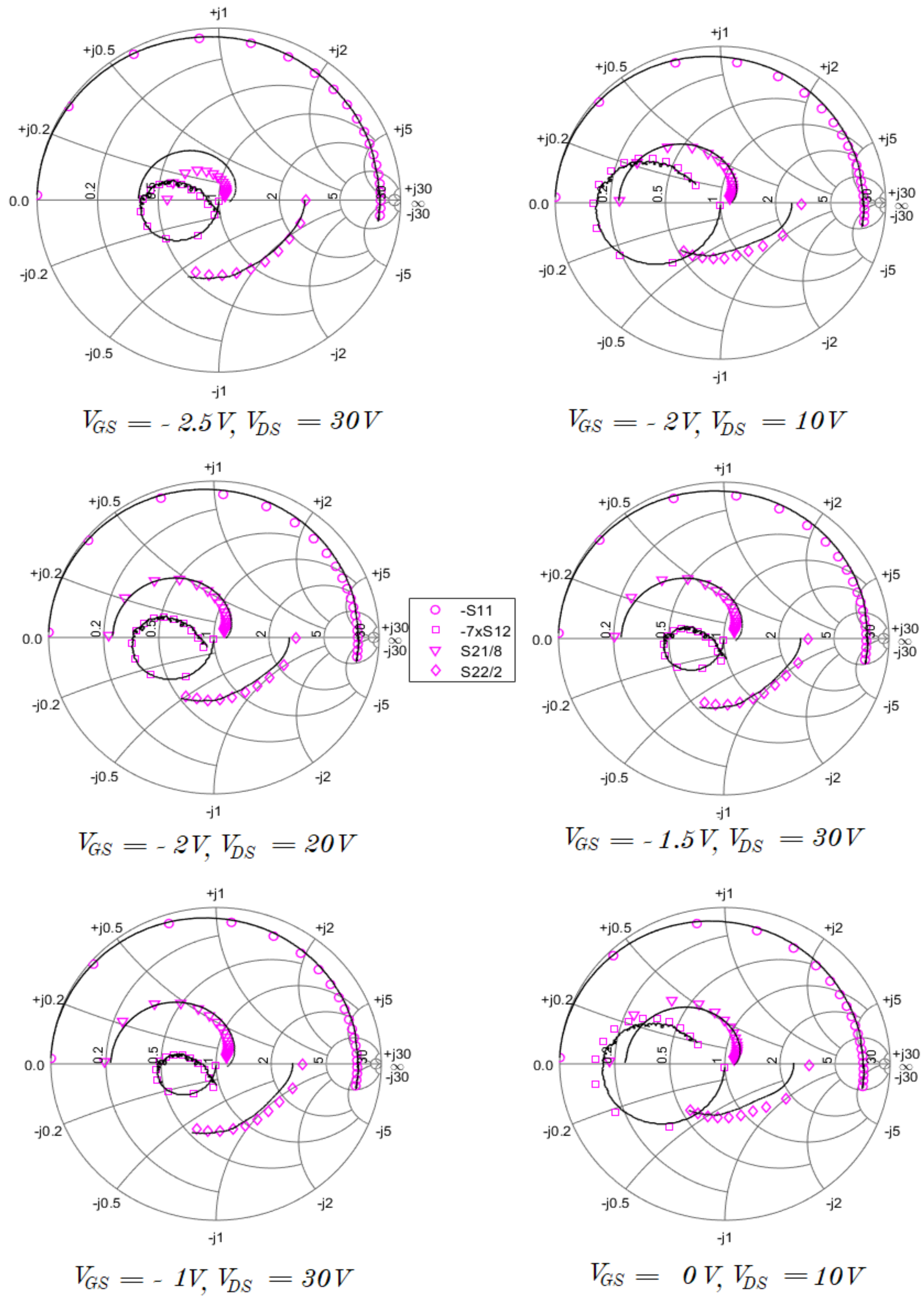


Figure 5.5 *S*-parameters simulations (symbols) using the model in ADS and compared with measurements (lines) of GaN/SiC at different bias points at frequencies from 0.1 GHz to 40 GHz.

5.3 Static IV-characteristics

Static IV-characteristics are very important in any transistor modeling. They are also very important in determining the quiescent bias points and the optimal load for designing PAs using load-lines. Since the EC-SSM was accurate in describing the parasitics of the device, the EC-LSM is needed to be accurate in describing the non-linear drain current and the current dispersion due to charge-trapping and self-heating effects. The model in ADS was configured to simulate the static IV-characteristics as shown in Figure 5.6 for both GaN/D and GaN/SiC. High accuracy has been achieved in saturation due to the empirical fitting of the charge-trapping and self-heating models using the Pulsed IV measurements. There are some errors in the linear region of the device attributed to the QPZD modeling approach and fitting errors from the pulsed IV measurements in the linear region. There are some errors as well when surpassing the highest measuring voltage in the pulsed IV measurements. These errors, however, were found to be small using a constant extrapolator in the DAC blocks used for extracting the fitting parameters related to current dispersion. It is not recommended, however, to work at voltages much higher than the measurements due to the inability of the extrapolator to accurately predict the device behavior beyond the measurement ranges.

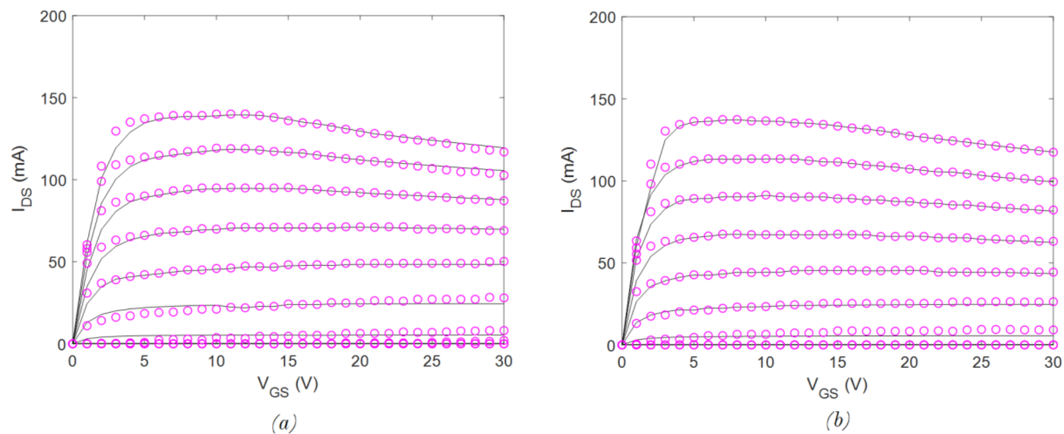


Figure 5.6 Static IV simulations (lines) using the model in ADS and compared with measurements (circles) for V_{GS} = -4 to 0V with a step of 0.4V, and V_{DS} = 0 to 30V using a step of 1V for (a) GaN/D and (b) GaN/SiC.

5.4 Single-tone Load-pull simulations

Simple LNAs are designed with input and output matching networks that match the input and output terminations to 50 Ω. This is used to maximize S_{21} and reduce S_{11} and S_{22}. In a PA, matching the output to 50 Ω is not efficient to deliver a large output power due to limitations on voltage swing and breakdown characteristics of the device. Hence load-pull measurements are done to match the load impedance depending on the harmonics generated by the device and the output impedance of the network. In this section, measured fundamental load impedances and source impedances from technical literature will be verified through load-pull simulations using the ADS models. Accurate results from the simulated fundamental load and source impedances with respect to measurements would guarantee the accuracy of the current at the fundamental and the output impedance network. Load-pull simulations for the ADS models are shown in Figure 5.7 at different frequencies and bias points. The source impedances were obtained from technical literature (from measurements at operating frequencies of 6 and 10 GHz). The source and load impedances at 2.4 GHz (frequency selected because of the future design of an amplifier for wireless Local Area Networking applications) were obtained via iterative approach by sweeping the input power and recording the PAE at each input power until finding the input that determines the optimal PAE. Table 5.1 shows a comparison between simulated and measured loads. It displays very close values indicating correct modeling of the currents at the fundamental frequencies and the output impedance.

Table 5.1 Comparison between load-pull simulations and measurements for both GaN/D and GaN/SiC at different frequencies and bias points.

Device	V_{GS} (V)	V_{DS} (V)	*Frequency (GHz)*	*Measured Z_s (Ω) [7]*	*Simulated Z_s (Ω)*	*Measured Z_l (Ω) [7]*	*Simulated Z_l (Ω)*
GaN/D	-2.15	20	6	22.45+j55.28	22.45+j55.28	108.21+j76.3	112.03+j76.75
	-2.15	20	10	9.7+j29.5	9.7+j29.5	71.34+j81.1	80.81+j84.9
	-2.5	28	10	9.7+j29.5	9.7+j29.5	47.65+j107.4	49.88+j95
GaN/SiC	-2.5	28	10	10.51+j21.18	10.51+j21.18	43.12+j98.23	49.88+j95

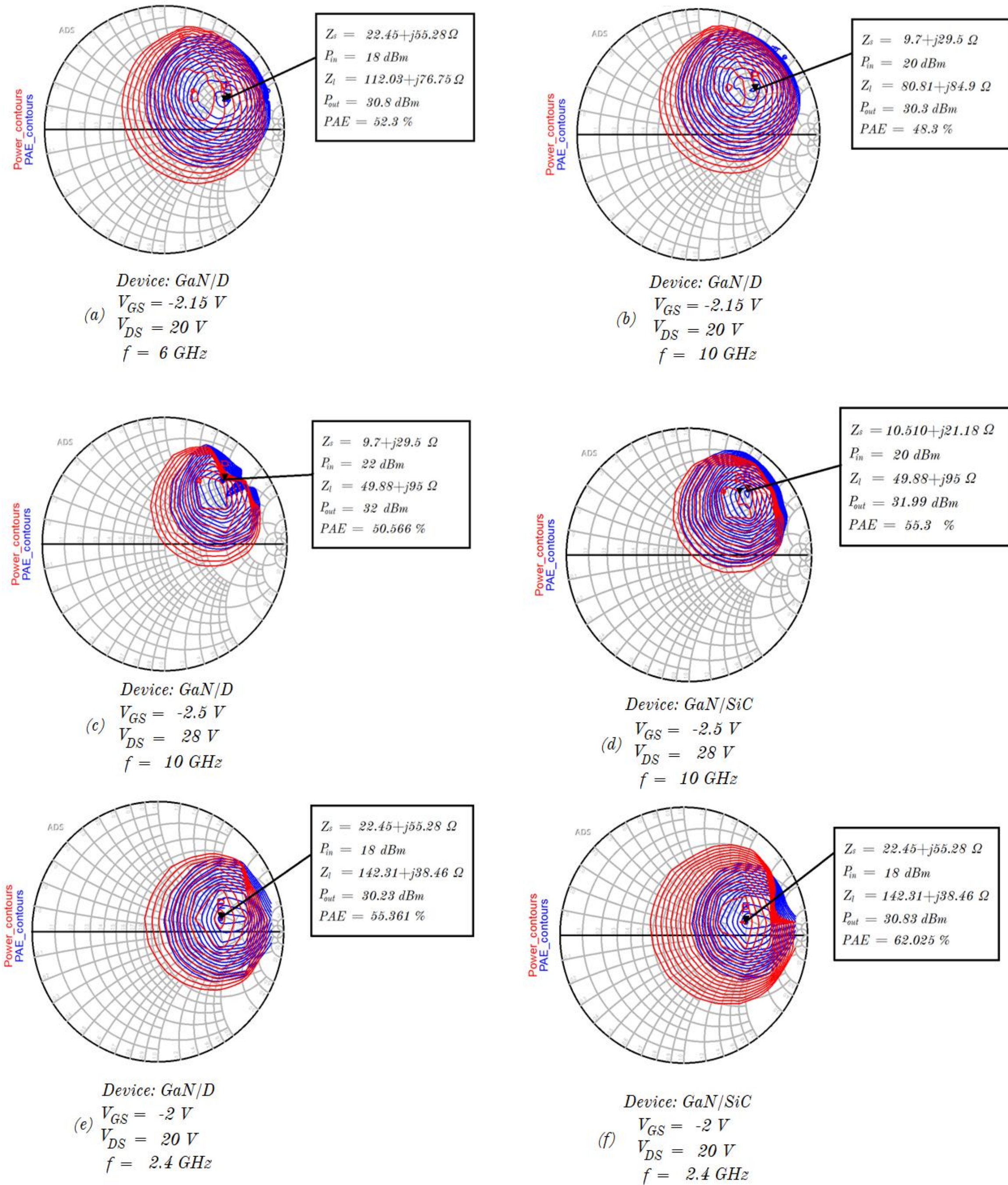
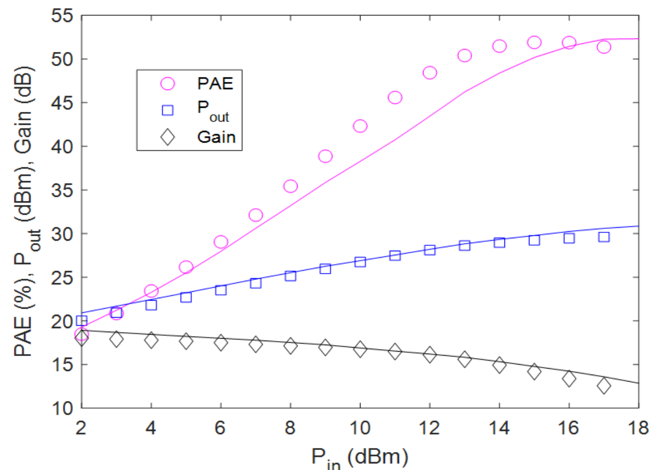


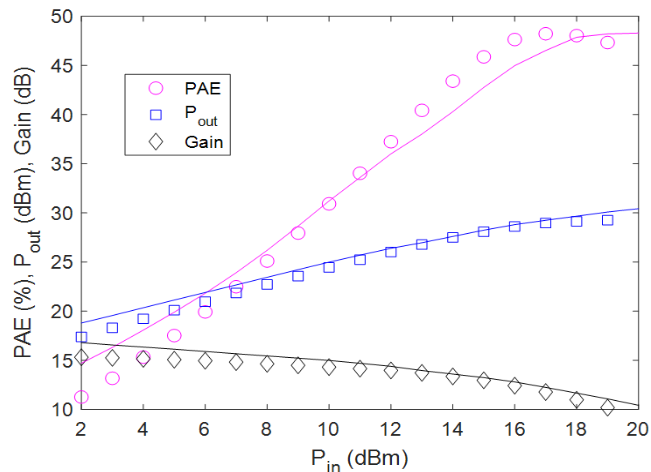
Figure 5.7 Load-pull simulations for both GaN/D and GaN/SiC at different bias-points and frequencies**.**

5.5 Single-tone input power-swept simulations

After determining the fundamental source and load impedances, we can sweep the input power and plot the output power, PAE, and the power gain at each swept value. This would allow us to determine at which point the output power would be compressed, enabling us to choose an input power that is not compressed while allowing an acceptable PAE. Figure 5.8 compares the large-signal characteristics between measurements and simulations for GaN/D.



(a)



(b)

Figure 5.8 Single-tone large-signal simulations (lines) and measurements (circles) for GaN/D at bias points of V_{GS} = -2.15V and V_{DS} = 20V at (a) 6 GHz and (b) 10 GHz.

We may notice from Figure 5.8 that the output power and the gain are very close to measurements. There are some discrepancies in the PAE, probably related to the poor sensitivity of the capacitances in the SDD block to harmonics. We were not able to simulate the large-signal characteristics at V_{GS} = -2.5V and V_{DS} = 28V (the bias points used in the reference [7] utilized for comparison). The currents at this bias point were extremely small for both devices, probably because they were not modeled appropriately in our large-signal model, causing inaccuracies at this particular bias point. Such limitations and possible solutions will be discussed in chapter 6.

A comparison between the single-tone large-signal characteristics of both GaN/D and GaN/SiC is shown in Figure 5.9. We may notice the superiority of the state-of-the-art GaN/SiC compared to GaN/D, especially in the PAE. As discussed in chapter 4, this is related to buffer-trapping effects due to the wafer transfer process of GaN/D, which reduces the PAE. This observation can be confirmed in [7]. Large-signal waves have been plotted for both GaN/D and GaN/SiC in Figure 5.10, showing the class AB operation at an uncompressed input power (12 dBm).

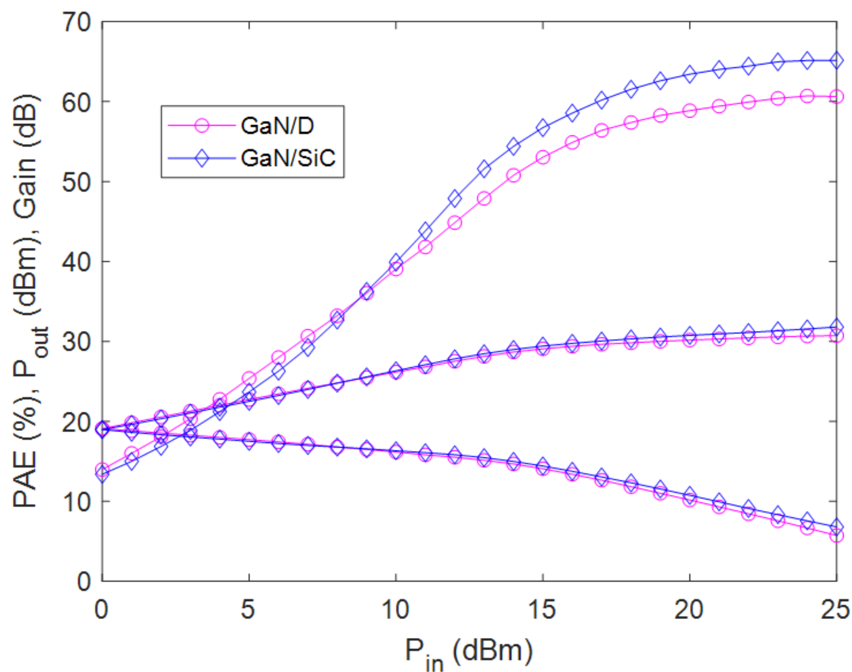
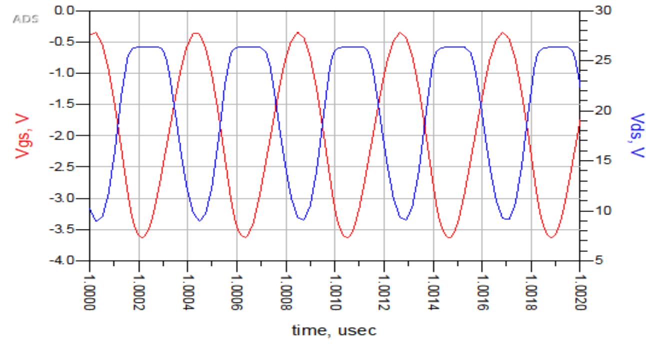
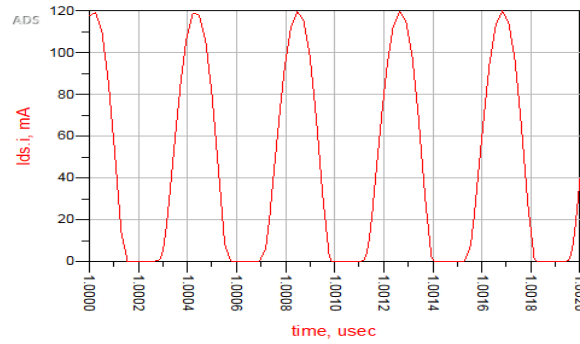
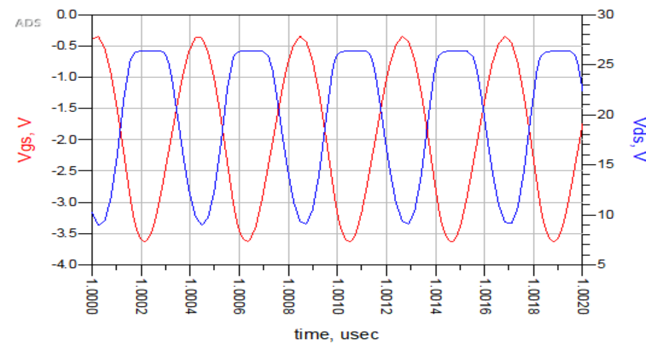


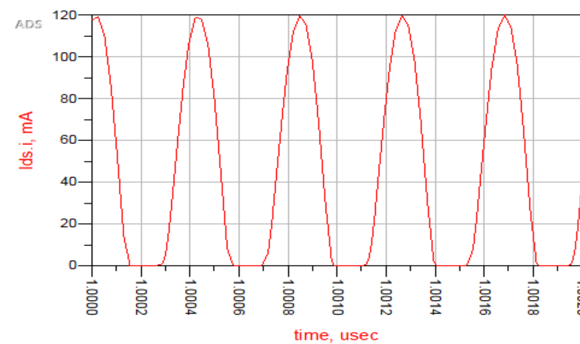
Figure 5.9 Single-tone large-signal simulations for both GaN/D (Magenta) and GaN/SiC (Purple) at a fundamental frequency of 2.4 GHz and bias voltages of V_{GS} = -2V and V_{DS} = 20.





(a)





(b)

Figure 5.10 Simulated large-signal waveforms for class AB at a frequency of 2.4 GHz with an input power of 12 dBm and bias voltages of V_{GS} = -2V and V_{DS} = 20V for (a) GaN/D and (b) GaN/SiC.

5.6 Conclusion

In this chapter, we developed an ADS model for both GaN/D and GaN/SiC in order to validate the work done on modeling the small- and large-signal characteristics of both devices. The ADS model was implemented using lumped components, Data Access Components, Variables and 14-port SDD block. The model is capable of describing the parasitics, current dispersion effects and the substrate choice for both devices. The intrinsic capacitances were implemented using the differentiation approach as appose to the integration method. The intrinsic resistances were implemented using conditional statements to remove negative values. The SDD block takes into account also the time delay used for high frequency dispersion in G_m, the self-heating effect on current dispersion by determining the instantaneous power dissipation, and charge-trapping effects by the RC branches at the input and output terminals. *S*-parameters simulations were conducted for both devices at different bias points, showing high accuracy with measurements available in the technical literature. The simulated static IV characteristics were also compared to measurements from the technical literature, showing high accuracy in the saturation region and slight discrepancies in the linear operating conditions. In order to verify single-tone optimal source and load impedance measurements, load-pull simulations were performed. The simulations provided close values to the data given in the literature, indicating accurate modeling of the fundamental source and load impedances. We also swept the input power and fixed the source/load impedances obtained from the single-tone load-pull simulations. This allowed us to plot the output power, PAE and the power gain vs. the input power for both devices. This gives us an indication at which input power the gain would be compressed allowing for different PA designs based on the application. Although high accuracy was obtained with the output power and the gain, PAE faced some inaccuracies, which could be due to the insensitivity of the differentiated voltages to the harmonics in ADS. We also compared single-tone large-signal simulations of both GaN/D and GaN/SiC, showing results that confirm those in the literature. It was obtained that even though GaN/D has superior thermal characteristics compared to GaN/SiC, it still suffers from buffer-trapping effects caused by the wafer transfer process, which leads to a reduction in the PAE.

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Chapter 6: Conclusions and Future Work

6.1 Conclusions from the research results

In this thesis work, a new small-signal extraction technique has been developed. It accurately describes the parasitics exhibited by small-scaled GaN HEMT devices regardless of the employed substrate. The extraction technique is based mainly on multiple important simplifications of the extrinsic network of the EC-SSM based on the range of frequencies at which the extraction occurs. The model has been validated and compared with measurements for GaN HEMTs on different substrates namely, Silicon Carbide, Diamond and Silicon. It was also tested for a completely different device structure namely, the Graphene-Based FET. Although different devices and/or substrates lead to different parasitics, they were described with high accuracy using only a single EC-SSM and a single extraction technique, which shows the superiority of the proposed extraction technique in automating the extrinsic parameters extraction of small-signal models.

Based on our results, it was found that Silicon Carbide substrates have very good matching with the GaN buffer, reflected by the extremely small parasitic conduction through the substrate. Silicon substrates, on the other hand, were found to have high parasitic conduction through the substrate, which indicated possible leakage current through the substrate. Diamond substrates showed low parasitic conduction through the substrate due to the high resistivity of Diamond; however, the extractor provided us with a converged value that could indicate possible buffer-trapping effects. All these observations were confirmed by the technical literature.

Large-signal modeling using Quasi-Physical Zone Division technique has been applied to both GaN/D and GaN/SiC to model the isothermal-trapping free current. High accuracy was achieved in modeling the linear region of both devices but failed at modeling the current-dispersion due to charge-trapping and self-heating effects. To solve this issue, an empirical model has been employed based on the Pulsed IV measurements. By extracting the fitting parameters for each non-ideal effect, we were able to study the causes behind current dispersion of both devices. The surface-trapping non-ideal effect

was found to be very similar for both devices due to the inclusion of a passivation layer near the gate surface. Buffer-trapping effects were found to be larger in GaN/D compared to GaN/SiC, which explains the reduction in the PAE induced by leakage current in the Diamond substrate. Self-heating effects were found to be direr in GaN/SiC compared to GaN/D, which is reasonable due to the high-temperature conductivity of Diamond substrates.

ADS models for both GaN/D and GaN/SiC have been implemented using Symbolically Defined Devices. The models were verified by simulating the small-signal *S*-parameters, large-signal IV characteristics, and single-tone load-pull. High accuracy was achieved compared to the measurement data available in the technical literature and obtained from fabricated devices.

6.2 Future work

Although the simulated results we obtained are mostly close to measurements, few simulations were not in par with our expectations. The drain current was not estimated correctly at very low gate-to-source voltages, which caused large errors in estimating the single-tone large-signal characteristics. A possible solution is to empirically fit the simulated drain current to the measurements at very low gate-to-source voltages while relying on the Quasi-Physical Zone Division technique to model the other gate-to-source voltages.

Another issue found is the insensitivity of the intrinsic capacitances to the harmonics in ADS, which caused few errors in estimating the single-tone input power-swept simulations. A revisit to intrinsic capacitances implementation as charge components could be a possible solution. Finding a way to estimate the initial charges existent within the device should be explored and studied in order to employ such a solution.

An observation highlighted in asymmetrical GaN/HEMTs is that the drain-to-source capacitance is very close to the gate-to-drain capacitance due to the large space between the gate and the drain, and the dominance of parasitics associated with the drain electrode. This observation can be used in creating a new direct extraction technique of the extrinsic parameters by assuming equal gate-to-drain and drain-to-source

capacitances. This will allow estimating accurately the pad capacitances and the gate-to-source capacitance without the scanning approach, which reduces the computational cost and improves the reliability of the extracted parameters.

In chapter 4, we were faced with inaccuracies in extracting the self-heating fitting parameters of GaN HEMT using pulsed and static IV measurements. The inaccuracies can be mitigated by employing a different electrothermal model that bases the self-heating effect on an actual thermal resistance extracted using a finite element method thermal analysis instead of relying on the normalized thermal resistance. This approach should reduce the correlation between the static IV measurements and the self-heating fitting parameter, which, in turn, will reduce the error pulses in the self-heating fitting parameter's map. This would give a better estimate for self-heating effects for both GaN/D and GaN/SiC.

Provided the improved self-heating model, the individual fitting parameters of surface-trapping, buffer-trapping and self-heating effects, can be used to produce an ADS model that takes into account each individual effect by itself with the isothermal trapping free current. This would allow simulating the large-signal characteristics of both GaN/D and GaN/SiC taking into consideration one effect at a time. This approach could provide important insights on which non-ideal effect is causing current dispersion and at which bias point it occurs. This can be used to optimize the design of power amplifiers by choosing the bias points that can provide the minimal current dispersion and hence, the optimal performance could be achieved. It could also be used to help in distinguishing the most troublesome non-ideal effect, which can be used to mitigate such an effect.

Appendix I: Relationships Between S- Z- and Y- parameters.

	S	Z	Y
S_{11}	S_{11}	$\frac{(Z_{11}-Z_o)(Z_{22}+Z_o)-Z_{12}Z_{21}}{(Z_{11}+Z_o)(Z_{22}+Z_o)-Z_{12}Z_{21}}$	$\frac{(Y_o-Y_{11})(Y_{22}+Y_o)+Y_{12}Y_{21}}{(Y_{11}+Y_o)(Y_{22}+Y_o)-Y_{12}Y_{21}}$
S_{12}	S_{12}	$\frac{2Z_{12}Z_o}{(Z_{11}+Z_o)(Z_{22}+Z_o)-Z_{12}Z_{21}}$	$\frac{-2Y_{12}Y_o}{(Y_{11}+Y_o)(Y_{22}+Y_o)-Y_{12}Y_{21}}$
S_{21}	S_{21}	$\frac{2Z_{21}Z_o}{(Z_{11}+Z_o)(Z_{22}+Z_o)-Z_{12}Z_{21}}$	$\frac{-2Y_{21}Y_o}{(Y_{11}+Y_o)(Y_{22}+Y_o)-Y_{12}Y_{21}}$
S_{22}	S_{22}	$\frac{(Z_{11}+Z_o)(Z_{22}-Z_o)-Z_{12}Z_{21}}{(Z_{11}+Z_o)(Z_{22}+Z_o)-Z_{12}Z_{21}}$	$\frac{(Y_o+Y_{11})(Y_o-Y_{22})+Y_{12}Y_{21}}{(Y_{11}+Y_o)(Y_{22}+Y_o)-Y_{12}Y_{21}}$
Z_{11}	$Z_o\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{11}	$\frac{Y_{22}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$
Z_{12}	$Z_o\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{12}	$\frac{-Y_{12}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$
Z_{21}	$Z_o\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{21}	$\frac{-Y_{21}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$
Z_{22}	$Z_o\frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}$	Z_{22}	$\frac{Y_{11}}{Y_{11}Y_{22}-Y_{12}Y_{21}}$
Y_{11}	$Y_o\frac{(1+S_{22})(1-S_{11})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{Z_{22}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$	Y_{11}
Y_{12}	$Y_o\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{-Z_{12}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$	Y_{12}
Y_{21}	$Y_o\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{-Z_{21}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$	Y_{21}
Y_{22}	$Y_o\frac{(1-S_{22})(1+S_{11})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}$	$\frac{Z_{11}}{Z_{11}Z_{22}-Z_{12}Z_{21}}$	Y_{22}

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