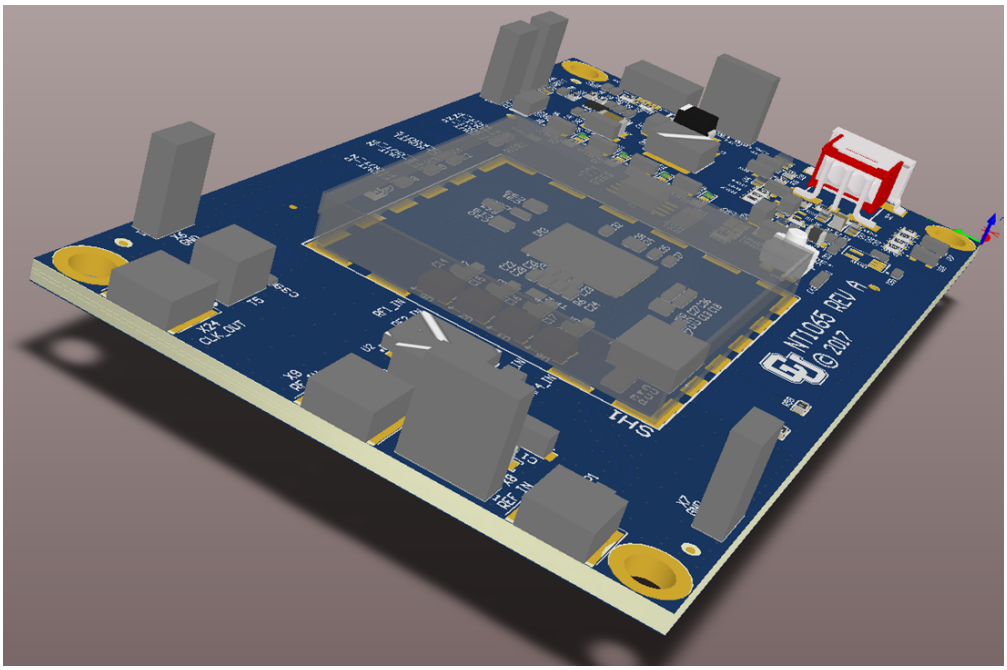
DEGREE PROJECT

New Generation 4-Channel GNSS Receiver

Design, Production, and Testing



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Space Engineering, master's level (120 credits)
2017

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Version Log	Issued by	Date
First version	Antoja, Guillem	Nov. 8, 2017

Abstract

Due to the current research needs and the lack of commercial multi-channel, multi-constellation GNSS receivers, a two-board solution has been developed so it can be mated with and take advantage of the processing power of the FPGA board branded as MicroZed.

In order to achieve the proposed goals, an initial phase for assessing and updating the older design, building, and testing of SiGe modules (including both the electronics and casings) has been carried out. The results included demonstrate performances at logging GPS-L1 data with similar C/N_0 and AGC values as the previous versions of the modules and offering navigation solutions with accuracies of a few meters. Secondly, a first iteration and design proposal for the new generation receiver has been proposed for GPS and GLONASS L1 and L2, which has been manufactured and tested. Partial tests have been performed due to the flaws of the current revision of the MicroZed Board in regards to its communication peripherals, and the results have validated the receiver's design provided certain modifications are considered for future iterations. Furthermore, voltage and frequency tests have provided results with an error of less than 7%, and signal tests have provided C/N_0 values similar to those of the SiGe modules of around 47[dB-Hz] which will be a useful baseline for future iterations. Finally, a design proposal for an Interface Board used between the older NT1065_PMOD Board and other FPGA boards carrying the standardized FMC connectors has been added to the report and negotiations with manufacturers have been engaged.

Acknowledgments

First and foremost, I would like to thank Prof. Akos for the opportunity of working with him and his team at CU Boulder, for his guidance during the project, and for all the support he offered out of the project that made moving to and living in Boulder a much more pleasant and comfortable experience.

Secondly, I'm also thankful to the rest of Prof. Akos' team and in particular Dr. Shivaramaiah, with whom I've worked the most during the project, for all the help and kindness.

Next, I would like to appreciate the help from my examiner in Luleå, Per Lindgren.

And last, but not least, I would also like to thank my family, who made it all possible and have always supported me.

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Abbreviations

ADC	Analog to Digital Converter
AGC	Automatic Gain Control
AMS	Agile Mixed Signaling
ASIC	Application-Specific Integrated-Circuit
BPSK	Binary Phase-Shift Keying
BeiDou	BeiDoü Navigation Satellite System
BOC	Binary Offset Carrier
BOM	Bill of Materials
CCAR	Colorado Center for Astrodynamics Research
CC-M	GLONASS Central Clock
CDMA	Code Division Multiple Access
DC	Direct Current
DIP	Dual In-line Package
EEPROM	Electrically Erasable Programmable Read-Only Memory
EoL	End of Life
FDMA	Frequency Division Multiple Access
FPGA	Field-Programmable Gate Array
GEO	Geostationary Earth Orbit
GLONASS	Globalnaya Navigazionnaya Sputnikovaya Sistema
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GS	Ground Segment
HPC	High Pin Count
IF	Intermediate Frequency
IO	Input/Output
ITLL	Integrated Teaching & Learning Laboratory
LED	Light-Emitting Diode
LEO	Low Earth Orbit
LNA	Low Noise Amplifier
LoS	Line of Sight
LPC	Low Pin Count
LVDS	Low Voltage Differential Signal
MCS	Master Control Station
MEO	Medium Earth Orbit
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MS	Monitoring and Measuring Station
NAVSTAR	Navigation System with Timing and Ranging
NGA	National Geo-Intelligence Agency
NUDET	Nuclear Detonation
OCX	Operational Control System
OS	Operating System
PCB	Printed Circuit Board
PID	Product ID (identification)
PMOD	Peripheral Module
PR	Pseudo Random

QPSK	Quadrature Phase Shift Keying
RAAN	Right Ascension of the Ascending Node
RAM	Random Access Memory
RF	Radio Frequency
SAESD	Smead Aerospace Engineering Science Department
SAR	Search and Rescue
SAW	Surface Acoustic Wave
SCC	System Control Center
SD	Secure Digital
SLR	Laser Ranging Stations
SNR	Signal to Noise Ratio
SS	Space Segment
TCXO	Temperature Compensated Crystal Oscillator
TMBOC	Time-Multiplexed BOC
TT&C	Telemetry, Tracking, and Command
UART	Universal Asynchronous Receiver/Transmitter
ULS	Mission Uplink Station
USB	Universal Serial Bus
USNDS	United States NUDET Detection System
VID	Vendor ID (identification)
VITA	VMEbus International Trade Association
WWI	World War I
WWII	World War II

1. Introduction

Throughout history, navigation has played an important role in many different areas, such as exploration, commerce, and warfare. The very initial techniques included determining one's position by observing the stars and using maps and specific tools. However, in the 20th century, new technologies were developed which allowed for a greater degree of automation while also increasing the accuracy of the results; this was the beginning of Radio Frequency (RF) navigation. Many different ground-based systems were used, each an evolution of the previous one, but the latest step in development brought the systems to space. As this newer version of RF navigation was then satellite-based, it was known as Global Navigation Satellite System (GNSS).

Currently there are many companies and organization with working GNSS receivers for the most popular constellations and services. However, solutions are mostly compatible with only one of the systems, usually either Global Positioning System (GPS) or *Глобальная навигационная спутниковая система* (Russian for *Global Navigation Satellite System* or GLONASS), and sometimes even a combination of two systems this time also including *北斗卫星导航系统* (simplified Chinese for *BeiDoü Navigation Satellite System* or only BeiDou) and the new (under development) Galileo and BeiDou-2 to the list. Nonetheless, some companies have brought their new dual-frequency (or 2-channel), multi-band, multi-constellation to the market, such as Swift Navigation and their Piksi Multi GNSS Module[1] which includes an FPGA for data processing and is currently one of the most advanced solutions. Another close alternative to this module would be the NT1065_USB3[2] developed by NTLab, which is a 4-channel, multi-band, multi-constellation evaluation board for their NT1065 "Nomada", this time without a processing FPGA but instead a USB3 for forwarding the data. Lastly, there are organizations such as Virginia Polytechnic Institute and State University, and Miami University among many others that are currently developing their own multi-channel, multi-band, multi-constellation GNSS receivers.

Taking into consideration the aforementioned state of the art solutions and organizations developing newer receivers, a collaboration project with the GNSS Lab[3] at the Smead Aerospace Engineering Science Department (SAESD) in Colorado University Boulder (from now on CU Boulder) in order to design and build a new generation receiver in close relationship with the Colorado Center for Astrodynamics Research (CCAR), also hosted by the SAESD. This receiver will be an evolution of a previous front-end used by the research group, and will include four RF channels and compatibility with any combination of GNSS constellations and bands, with components carefully chosen so that they can be easily replaced without having to alter the design. Furthermore, the processing side of the receiver will also experience a quite important optimization, as the front-end will be able to be stacked with the new MicroZed Board, a powerful credit card-sized FPGA board. It should be noted, though, that this project will be the first design iteration so the receiver will be designed to be compatible with GPS-L1, GPS-L2, GLONASS-L1, and GLONASS-L2 mainly due to the fact that these are the most common services of the only two fully operational GNSS constellations with worldwide coverage. Furthermore, this design project will be the

[1] Swift Navigation's Piksi Multi website: https://www.swiftnav.com/piksi-multi
[2] NTLab's NT1065_USB3 board description: http://ntlab.com/IP/NT1065/NT1065_USB3_description_v1.04.pdf
[3] GNSS Lab at CCAR in CU Boulder website: https://ccar.colorado.edu/gnss/

first step towards a more advanced solution, this time including both the GNSS front-end and the required components from the FPGA board into a single board so costs and dimensions can be optimized.

Therefore, this report will first include a background study of the different RF navigation technologies where, in regards to GNSS, special emphasis will be put on GPS and GLONASS as these will be the ones included in the initial design proposed by this project. Secondly, *"Phase 1: The SiGe Module*" will be described as a get-to-know phase, where an older GNSS data sampler will be revised and brought back to a production stage. Next, the core of the project will be introduced and explained in detail under the title of "*Phase 2: The New Generation Receiver*". In this chapter, a brief description of previous solutions used at CU Boulder will be included followed by an elaborated motivation for this new design and a detailed explanation of both the process and parts involved in the project. Afterwards, "*Phase 3: Additional Work*" will comprise an additional board which does not fit in any of the previous phases but has also been designed during this project. Finally, supplementary material regarding the design and production files of the different phases will be added in the form of annexures.

Additionally, several pieces of software will be used during the execution of this project. The core element will be Altium Designer[4], which is the electronic design software used by the members of the GNSS Lab, which allows not only to design the schematics but also the component and board layouts as well as performing simulations and obtaining 3D models and all the files required for production. Furthermore, for designing mechanical pieces such as module housings, the software of choice will be Siemens NX[5]. In this case, the selection has completely been an individual decision motivated by personal expertise. Lastly, the CyConsole[6] by Cypress Semiconductor will be used in order to program the modules built during Phase 1, as this piece of software has been specifically designed and provided for facilitating the programming of these modules' core processor.

As a final note for this introductory chapter and regarding the methodology followed during the practical part of the project, each phase will begin with a specific background study, be it either previous design files or guidelines, component datasheets, and data from alternative solutions in the market. Next, the design (or revision in the case of the first phase) activities will be engaged. In that regard, component availability and specifications will be checked for the SiGe modules, whereas a block-based design will be carried out for the other two phases. Said block-based design will mainly consist on studying the different technologies that can be successfully implemented for different parts of the board along with an analysis and electronic design of all the associated components for each individual block of the board (such as the oscillator, the core ASIC, the power supply, and so on). The layout design that follows will be outsourced and, once all production files are ready, manufacturers will be contacted for quoting and building the boards. During the production stage, the experiments for testing the boards will be designed accordingly to the TLR of the phase, which will then be executed. These tests will range from simple programmability and performance tests for the SiGe modules to complete voltage and frequency tests on critical parts of the circuitry and further performance tests for the New Generation Receiver, always comparing the results to those obtained from previous versions of the board or from the datasheets, as well as comparing the final performance with online tools in order to verify the satellites IDs that have been detected and the navigation solutions.

[4] Altium Design website: http://www.altium.com/altium-designer/overview

[5] Siemens NX website: https://www.plm.automation.siemens.com/en/products/nx/

[6] CyConsole website: http://www.cypress.com/documentation/software-and-drivers/suiteusb-34-usb-development-tools-visual-studio

2. Background

2.1 History

RF navigation systems are based on performing measurements over the signals transmitted by strategically positioned stations, said measurement being primarily regarding the direction of an incoming beam (either by bearing, phase, or interferometry), the distance the signal has traveled from the transmitter (mostly by time-of-travel), and the velocity at which the target or user is moving (Doppler shift of the received signal). There have been many different RF navigation systems throughout history, which can be classified as Bearing-Measurement Systems, Beam Systems, Transponder Systems, Hyperbolic Systems, and Satellite-based Systems.

The first type, the Bearing-Measurement Navigation Systems, was developed and used from before World War I (WWI) to the 1960s. Although there are many different variants of this systems, one of the most relevant and early ones is the Radio Direction Finding, which used a rotating directive antenna in order to determine the incoming direction of multiple RF beams, which then where used to triangulate the receiver position. Another example, which happens to be an evolution of the previous one, is the Reverse Radio Direction Finding, in which the rotating antenna was placed on the ground in order to simplify the onboard receivers and which would transmit the station's ID in Morse code. One more variant would be the Automatic Direction Finder, similar to the original Radio Direction Finding but adding phase comparison thanks to receiving with multiple antennas, also with the re-introduction of Non-Directional Beacons at low and medium frequency which removed the Line of Sight (LoS) restriction of the system. As a final version, the Very High Frequency Omnidirectional Range introduced many changes to the Reverse Radio Direction Finding systems, such as omnidirectionally broadcasting the Morse-coded station ID along with a continuous signal, and a directive signal rotating at 30[rmp].

The second kind of navigation systems that has been mentioned above are the Beam Systems, which were used especially before World War II (WWII). They are characterized by being especially simple on the receiver side and their operation consisted in keeping the receiver centered in an RF beam so multiple beams broadcasted by different stations may create the track to be followed by the receiver. The first of this kind was the Lorenz System, developed by the homonym German company after WWI, and it consisted in transmitting audio signals on two directive beams which overlapped by a bit, so the users could position themselves right where the beams overlapped by listening to the audio of both channels. A second version of Beam System could be the Low Frequency Radio Range, used between WWI and WWII during both en route navigation and instrument approach procedures (maneuvers for transitioning between instrumental flight to visual flight). The Low Frequency Radio Range was based on having a set of stations between airports that would have four antennas transmitting to in four cardinal directions. Furthermore, the signals transmitted by each antenna were two Lorenz beams Morse-coded with "short-long" and "long-short" respectively, so once the receiver was properly positioned in the beam overlap a steady tone would be perceived. The last example of Beam System could be the Instrument Landing System Localizer which is still used nowadays and provides planes with horizontal and vertical positioning, distance to the landing runway, and additional airport data.

Thirdly, the Transponder Systems are another kind of positioning and navigation system developed before WWII, and based on distance determination via radar. The simplest version of Transponder Systems would

be to use a transponder in order to reply to the signal received from a scanning radar in order to measure distances from objects, which would highly increase the accuracy of using previously described systems such as the Lorenz System by measuring the time between transmission and reception (including both a known transducer delay and the time-of-travel). In addition, a Lorenz beam may be added for horizontal positioning while keeping the transducer for ranging in order to improve the long-distance accuracy. Moreover, other versions would use multiple stations, each with its own frequency so ground control could estimate the transponder's (usually mounted on a plane) position by triangulation. One last example of transponder-based navigation system could be the Distance Measuring Equipment System developed in the early 40s and which mostly improved the electronics from the previously described system, which allowed further automation and included some changes in the pulses transmitted. Each of the operators of this system had available a specific pulsed code in order to prevent ambiguity. Finally, Distance Measuring Equipment Systems have traditionally been allocated next to Very High Frequency Omnidirectional Range systems, which provide both angle and distance estimations.

The next type of RF navigation system from the list above are the Hyperbolic Systems, introduced during WWII, and which main benefit was not needing transponders that replied to the messages broadcasted by the ground stations thanks to being able to determine a position solution by using any number of hyperbolic lines in space. Although there are many different examples of Hyperbolic Systems, below a brief description of three of them has been included, namely Gee, Decca, and LORAN-C. Regarding Gee, it was the first ever hyperbolic system, developed by the United Kingdom during WWII. Gee users could determine the distance to multiple transmitting stations over hyperbolic lines by knowing the fixed transmission delays and the time of arrival of the different pulsed signals. The second system, Decca, was another British system similar to Gee, but in this case instead of pulsed signals, the stations would transmit continuous signals with delayed phases, making it easier to display and requiring much simpler electronics. Lastly, LORAN-C (standing for long range navigation version 3) was being developed in 1952 by the US as an evolution of the original LORAN (similar to Gee but at much lower frequencies), with the main characteristic of combining Gee's pulse delays with Decca's phase delays at rather low frequencies. Although LORAN-C was much more complex than the previous alternative systems, electronics miniaturization greatly benefitted this system becoming this way one of the most popular ones until the introduction of GNSS.

Once the first satellite was launched (Sputnik in 1957), development was focused on new navigation systems, this time satellite-based. The first system of this kind was Transit, deployed in the 60s by the US, which allowed users to obtain accurate positioning data thanks to analyzing the Doppler shift of signals broadcasted at a certain frequency by satellites orbiting fixed and known orbits (set of low polar orbits at approximately 1,100[km]). Afterwards, there have been many different satellite-based systems, some offering regional coverage and some others offering worldwide coverage. GPS (US) and GLONASS (RU) are the only global satellite-based navigation systems which are fully functional, even though both are undergoing a modernization and updating process, whereas Galileo (EU) and BeiDou-2 (CN) are being developed and implemented, and they are both expected to be fully operational in 2020. Therefore, bearing in mind that only GPS and GLONASS are currently fully operational at the time of writing this document, their history has been detailed in the following subchapters.

2.1.1 GPS

After the military success of Transit in the 60s and with the reliable and accurate navigation needs for the American submarine-launched ballistic missiles, strategic bombers, and intercontinental ballistic missiles during the Cold War, the US government started working on a new generation of GNSS first known as Defense Navigation Satellite System but soon rebranded to Navigation System with Timing and Ranging (NAVSTAR), most commonly known simply as GPS. Although it is usually mentioned that the program's design began in 1973 during a meeting held by military officers in Labor Day Weekend, there are evidences that the design phase was engaged before that year, such as articles discussed in the aforementioned meeting like "Low-Altitude Navigation Satellite System" (by R.B. Kershner of the Johns Hopkins Applied Physics Laboratory), "Mid-Altitude Navigation Satellites" (by R.L. Easton of the U.S. Naval Research Laboratory), and "Satellite Systems for Navigation using 24-Hour Orbits" (by J.B. Woodward, W.C. Melton & R.L. Dutcher, of the Aerospace Corporation)[7].

The first 10 GPS satellites (model Block I) were launched between 1978 and 1985[8], and provided service for military applications but, after the Korean Air Lines Flight 007 was shot down in 1983 due to flying over USSR's prohibited airspace by mistake[9], US president Ronald Reagan stated the plans for GPS including civilian services and further signed an executive order in 1983[10]. The next generation of GPS satellites began with the launch of the first Block II in 1989, and it took five years to fully deploy the 24 vehicles. This newer constellation provided for the first time civilian service, which was originally degraded in terms of accuracy due to fear of US enemies using it for their advantage.

A few years after becoming fully operational, additional needs were foreseen and so a modernization process was announced. This modernization affected both the military and the civilian services, and its implementation started with Block IIR(M), a modernized version of the legacy Block IIR, followed with the current Block IIF and the future Block III, always keeping compatibility with the legacy services and the ones introduced by previous modernized versions. The first step of this modernization process was to remove the selective availability (for which civilian precision was forcedly lower than the military) as techniques for both increasing civilian signal accuracy (such as differential GPS) and denning GPS service over specific areas had been developed. Secondly, a service rework was done, with which both signal characteristics like forward error correction and new services such as additional civilian and a modernized military signals on GPS-L2 or a Safety-of-Life (SoL) service on GPS-L5 (find more information about the GPS signals in chapter *2.2.1 GPS*). During the modernization process, also the ground segment has been being upgraded with a newer operational control system by Raytheon. The process for the control center is currently undergoing phase two out of three, where Block III satellites launch and verification and capabilities of the civil GPS-L2 have already been included, the migration from the old control system to

[7] Easton, Roger L., McCaskill, Thomas B., "*Defense Navigation Satellite Systems Proposed Prior to GPS*", *Proceedings of the 55th Annual Meeting of The Institute of Navigation (1999)*, Cambridge, MA, June 1999, pp. 57-61.
[8] Hegarty, Christopher J., Chatre, Eric, "*Evolution of the Global Navigation SatelliteSystem (GNSS)*", *Proceedings of the IEEE*, Vol. 96, No. 12, December 2008, pp. 1902-1917.
[9] International Civil Aviation Organization, "*ICAO Completes Fact-Finding Investigation - PIO 8/93 Revised*", Montreal: ICAO, June 16th 1993.
[10] "*Statement by Deputy Press Secretary Speakes on the Soviet Attack on a Korean Civilian Airliner*", extracted from reaganlibrary.archives.gov, September 16, 1983.

the new is expected to be Ready to Transition to Operations in 2019, and additional navigation signals, such as the civil GPS-L1 and GPS-L5, will be supported, monitored, and controlled in the near future[11].

2.1.2 GLONASS

The Russian navigation system GLONASS was born in 1957 from the research of potential applications of radio-astronomy techniques, in particular for aero-navigation. Its first soviet ancestor was the Low Earth Orbit (LEO) *Tsiklon*, developed in the early 60s, and having a total of 31 satellites launched between 1967 and 1978 with the main goal of providing ballistic missile submarines with accurate enough position fixes. Shortly after the first launch, though, development efforts were already placed in improving the design of a part of the system, known as *Parus*, and the whole modified version of *Tsiklon* became *Tsiklon-B*. *Parus* consisted of a six-plane constellation and usually had one active satellite (with additional spare ones) per plane, which had a nominal lifetime between 1.5 and 2 years, resulting in around 100 satellite launches between 1974 and 2010. Furthermore, and in order to complement the new *Parus* military system with civilian services, another system was developed after the first *Parus* flight test in 1974, the civilian *Tsikada*. With most of the development being done for *Parus*, it took no more than two years until the first satellite was placed in orbit for flight tests, and in 1978 the deployment of operational four-plane constellation (again each orbital plane with at least one operational satellite and one spare) of satellites with similar lifetime as *Parus*.

Nonetheless, these newly developed systems took too much time in order to establish a position fix (the order of minutes), and so they could only be used with stationary or slowly moving targets. Therefore, a set of system requirements was prepared and basic research performed in the early 70s, establishing this way the foundation of GLONASS. Later in 1978, the system design was complete, leading to flight tests three years later and a preliminary 10- 12-satellite constellation in 1984. GLONASS was completely operational with a 24-satellite constellation with three orbital planes. As a final note, it is worth mentioning that although GLONASS was conceived as an alternative and competition for the more popular American GPS, it has been often used in conjunction with GPS by many receivers in order to either complement or serve as backup.

2.2 System Structure

GNSS are, as the name suggests, satellite-based navigation systems and, therefore, they share the same structure as any other space system. These systems are composed of a Space (SS) and a Ground Segment (GS). In this subchapter, a description of these two segments can be found as well as their most relevant agents or parts, focusing on GPS' modernized form and GLONASS.

[11] "*PE 0603423F / Global Positioning System III - Operational Control Segment*", Project 67A021 / OCX, US Air Force, February 2015.

2.2.1 GPS

2.2.1.1 Space Segment

The SS consists of all the elements of the system allocated outside the Earth's atmosphere, which are mostly the Space Vehicles (SV) or satellites. Nonetheless, GPS signals have been included in this section because they have their origin in space.

2.2.1.1.1 Signals

GPS satellites have five different RF bands assigned, each of them for different particular applications and, as mentioned in chapter *2.2.1 GPS*, they system being based on Code Division Multiple Access (CDMA), meaning that all satellites transmit a specific service at the same frequency and time, but using a satellite-specific code. A brief description of each band and its services has been detailed in the subchapters below.

2.2.1.1.1.1 GPS-L1

GPS-L1 is the most commonly used for navigation purposes, it offers four different services, and it is characterized for broadcasting code-multiplexed signals In-Phase or Quadrature at a central frequency of 1,575.42[MHz] depending on the service.

The first service is L1 – Coarse Acquisition (C/A) and is one of the Quadrature civil signals in L1. Modulated by a BPSK(1), it uses 1,023-chip long Gold Codes at a 1.023[MHz] frequency which identify the SV that broadcasted the signal, and has a total data rate of 50[bps] / 50[sps] (bits per second and symbols per second respectively).

Another Quadrature civil signal is L1 – L1C, which is modulated by a TMBOC(6,1,1/11) characterized by two sub-carriers, one at 1.023[MHz] and another at 6.138[MHz]. In this case, the codes used are Weil Codes, with a total length of 10,230 chips per main sequence and 1,800 chips per secondary sequence, and a code frequency of 1.023[MHz]. Last but not least, this service has a data rate of 50[bps] / 100[sps].

Regarding the military services, the first one is the L1 – P(Y) Code, also known as Encrypted Precision Code, and is transmitted In-Phase. It is modulated on a BPSK(10) with a data rate of 50[bps] / 50[sps], and is based on an encryption of a 37-week long code composed of $2x10^{14}$ chips, thus having a code frequency of 10.23[MHz]. Each of the SV has a specific week of the total code assigned, which relates to the SV's ID and is repeated every 7 days.

Finally, the second military service offered in L1 is the L1 – M-Code, which had been designed for military purposes only and is expected to replace the P(Y) code. The improved jamming resistance relies on basically allowing a higher power transmission without interfering with the C/A or P(Y) codes, thanks to allocating most of the energy at the sides of the band[12]. Although little has been disclosed about this service, it is known that it uses a $BOC_{sin}(10,5)$ modulation with a sub-carrier frequency of 10.23[MHz] and a code frequency of 5.115[MHz].

[12] Barker, Brian C., Betz, John W., Clark, John E., Correia, Jeffrey T., Gillis, James T., Lazar, Steven, Rehborn, Kaysi A., Straton, John R., "*Overview of the GPS M Code Signal*", *Proceedings of the 2000 National Technical Meeting of The Institute of Navigation*, Anaheim, CA, January 2000, pp. 542-549.

2.2.1.1.1.2 GPS-L2

Similarly to the GPS L1 band, the L2 band is used for providing four services, the main difference being that the center frequency is in this case 1,227.60[MHz], but the same In-Phase and Quadrature signal structure using CDMA is used.

The first two services are the civil L2 – L2CM and L2 – L2CL, both in Quadrature, and they are multiplexed onto a BPSK(1) at 1.023[MHz]. The codes they are based on are Moderate (10,230 chips) and Long (767,250 chips) Ranging Codes, both types with a code frequency of 511.5[kHz]. Thanks to this multiplexed signals which add redundancy, it is possible for L2 – L2C to improve the accuracy of navigation with an easy to track signal especially in case of localized interferences.

The two remaining services are L2 – P(Y) and L2 – M-Code, which are basically the same as those in L1 but in this case at a different frequency band. For more information about these services refer to the point above *2.2.1.1.1.1 GPS-L1*.

2.2.1.1.1.3 GPS-L3

The GPS L3 band has a center frequency of 1,381.05[MHz] and is nowadays no longer being used. Nonetheless, its original usage was providing a communication link for the US Nuclear Detonation (NUDET) Detection System (USNDS), which could provide near real-time worldwide, highly survivable capability to detect, locate, and report any nuclear detonations or other high-energy infrared events in the Earth's atmosphere or in near space[13].

2.2.1.1.1.4 GPS-L4

Contrarily to GPS L3, L4 (center frequency of 1,379.913[MHz]) wasn't originally used, and technically it still isn't in the modernized version of GPS, but it is being studied for additional ionospheric correction, which could improve GPS accuracy.

2.2.1.1.1.5 GPS-L5

The lowest frequency band GPS uses is L5, centered at 1,176.45[MHz] and, similarly to L1 and L2, it uses an In-Phase and Quadrature signal modulation. The main service provided over this band is the SoL service (data transferred In-Phase and pilots in Quadrature), which is a safety service for aviation that features higher power, greater bandwidth, and more advanced signal design. Regarding the technical specifications of the signals, both signals are modulated over a BPSK(10) and use codes obtained by combination and short-cycling of M-sequences. Said codes have a frequency of 10.23[MHz] and a length of 10,230 chips. As one last detail about this service and in order to benefit the most from it, it may be used in combination with L1 – C/A and L2 – L2C, resulting in a technique called trilaning that enables sub-meter accuracies without augmentations, and very long range operations with augmentations.

[13] "*PE 0305913F: NUDET Detection System (Space)*", Project 672808 / Nuc Detonation Det Sys (sensors), US Air Force, February 2012.

2.2.1.1.2 Constellation and Space Vehicles

The GPS constellation consist of 32 satellites orbiting a set of six orbital planes (see *Figure 1: GPS constellation*), which ensures that at any point in time and anywhere on Earth a receiver would be able to get the signals of at least 4 GPS satellites, which allows it to obtain its coordinates. Regarding the orbits in particular, those are characterized for being approximately circular, being Medium Earth Orbit (MEO) with an altitude above sea level of 20,200[km], having an inclination of 55° and a 60° separation between Right Ascension of the Ascending Node (RAAN). Moreover, this orbits allow the SVs to pass over the same point on Earth's surface twice a day, which is also beneficial for some military applications among others.

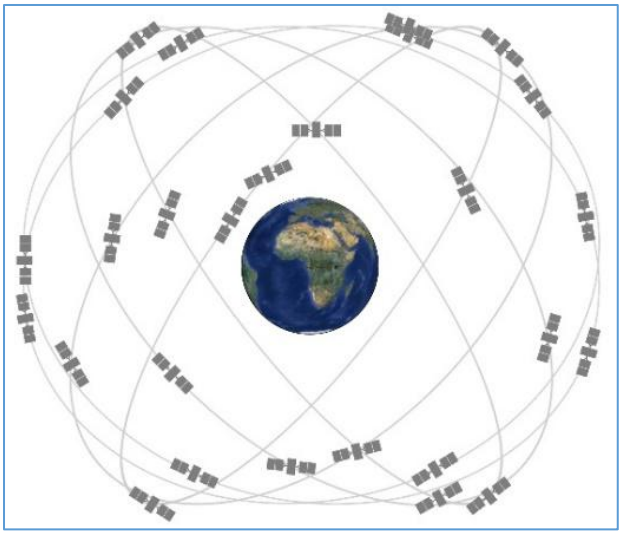

Figure 1: GPS constellation

In regards to the SVs, as mentioned before, the constellation is formed by 32 satellites, 30 of which are active, but these vehicles are not all the same. Instead, there are three different types of SV being used and one being developed, asides from one of the legacy types which is obsolete. There are, from oldest to newest, 11 operational Block IIR, 7 Block IIR(M), and 12 Block IIF.

Regarding the Block IIR, they were launched between 1997 and 2004 and they were renewed versions of the older Block IIA so the latter could be replaced after their End of Life (EoL). Since they were essentially the same as the previous version, they also broadcasted L1 – Coarse Acquisition, L1 – P(Y), and L2 – P(Y), and they had a similar lifespan of about 7 years and a half. Considering their launch date, they are already approaching their expandable EoL, being the latest decommission for satellite E6 on May 5, 2017.

The next generation were Block IIR(M) satellites, launched between 2005 and 2009 and, as an evolution (M standing for modernized) of Block IIR, they offered some additional signals such as a second civil one in L2 (L2 – L2C) and a new military one with increased jamming resistance, the L1 – M-Code. Furthermore, they also provided flexible power levels for military signals, although the lifespan had not been improved.

The 4th GPS satellite generation is known as Block IIF. These satellites broadcasted the same signals as the previous generations, with the addition of a third civil signal, the L5 – Safety-of-Life. These have been launched since 2010, and they also provide other performance improvements such as more advanced atomic clocks, improved accuracy, signal strength, and quality while increasing the life span for the first time since Block IIA.

Finally, the new GPS III is considered to be ready for launch in 2017 and will add a civil signal to L1, enhance the signal reliability, accuracy, and integrity, and even increasing the life span by approximately 3 years.

2.2.1.2 Ground Segment

The GS comprises all the elements which are, as the name suggests, on the ground. In the case of GPS, these elements are a Master Control Station (MCS), the Monitoring and Measuring Stations (MS), and the Ground Antennas (see *Figure 2: GPS Ground Segment*).

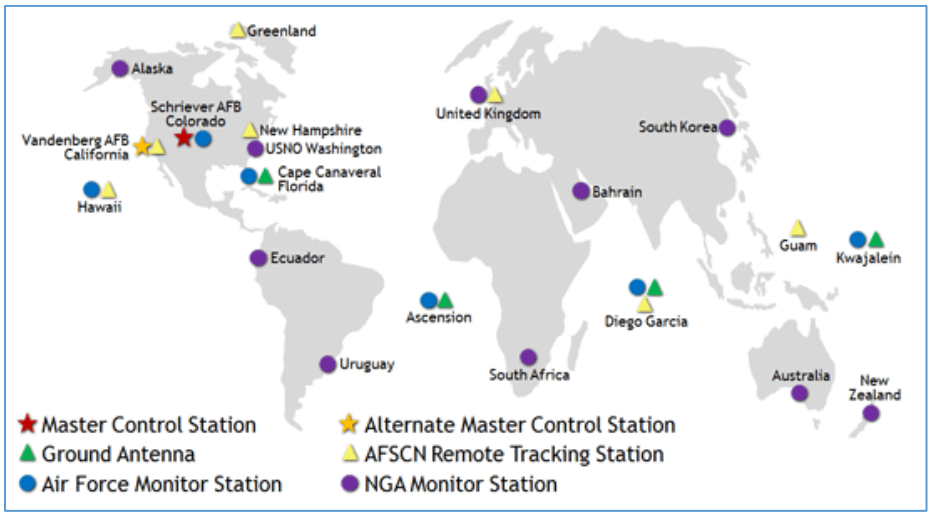

Figure 2: GPS Ground Segment

The MCS is at the Schriever Air Force Base, Colorado, where the 2nd Space Operations Squadron commands and controls the GPS constellation. The main tasks performed there are generation and upload of navigation messages as well as ensuring the proper operation and accuracy of the GPS constellation. Furthermore, the MCS also receives navigation information form the MS, which is used to track the different satellite positions in orbit so their orbital distribution can be modified in case of failure in order to maintain an optimum service. It should also be noted that there is an Alternate MCS, this one in Vandenberg Air Force Base, which used to be the main one originally now serves as redundancy.

Secondly, regarding the MS, there is a total of 15 located throughout the world. The first 6 are from the Air Force and the other 9 are from the National Geospatial-Intelligence Agency (NGA). The main goal of such stations is to track the SV as they orbit above them and report the collected data (including not only the downlink messages themselves but also atmospheric data and other signal measurements) to the MCS.

The third element that has been mentioned as part of the ground segment are the Ground Antennas. These are the elements that allow communication with the satellites and they support S-Band frequencies. There are two kinds of antennas, GPS dedicated and shared. The GPS dedicated antennas are only 4, and they are located at Kwajalein (Marshall Islands), Ascension Island (Saint Helena, Ascension and Tristan da Cunha), Diego Garcia (British Indian Ocean Territory), and Cape Canaveral (US). The remaining 7 antennas are shared with the Air Force Satellite Control Network (AFSCN), which are remote tracking stations located throughout the globe and help increasing communication windows with satellites as well as improving tracking capabilities.

Lastly, it is worth mentioning that the GS is undergoing a modernization process by implementing the next generation Operational Control System (OCX) which will, among others, provide improved cybersecurity and resilience in managing both civil and military navigation signals and the different GPS satellite families.

2.2.2 GLONASS

2.2.2.1 Space Segment

Similarly to GPS, GLONASS' SS comprises those elements outside the Earth's atmosphere, namely the SV, but signals have also been included.

2.2.2.1.1 Signals

GLONASS is a double-band system, meaning that its services are found in two different bands: L1, and L2; and mentioned in chapter *2.1.2 GLONASS*, it traditionally used Frequency-Division Multiple Access (FDMA) for its services. Nonetheless, the usage of CDMA was disclosed in 2008[14] for the already existing bands and 2 additional ones: L3 (already being implemented by some SVs) and L5. The following subchapters contain more information regarding each of the bands and their signals.

2.2.2.1.1.1 GLONASS-L1

The highest frequency band used by GLONASS is L1, with its center frequency at 1,602[MHz]. It is important to notice that although the constellation has 24 nominally operating satellites, in order to both optimize the amount of frequency channels and at the same time comply with the CCIR Recommendation 769, GLONASS has been using a maximum of 15 channels since 2005, where each channel's center frequency is calculated by:

$$f_{k_{L1}} = f_{0_{L1}} + k\Delta f_{L1}$$

Where:

- k: frequency channel number.
- $f_{0_{L1}}$: 1,602[MHz].
- Δf_{L1}: 562.5[kHz].

This is possible because, as can be seen in the figure below (see *Figure 3: Antipodal assignment of GLONASS satellites*, where the displayed parameters have the form i(k), "i" standing for satellite almanac slot, and "k" being the frequency channel number), satellites occupying antipodal slots may use the same frequency as they will never be seen at the same time by any ground user.

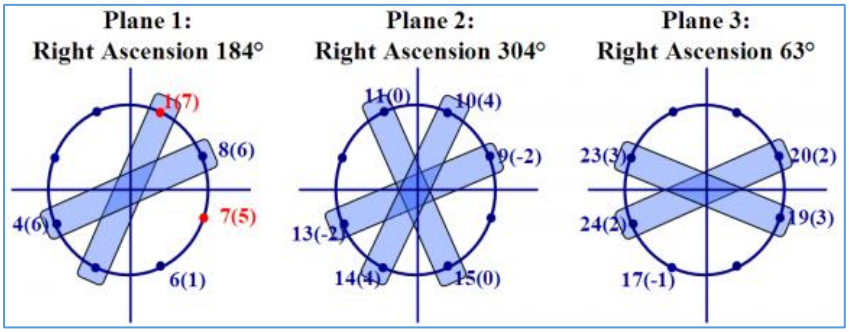

Figure 3: Antipodal assignment of GLONASS satellites

Regarding the different services provided in L1, satellites broadcast both an open signal known as Standard Precision (SP) or L1OF ("O" meaning *открытый* or *open*, and "F" meaning FDMA), and an

[14] Gibbons, G., "*Russia Approves CDMA Signals for GLONASS, Discussing Common Signal Design*", *Inside GNSS*, April 28, 2008.

obfuscated signal also known as High Precision (HP) or L1SF ("S" meaning *зашифрованный* or *encrypted*, and again "F" meaning FDMA).

L1OF is characterized by using a BPSK(0.511), an M-sequence Pseudo Random (PR) code for all satellites with a frequency of 511[kHz], a Meander sequence of 1,000[Hz] which Modulo-2 addition with the PR code is used to modulate the signal, and a data rate of 50[bps]. The L1SF, on the other hand, uses a BPSK(5.11), meaning the undisclosed PR code has a frequency of 5.11[MHz], and it is transmitted In-Quadrature (phased by 90°) of the L1OF.

As a side note and as a consequence of GLONASS' modernization, newer satellites (from GLONASS-K2 launched since 2015) have started including CDMA-compatible payloads. These newer SV additionally offer the same L1 services originally broadcasted in FDMA, but in CDMA, thus becoming L1OC and L1SC (the "C" logically meaning CDMA). The new services have a center frequency of 1,600.995[MHz], and they use Time-Division Multiplexing in order to send the pilot and data signals, with a BOC(1,1) and BPSK(1) respectively for L1OC, and a BOC(5,2.5) both for L1SC. Finally, another service is being developed for L1 which is expected to be provided by GLONASS-KM vehicles in 2025, L1OCM. It is an interoperable CDMA signal based on the same frequencies and format as GPS-L1 – L1C (see chapter *2.2.1.1.1.1 GPS-L1* for information on GPS-L1) that uses a BOC(1,1) modulation.

2.2.2.1.1.2 GLONASS-L2

Similarly to GLONASS-L1, L2 has a 15-channel frequency setup (see chapter *2.2.2.1.1.1 GLONASS-L1* for more details), but in this case the center frequency is 1,246[MHz] and each channel's center frequency is obtained by the following expression:

$$f_{k_{L2}} = f_{0_{L2}} + k\Delta f_{L2}$$

Where:

- k: frequency channel number.
- $f_{0_{L2}}$: 1,246[MHz].
- Δf_{L2}: 437.5[kHz].

GLONASS-L2 services are the same as those for L1, receiving the names L2OF and L2SF, meaning L2 open FDMA (for Standard Precision) and encrypted FDMA (for High Precision) respectively. Furthermore, these two services are transmitted with a 90° difference in phase, being L2OF In-Phase and L2SF In-Quadrature.

As mentioned above, L2 services are identical to L1's ones but with a different carrier frequency. Therefore, L2OF is again characterized by a data rate of 50[bps], a BPSK(0.511) signal modulation, an M-sequence code with a frequency of 0.511[MHz], and a Meander sequence of 100[Hz], the last two being combined by the Modulo-2 addition and further used to modulate the signal. In regards to the High Precision signal, the L2SF, its known specifications (it should be kept in mind that not all specs are available to the public) are also the same as the ones from L1SF, having a BPSK(5.11) modulation and a PR code frequency of 5.11[MHz], which is kept private.

In addition to the traditional FDMA signals and alike GLONASS-L1, CDMA services over GLONASS-L2 are being developed and implemented, starting with GLONASS-K2 launches in 2015, which included a CDMA-compatible payload. These CDMA services on GLONASS-L2 are the L2OC (open or Standard Precision

CDMA) and the L2SC (encrypted or High Precision CDMA), both using a carrier frequency of 1,248.06[MHz]. The public service known as L2OC uses Time-Division Multiplexing so both data and pilot signals can be transmitted over the same medium, which are modulated with a BPSK(1) and a BOC(1,1) respectively. On the other hand, the encrypted service known as L2SC has its data and pilots modulated by a BOC(5,2.5), and it is broadcasted In-Quadrature in respect to the public services.

2.2.2.1.1.3 GLONASS-L3

GLONASS-L3 is a CDMA-only band that provides the service L3OC (open or Standard Precision CDMA) with a carrier frequency of 1,202.025[MHz] and a bandwidth of 20.46[MHz] which was first tested in February 2011[15]. In more detail, the signal is modulated by a QPSK, where the data is In-Quadrature and the pilots are In-Phase, and has a total chip rate of 10.23[Mcps]. About the codes used, GLONASS-L3 uses ranging codes based upon Kasami sequences with a length of 214-1 symbols which are truncated at 10,230 symbols, where each symbols lasts for 10 chips and each chips has a duration of 10[ms]. Additionally, secondary codes with 1[ms] per symbol are used for both data and pilots, these being a 5-bit Barker code (00010) and a 10-bit Neuman-Hoffman code (0000110101) respectively.

In a similar way as in other GNSS systems, new services for GLONASS-L3 are being developed, namely the L3SC and the L3OCM, which are expected to be available by 2025. Regarding the L3SC (encrypted or High Precision CDMA), it will be an encrypted version of the L3OC, meaning that the codes will be private so only authorized users may take advantage of this service. Secondly, the L3OCM will be a modernized and interoperable CDMA signal, which will use a BPSK(10) modulation centered at 1,207.14[MHz] and will be similar to the Galileo/COMPASS E5b signal in order to improve multiple GNSS interoperability.

2.2.2.1.1.4 GLONASS-L5

Efforts are being put onto developing another GLONASS service which is compatible with other GNSS so easier and cheaper implementation of multi-standard GNSS receivers is possible. One of such services in L5 is L5OCM (meaning Open CDMA Modernized), which is expected to be provided by GLONASS-KM satellites from 2025, will be very similar in specifications to the GPS-L5 and Galileo/COMPASS E5a, will use a BPSK(10) modulation, and will have a carrier frequency at 1,176.45[MHz]. Similarly to GPS-L5, the main goal of this new frequency band and its signals is to provide a SoL service, which will mostly be used by the aviation sector.

[15] Thoelert, S., S. Erker, J. Furthner, M. Meurer, G. X. Gao, L. Heng, Walter, and P. Enge, "*First Signal in Space Analysis of GLONASS K-1*", *Proceedings of ION ITM 2011*, Portland, OR, September 2011, pp. 3076-3082, 2011.

2.2.2.1.2 Constellation and Space Vehicles

Figure 4: GLONASS constellation

GLONASS's satellite constellation (see *Figure 4: GLONASS constellation*) consists, as of summer 2017, of 27 vehicles, of which 24 are operational. The 3 unused SV are either under check by the Prime Contractor, spare satellites in case of another one failing, or in in-flight tests phase. These satellites are orbiting a set of 3 orbital planes, all with an inclination of 64° 8', an altitude of 19,140[km] and a separation between their respective RAANs of 120°.

Regarding the SV themselves, only 2 out of the 4 different generations are operative nowadays, being Generation Zero prototypes and having all First Generation (Block IIa, IIb, and IIv) satellites been decommissioned before 1989. Out of the 27 in-orbit SV, the active ones are 23 belonging to the Second Generation and 1 to the Third Generation. Regarding the 3 non-operative satellites, the spare one and the one under maintenance are from the Second Generation, whereas the one being tested belongs to the Third Generation.

Second Generation satellites, also known as GLONASS-M, Urugan-M or simply M, were developed from the 90s and put in orbit after 2003. These satellites provided substantial improvements regarding the propulsion subsystem and clock stability, which allowed at its turn an increase of lifetime. Another important upgrading over the previous generation is that these newer satellites broadcast a second civil signal on G2 frequency band which allows ionospheric refraction cancelation. It is also worth mentioning that one of the GLONASS-M vehicles are capable of transmitting CDMA signals in GLONASS – L3, which originally was only intended for the Third Generation.

GLONASS-K is the name Third Generation SVs receive. The main changes these propose over the previous versions are an additional CDMA-capable payload, an increased lifetime, a clock stability improvement of an order of magnitude, and a weight reduction of almost a half compared to GLONASS-M, allowing twin launches.

Finally, a newer version of the GLONASS-K is being developed and expected to fly by 2025, the GLONASS-KM. It will feature CDMA-compatible payloads capable of offering modernized and interoperable signals on L1, L3, and L5 as well as all legacy signals.

2.2.2.2 Ground Segment

GLONASS' GS consists of the different elements required for the system to nominally operate which are on Earth's surface, namely the System Control Center (SCC), the Telemetry, Tracking, and Command Centers (TT&C) and Upload Stations (ULS), the Central Clock (CC-M), the Laser Ranging Stations (SLR), and the MS (see *Figure 5: GLONASS Ground Segment*, where red is for the SCC, yellow other operative centers, and green facilities available in the future).

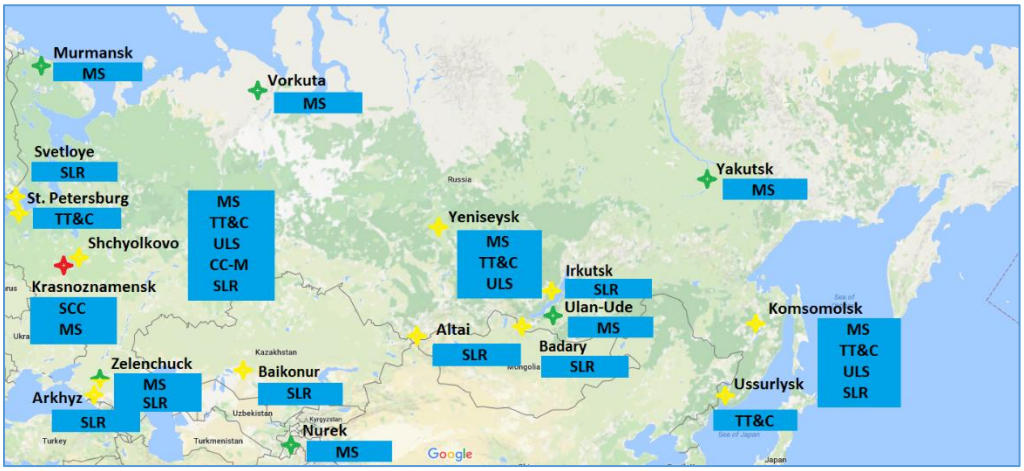

Figure 5: GLONASS Ground Segment

The core of the GS is the SCC, located at Krasnoznamensk, which main goal is to control the constellation as well as each individual satellite as it coordinates all different functions and it processes the gathered information in order to determine satellite clocks, orbits, and updates their navigation messages.

The second element mentioned above are the TT&C Centers. GLONASS has 5 of them located in Russia, in particular at Shchyolkovo, Komsomolsk, St. Petersburg, Ussuriysk, and Yeniseysk. Their main purpose is to track GLONASS satellites in view and log ranging data and telemetry from their signals, which is then forwarded to the SCC where it is processed. Two of this centers, in particular the ones at Shchyolkovo and Komsomolsk, have Mission Uplink Stations (ULS), which receive data from the SCC that has to be uploaded to the satellites, such as basic commands, navigation message updates, etc.

Regarding the system clock, a reference time is kept at Shchyolkovo at the CC-M, which is used by the SCC to compare with the onboard clocks and can be obtained thanks to the correction terms transmitted by the system.

The next element of GLONASS' GS are the eight SLR which are part of the Russian Laser Tracking Network and are located at Svetloye, Shchyolkovo, Zelenchuck, Arkhyz, Zmeinogorsk (Altai Krai), Badary, Irkutsk, and Komsomolsk-na-Amure, and a mobile one used at Baikonur as of 2014[16]. They are provided with three different optical channels: ranging, angular measurement, and photometric. The ranging channel is mostly used as a single source of calibration data for SV ephemeris determination, which is useful for also provide support for the estimation of accuracy and calibration of RF means for orbit measurements, for monitoring the on-board clocks, and applying the data for operational control of GLONASS time and ephemeris data thanks to their geodetic-class RF navigation receivers connected to hydrogen maser

[16] Shargorodsky, V., "*Russian laser station network and the plan for network expansion*", GGOS Bureau on Networks and Communication (BNC) Meeting, Viena, AT, April 30, 2014.

frequency standards, providing the geodetic base for GLONASS reference frame, and finally for providing declared values of the ephemeris precision as well as computation and forwarding of accuracy factor in the navigation frame. Regarding the angular measurement channel, it provides data for implementing a single-point flight control for geostationary satellites by performing periodical orbit inclination measurements. Lastly, the photometric channel is used for registering flight phases during highly elliptical and geostationary orbits (such as engines turn-on), and for attitude stability and determining the motion of a SV relatively to its center of mass.

The last GS element are the MS, of which 4 conform a network located throughout Russian territory (namely at Krasnoznamensk, Shchyolkovo, Yeniseysk, and Komsomolsk) and 6 others were planned to start operating both in Russia and nearby states (in particular in Murmansk, Zelenchuck, Vorkuta, Nurek, Ulan-Ude, and Yakutsk) after 2010[17]. These monitoring and measuring stations are very similar to TT&C Centers in functionality and are sometimes even located in the same place. The have as main objectives to perform measurements on the RF signals received from the SVs, and they also include some parameter analysis.

2.3 Applications

The main application for GNSS is that for which they are designed: to provide a ground user (or any inside the atmosphere) with precise location coordinates. This may be achieved by applying the trilateration method (see *Figure 6: Trilateration method*) for which at least signals from at least four different satellites (although it may be implemented at a lower scale with transmitting stations instead) shall be received, and both the data contained in the messages (transmission time, ephemeris, satellite ID in the form of freq. or code, etc.) and their physical parameters (frequency, phase, Doppler, etc.) shall be analyzed. The way trilateration works is that with the first satellite signal, a sphere of possible locations is set around that particular SV. Next, the second signal is used for setting another sphere of positions around the second SV, which intersects with the first one and thus narrows down the amount of potential locations. Similarly to the previous cases, the third signal is also use to generate a sphere of locations around the third satellite, which intersects with the last selection and thus results in an ambiguity of only two points. The fourth signal (again by generating a sphere around the SV) assists with calculating a time and local correction that will determine which of the two remaining points is the actual position.

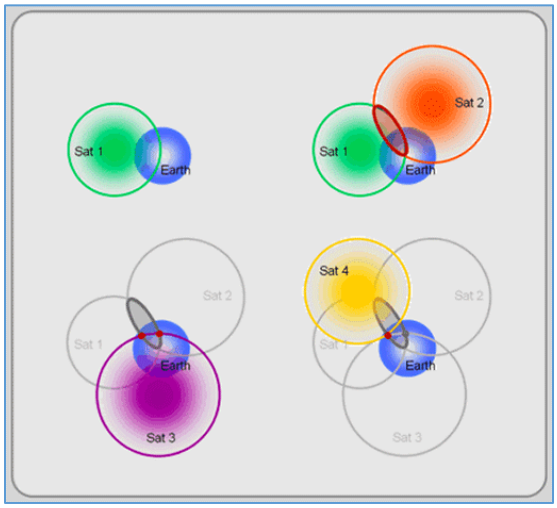

Figure 6: Trilateration method

There are many different applications for such a system, so they have been grouped into “Direct Applications”, “Indirect Applications”, and “Other Applications”, all of them detailed in the following subchapters.

[17] United Nations Office for Outer Space Affairs, “*Current and Planned Global and Regional Navigation Satellite Systems and Satellite-based Augmentations Systems*”, United Nations publication, AT, 2010.

2.3.1 Direct Applications

The first set of applications are those that directly relate to the original purpose of the system, more specifically all the navigation applications, which may be further divided into space and ground applications.

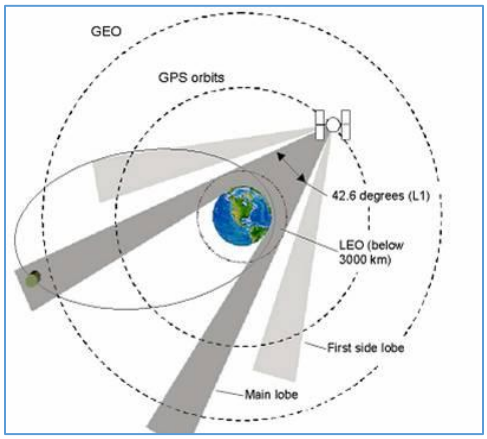

Figure 7: GPS-L1 for MEO and GEO

Regarding the space navigation application GNSS networks may be used for orbit determination thanks to the trilateration method explained above. GNSS satellites commonly have directive antennas in order to focus the transmitted power on the Earth's circle where the original users are. For this reason, using these navigation signals is mostly useful for LEO vehicles positioned right between the GNSS satellites and the Earth. Nonetheless, considering the small amount of RF power radiated at the sides of the Earth, some SV at higher orbits may receive GNSS messages of rather low power for short periods of time when flying through the spillover coverage windows as can be seen in *Figure 7: GPS-L1 for MEO and GEO*.

In regards to ground applications, it should be borne in mind that ground applications will also include using the navigation signals on flying receivers as long as these are inside the atmosphere. That being said, the most common ground application of GNSS is to use a receiver which provides location coordinates or more elaborated data, such as maps and navigation instructions, to users, regardless of these using vehicles (such as ground, water, or air transport) or not. In order to implement GNSS' most direct application, an independent receiver may be used, even though these can also be integrated into other devices more commonly used by people, as is the case of smartphones, tablets, and the currently growing smartwatches and smartbands.

2.3.2 Indirect Applications

GNSS' Indirect Applications have been defined as those in which position data is used by another system which goal is not directly navigation, although it might be included as part of the goal.

The first of these applications, which could be argued whether or not it should instead be considered a direct one, would be the usage of the position data by another system in order to track where all members of the system are. Some particular examples would be to track pets, people with special need, registered criminals such as sex offenders, or people who work in dangerous environments like those under heavy (or relatively heavy) radioactive environments (airline cabin crew and pilots, astronauts).

Another application which could as well be considered direct would be using the navigation data in order to command an autopilot system. This could be used in a variety of sectors, including transport vehicles (mostly unmanned aerial vehicles, planes and ships, but cars might be included in the near future), military applications such as guided ammunition, and the industrial sector (including smart agriculture, construction, and mining among many others, where machinery is automatically guided using GNSS data).

Using positioning data obtained from a GNSS system may also be used for Safe and Rescue (SAR) means, making it easier to locate and rescue those in distress such as hikers, rock climbers, and others. Also

related to sports and recreational activities, GNSS positioning data may be used by sport practitioners such as cyclists in order to log distances, trajectories, and timings. It may also be used in other recreational activities, such as in sky diving in order know the right drop zone, in wreck diving so specific shipwrecks may be found, or even in social networking for knowing when users of certain applications or products are nearby.

Regarding Cartographic and Geology/Geophysics applications, GNSS data may be used for different purposes. The first could be to automatically geo-tag images taken from planes which will be further used for map production and analysis, although this same application may be used by the public for geo-tagging pictures. Another application may be to use the relative displacement of GNSS receivers, which had been previously strategically positioned, in order to preform high precision measurements of Earth movements like those caused by volcanos or faults (as in planar fractures). Somewhat related to geophysics, but in this case closer to safety and construction, survey-grade receivers may be used to monitor position survey markers, buildings, and road construction (among others) thanks to the accurate positioning (down to 1[cm] or sometimes even less) achieved by using both L1 and L2, the latter for ionospheric compensation.

Finally, some other commercial uses of GNSS data may include the use of geo-fences and smart road pricing. Regarding geo-fences, those would allow devices to be switched on or off depending on their location, whereas smart road pricing would allow tracking vehicles and automatically charge them depending on distance and road type as well as gathering other data such as speed and exact trajectories which might be useful for insurance companies.

2.3.3 Other Applications

The third kind of applications are all those that don't really fit into the previous groups. These may be understood as "smart uses" of GNSS, meaning that they do not use the signals in the traditional way as navigation messages, but instead they take advantage of certain signal properties in order to obtain different information.

The first example of these applications could be a Global High-Precision Timing System. Thanks to having GNSS satellites orbiting and giving coverage to the whole planet, and broadcasting a specific time, this could be used by devices which include a receiver in order to accurately display or use the GNSS time.

Another way to take advantage of such systems could be to analyze the RF properties of the received signals. Knowing in advance how signals are generated and how atmosphere may change it (attenuation, phase, and polarization changes at different frequencies), knowledge about these and other parameters can be used to determine atmospheric properties, such as layer composition, winds, and many others, which at their turn may be useful for assisting in weather predictions.

To conclude, GNSS signals may also be used both on ground and space, in addition to positioning, for attitude of the receiver. This may be achieved by including multiple antennas and including a phase comparison between the signals received by each.

3. Phase 1: The SiGe Module

3.1 Introduction

The SiGe GN3S Sampler (see *Figure 8: SiGe GN3S Sampler*), also known as SiGe module, is a Universal Serial Bus (USB) GPS-L1 data sampler developed by the GNSS Lab at the SAESD in CU Boulder and SiGe Semidonductor[18]. The main purpose of this device is to be programmed with the Firmware (see chapter *3.3.1 Firmware*) and use the Data Logging Software (see chapter *3.3.3 Data Logging*), both developed by the GNSS Lab, in order to store and post-process the raw GPS-L1 data.

Figure 8: SiGe GN3S Sampler

This module's production had been discontinued after having had three updated designs due to core Application-Specific Integrated-Circuit (ASIC) SE4120L becoming an obsolete part. Nonetheless, thanks to the GNSS Lab having some spare parts as well as there being a couple of potential replacements, it had been decided that the module would be brought back not only because of its rather high demand by other research organizations, but also as a starting point and getting-used-to for this thesis project.

3.2 Hardware Design

SiGe's hardware can be divided into an electronics part and a casing part, both of which have been revised in this project, with more details in the following subchapters.

3.2.1 Electronics

The very first step carried out in this phase has been to determine which design files included the very last changes in order not to have to modify any and save time. From a general point of view in regards to the electronics of the module (see the complete schematics in *8.1 Annexure 1 – SiGe's Schematics* and the detailed design files in *8.2 Annexure 2 – SiGe's Layout*), they can all be found on the top layer (see *Figure 9: SiGe's layout*) of a 4-layer Printed Circuit Board (PCB). SiGe's electronic parts can be grouped as RF- or Computer-related, each group having a specific connector (USB or coaxial), having the most RF-sensitive parts protected by an RF shield. Moreover, it is worth mentioning that in order to further isolate the more robust digital (Computer) side from the more sensitive analog (RF) side, each has its own power supply which regulates the power provided by the USB to that required by the individual components.

[18] SiGe GN3S Sampler's main website: https://ccar.colorado.edu/gnss/

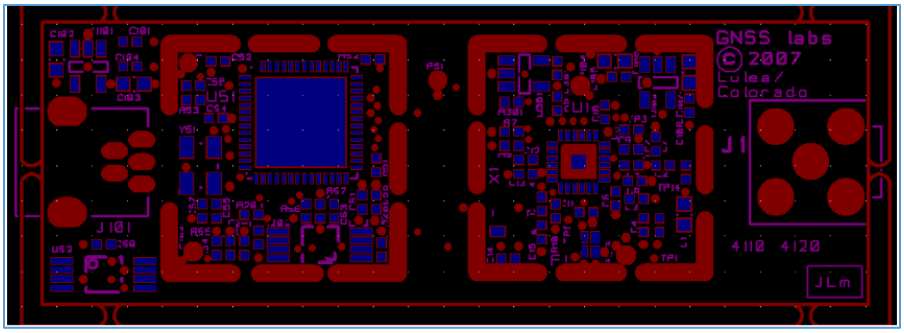

Figure 9: SiGe's layout

Regarding the RF portion, the components that belong to this group are located on the right half of the board, with the most relevant parts being the power supply, the RF shield, the coaxial connector, the Bias Tee, the oscillator, the Surface Acoustic Wave (SAW) filter, and the ASIC SE4120L. Below is a brief description of these RF components:

- Power supply: As mentioned above, it takes the power provided by the USB and regulates its voltage to that required by the other components.
- RF shield: Covers the most sensitive RF components in order to shield them from external interferences, be them environmental or from the digital part of the module.
- Coaxial connector: This is the common point between the module and its antenna.
- Bias Tee: Taking into consideration that the module is compatible with active antennas, it shall be able to provide the antenna a Direct Current (DC) voltage without interfering with the rest of the RF part (see *Figure 10: Bias Tee generic circuit*).

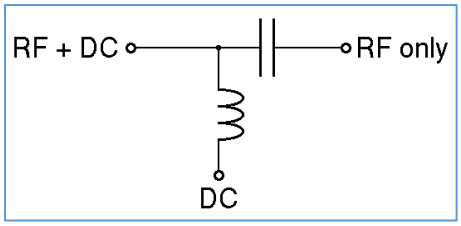

Figure 10: Bias Tee generic circuit

- Oscillator: This component (in particular a Temperature Compensated Crystal Oscillator or TCXO) provides the module with a reference frequency, which is used for down-converting the extremely high frequency of the GPS signal to a more manageable Intermediate Frequency (IF) by using multiples of it. As a side note, although originally the module and its related software were designed for a 16.368[MHz] oscillator, the previous manufactured version used a 16.3768[MHz] oscillator due to inaccuracies.
- SAW filter: Centered at 1.575[GHz], it is mostly used to limit the power out of the band of reception (in this case GPS-L1), so other components do not saturate and a clean signal may be received.
- SE4120L[19]: It is the brain of the RF section. It takes the signal provided by the antenna, amplifies it via an integrated Low Noise Amplifier (LNA), and processes it so a digitized version of it may be provided to the Computer part of the module.

[19] SE4120L datasheet on DigiKey: https://media.digikey.com/pdf/Data%20Sheets/Skyworks%20PDFs/SE4120L.pdf

On the other hand, the components of Computer portion of the module are located on the left side, with the main components in this case being the power supply, the RF shield, the USB connector, the core computer, the oscillator, the electrically erasable programmable read-only memory (EEPROM), and the Analog to Digital Converter (ADC). As the power supply and the RF shield serve the same purpose as in the RF section, these have been excluded from the brief component description below:

- USB connector: This connector is mostly used for communicating with the module's computer while providing it with enough power for operating. There are two different modes for communicating with the SiGe, namely programming (by which a firmware is set) and operating (by which data is extracted).
- Core computer: The core element of the Computer section is Cypress' CY7C68013A-56LFXC[20]. This element is the one in charge of operating the whole circuit and communicates the digitized signal to the host machine which is storing and potentially processing the GPS-L1 data.
- Oscillator: Again, this component provides a reference frequency, but in this case it is used by the core computer as a system clock.
- EEPROM: This memory is the one in charge of keeping the firmware required for operation and is accessed by the core computer.
- ADC: Placed between the SE4120L and the Cypress microcomputer, this component converts the analog output voltage which is proportional to the gain of the Automatic Gain Control (AGC) to a digital processable value.

3.2.1.1 Component Replacements

The electronics sector is, as many other, ever evolving, and new technologies and components are always being developed and introduced to the market, replacing older ones with better performance and features. For this reason, it is important to design with that in mind and choose components that not only have the right performance, but also a fairly common form factor so they can be easily replaced by other alternatives in case they become obsolete. This being said, the SiGe project is no exception, and since it has a rather old design, before bringing it back to production a component availability check has had to be performed.

Most components such as resistors, capacitors, power supply units, the ADC, diodes, connectors, and the RF shields have been easy to replace mainly because of their generic specifications and packages. Nonetheless, there are some other components which have required a bit more detailed analysis when assessing potential replacements, as can be seen in the subchapters below.

[20] CY7C68013A-56LFXC datasheet on Cypress: http://www.cypress.com/file/138911/download

3.2.1.1.1 The ASIC

As mentioned before, the SE4120L became obsolete and is consequently no longer available in the market. This posed a major issue in the return of the SiGe module, as its design is built around this piece of hardware. Therefore, two alternative parts from the same manufacturer have been analyzed:

- SE4110L[21]: This is an older version with similar specifications. The main differences between these two chips are only the available frequency scaling (slightly different values and the SE4120L having smaller increments as well), and three pins having different functionalities (see *Table 1: SE4110L and SE4120L pin comparison* below). Since these pins are all connected straight to the microcomputer, different behaviors would imply only changes in the Firmware so the electronic design could be maintained.

Table 1: SE4110L and SE4120L pin comparison

Pin #	SE4110	SE4120
Pin 10	RF data sign	RF data output
Pin 11	RF data magnitude	RF data output synchronization
Pin 14	Reference frequency 2	Filter bandwidth

- SE4150L[22]: This, on the other hand, is a newer version of the chip again with similar specifications. Although both chips belong to the same series, most of their pins have different behaviors. If this chip were chosen as an alternative, the electronic design would have to be changed in order to accommodate this new ASIC.

Because of the differences and similarities between these chips, the most suitable replacement that would imply the least and ideally only software modifications would be the SE4110L. Nonetheless, considering that some SE4120L (255 units) were still remaining in the GNSS Lab and found once the revision already had begun, SE4120L have been kept and used in this last production. However, it is advised to use SE4110L in case of future production phases.

3.2.1.1.2 The Oscillator

Regarding the original TCXO, it was the IT3205BE-16.3676[23] by Rakon. Some unattractive details of this part were that it was a rather expensive component (compared to other alternatives) despite its high-quality, that it is commercialized by Rakon itself instead of a general electronics supplier, and that it has a frequency of 16.3676[MHz]. The frequency value in particular is close to another standard value (16.368[MHz]), but the fact that it is lower mainly means that lower data rates are achieved, which at its turn translates to a worse Signal to Noise Ratio (SNR).

Therefore, for this project, a new choice of TCXO has been considered so the total module's cost could be lowered and, potentially, the signal quality improved by using the 16.368[MHz] option while at the same time maintaining the same form factor (see *Table 2: TCXO alternative comparison* below). It should be noted that only parts without a minimum order quantity have been considered, as the maximum amount

[21] SE4110L datasheet on DigiKey: https://media.digikey.com/pdf/Data%20Sheets/Skyworks%20PDFs/SE4110L.pdf
[22] SE4150L datasheed on SkyworkSinc: http://www.skyworksinc.com/uploads/documents/202445A.pdf
[23] Rakon TCXO: http://www.rakon.com/products/families/tcxo

of modules that would be built would not exceed 255 (maximum amount of available SE4120L as mentioned before).

Table 2: TCXO alternative comparison

Manufacturer Part Number	Manufacturer	Frequency [MHz]	Tolerance [ppb]	Price[24] [$]
7Q-16.368MBG-T	TXC Corporation	16.368	500	2.84
D32G-016.368M	Connor-Winfield	16.368	500	8.8
KT3225F16367ACW30TA0	AVX / Kyocera	16.3676	500	4.16
7Q-16.367667MBN-T	TXC Corporation	13.3676	2,000	2.25

As can be observed, the cheaper option would be 7Q-16.367667MBN-T by TXC Corporation, but it was also the one with the worse tolerance and 16.3676[MHz] (meaning a worse SNR as mentioned above), closely followed by the 7Q-16.368MBG-T, which had a better tolerance and the higher frequency. The remaining alternatives had prices twice or four times as high respectively but not more attractive specifications (even if the manufacturers might be well-known). Therefore, it has been concluded that the most valuable option (compromising specs, company respectability, and cost) would be the TXC's 7Q-16.368MBG-T.

3.2.1.1.3 The Inductors

The last of the sensitive replacements were the inductors (L1, L3, and L4 in the design files). The original inductors used in filters in the RF line had been discontinued, so they were either not commercialized or could only be purchased in large amounts (order of thousands), which were way too big for this project's scope. Moreover, finding replacements for these parts was not as simple as in other cases, mostly because these inductors had been carefully chosen with a specific induction and Q-factor.

This being said, although some potential alternatives were found in the market with same induction values and rather similar Q-factors, it has been decided to dismiss these and instead focus the research on finding a supplier which had the original parts in stock and commercialized them in smaller amounts. Afterwards, a company in Hong Kong has been found that offered the required parts without a minimum quantity and at competitive prices, so it has been decided to acquire those for production.

3.2.2 Casing

Previously, the SiGe modules were provided with a white plastic casing as can be seen in the figure below (see *Figure 11: SiGe's latest housing*), characterized by consisting in two pieces that would mate and be either glued or screwed together. This housing would provide not only some degree of mechanical protection to the electronics it contains, but also some aesthetics. However, due to the current lack of pieces and many new modules being produced during the execution of this project, newer housings have had to be manufactured as well.

[24] Values extracted from DigiKey (see *Bibliography* for a link) for comparison reasons.

Figure 11: SiGe's latest housing

Since the original production files were not available anymore, the first step towards production has been modeling two different versions of previous housings using Siemens NX in order to further assess them and choose the most feasible and attractive one.

The first version, and also the oldest reference housing, would be of a rectangular shape with rounded corners of about 65[mm] by 36[mm] by 12[mm], and consisted in two different pieces that would be screwed together (see *Figure 12: SiGe's new housing model v.1 lower (left) and upper (right)* parts).

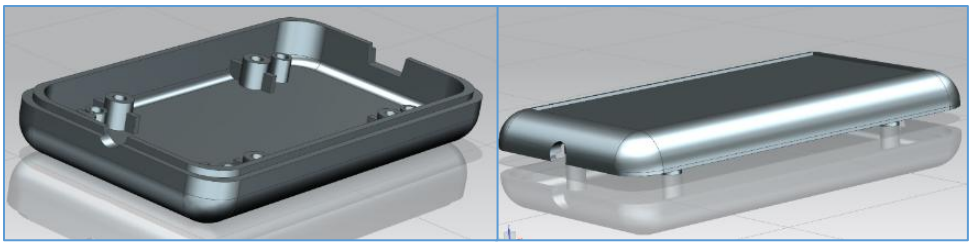

Figure 12: SiGe's new housing model v.1 lower (left) and upper (right) parts

The second alternative has been the latest housing available (see *Figure 11: SiGe's latest housing*). In this case, the two pieces would be identical and the dimensions would be 66.5[mm] by 32[mm] by 18[mm] (see *Figure 13: SiGe's new housing model v.2 inner view (left) and outer view (right)*). However, for this second version, the logo has been changed from the previous "SiGe" to "Buff", which is more symbolic for CU Boulder.

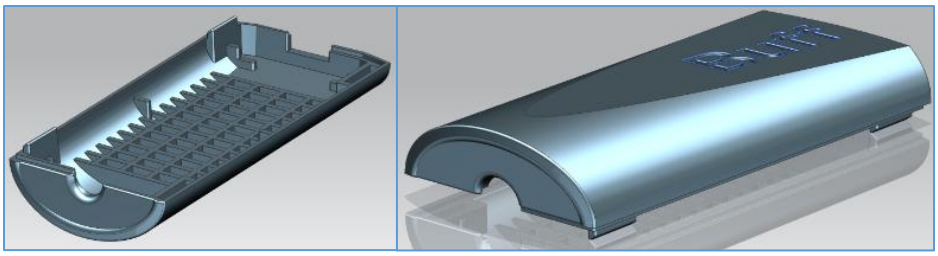

Figure 13: SiGe's new housing model v.2 inner view (left) and outer view (right)

After an initial assessment and market prospection, it has been concluded that the second version with two identical pieces would be much cheaper to build and it was also more aesthetic, and has consequently been chosen. As a final note, the logo might be changed once more in the future, even though this is out of the scope of this project.

3.3 Software Design

The main focus of this project has been on the electronics, even though some work has been done on the software side mostly in order to test the manufactured products and prepare them for future usage by the GNSS Lab. Details regarding the different software elements regarding the SiGe modules have been specified in the following subchapters.

3.3.1 Firmware

The firmware is the piece of software installed on a specific device with computing capabilities (ranging from simple TV remote controls to complex rocket guidance systems), and which provides the device with control and regulates its behavior.

Regarding the SiGe's firmware, it was developed for Linux back when the module was initially designed, by a dedicated team in the GNSS Lab. Furthermore, it would be stored in the SiGe's EEPROM and would allow the core computer to control the ASIC (which at its turn would provide the computer with sampled IF and AGC data) and the USB port (in order to communicate with an external machine), allowing the control of the operation mode (see more details of each mode in chapter *3.3.3.1 Intermediate Frequency (IF)*) and the extraction of the IF and AGC data. Moreover, the firmware also provides the module with a specific Vendor ID (VID) and Product ID (PID). These IDs are unique values given to USB devices which identify them from any others and which rights have to be purchased. In particular, the latest version of SiGe module used the VID/PID pair 0x1781/0x0B3F (in hexadecimal). However, in order to distinguish the new modules manufactured during the execution of this project from the old ones that have been successfully tested and the old ones which have not been tested, two new VID/PID sets have been implemented in the firmware. This way, the newly built modules have been assigned the pair 0x1781/0x0B37, whereas the old and successfully tested modules' IDs have been changed to 0x1781/0x0B36, and the old one which have not been tested have kept the original 0x1781/0x0B3F.

3.3.2 Drivers

Drivers are a piece of software installed on a computer which are required and used by certain operating systems (OS), such as Windows. They allow the computer to recognize a device connected to it, so interaction can be made possible. The SiGe modules require a USB connection for mainly two reasons: programming and operating. Therefore, a couple of drivers have been developed during this project and are detailed below.

As previously detailed, the SiGe's core computer is the Cypress CY7C68013A-56LFXC, which is programmed via USB using the same company's proprietary software known as CyConsole (see *Figure 14: Cypress' CyConsole*). This piece of software allows uploading IIC files (.icc), which are versions of the firmware, to the SiGe's EEPROM, and it was originally used along with Windows XP machines in order to make the modules operational. Nonetheless, due to Windows XP's support being ceased and becoming an obsolete OS, the application was ported to a newer Windows 10. Therefore, since the previously working driver was not compatible anymore with the new OS, a new version has been developed allowing the CyConsole to recognize the SiGe modules connected to the computer that are ready for being programmed with a new firmware.

In regards to the operation, SiGe modules are commonly used along with Linux machines, which do not require any additional drivers. Nonetheless, the GNSS Lab is working on porting the current Linux-only Data Logging application to Windows. Because of this, a driver will again be required in order to operate the modules and since the "programing" driver does not include compatibility features for libusb (one of the libraries used in the firmware's code) operation, a new "operation" driver has been developed. This has been based on another standard libusb driver for Windows 10, but the specific VID and PIDs used by the modules and their name have been detailed in order to easily distinguish the SiGe modules from other devices potentially using libusb.

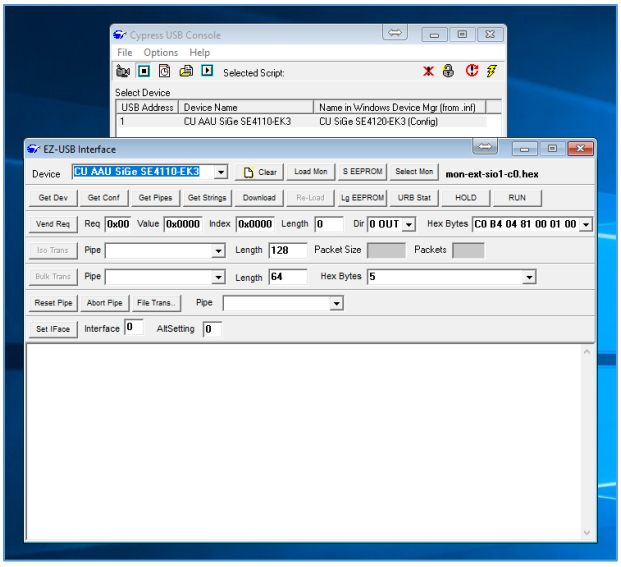

Figure 14: Cypress' CyConsole

3.3.3 Data Logging

The Data Logging is an ever evolving piece of software being developed by the GNSS Lab which is run typically on a Linux machine (even though efforts are being put on migrating it to a Windows environment). It accesses a SiGe module connected to the machine and operates it according to different parameters given at the beginning of the execution (such as operational mode, packing, IDs, etc.), recording the sampled IF and AGC data into binary files that can be further inspected and processed. More information about the kind of data that can be obtained from the SiGe modules has been detailed in the subchapters below.

3.3.3.1 Intermediate Frequency (IF)

As mentioned in the previous chapters, the SiGe GN3S Sampler is, as its name suggests, a data sampler which receives and processes a GPS-L1 signal by having the ASIC to downconvert the signal to an Intermediate Frequency (IF) and sample it, and the core computer to transfer it to a host machine via USB. The data can be obtained by operating the module in one out of a total of eight different modes, each having a specific IF, sampling frequency, and data type as represented by the table below (see *Table 3: SiGe's operational modes*).

Table 3: SiGe's operational modes

Mode	Band	Data Type	Oscillator Frequency [MHz]	Intermediate Frequency [kHz] (Factor)	Sampling Frequency [MHz] (Factor)
1	Narrow	2-bit real	16.3676	4,130.40 (96.00)	16.367600 (1/1)
			16.3680	4,092.00 (96.00)	16.368000 (1/1)
2	Narrow	4-bit I/Q	16.3676	38.84 (96.25)	8.183800 (1/2)
			16.3680	0.00 (96.25)	8.184000 (1/2)
3	Narrow	2-bit real	16.3676	4,130.40 (96.00)	5.455867 (1/3)
			16.3680	4,092.00 (96.00)	5.456000 (1/3)
4	Narrow	4-bit I/Q	16.3676	38.84 (96.25)	4.091900 (1/4)
			16.3680	0.00 (96.25)	4.092000 (1/4)
5	Wide	2-bit real	16.3676	4,130.40 (96.00)	16.367600 (1/1)
			16.3680	4,092.00 (96.00)	16.368000 (1/1)
6	Wide	4-bit I/Q	16.3676	38.84 (96.25)	8.183800 (1/2)
			16.3680	0.00 (96.25)	8.184000 (1/2)
7	Wide	2-bit real	16.3676	4,130.40 (96.00)	5.455867 (1/3)
			16.3680	4,092.00 (96.00)	5.456000 (1/3)
8	Wide	4-bit I/Q	16.3676	38.84 (96.25)	4.091900 (1/4)
			16.3680	0.00 (96.25)	4.092000 (1/4)

As can be observed, the two different clock frequencies (original value of 16.3676[MHz] and the new 16.368[MHz]) are represented since both modules are now simultaneously operational. Moreover and regarding the IF, this values have been obtained by mixing the GPS-L1 signal at 1,575.42[MHz] with a multiple of the internal oscillator frequency so as the final downconverted value lands either at baseband or very close (resulting in complex data), or at a low enough IF (resulting in real data). The resulting IF value can be determined by solving the following equation for F:

$$F_c = F_{osc} * F + IF$$

Where:

- F_c is GPS-L1 central frequency.
- F_{osc} is the internal oscillator frequency.
- F is the multiplying factor.
- IF is the intermediate frequency.

On a final note regarding these operational modes, a variety of sampling frequencies is assigned by dividing the oscillator frequency by factors 1, 2, 3, and 4.

The IF data stored in a file can then be post-processed by the code developed by the GNSS Lab team, which results in the following plots as well as additional text reports on the screen which give information not only regarding the signals that have been received and their properties but also about the satellites, their positions in the sky and the receiver's position (see *Figure 15: IF post-processing results*).

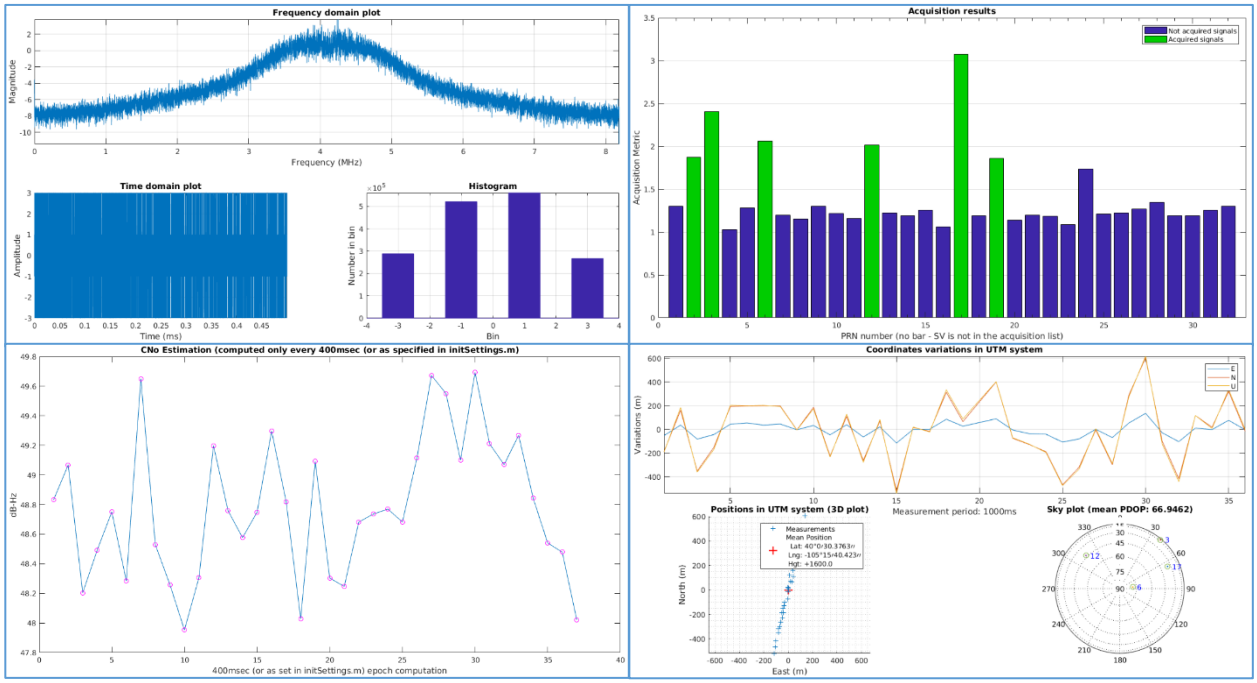

Figure 15: IF post-processing results

The first plot that can be obtained is the upper-left one, showing the frequency spectrum of the signal, its representation in time and the IQ distribution in the form of a histogram. Secondly, signal power representation for each of the satellites can be plotted, indicating in green those which are above a predefined threshold and for which the in-depth analysis will be performed (in order to obtain a position solution at least 4 satellites and 37[s] of data must be available). Thirdly and once the in-depth analysis has been initiated, a C/N_0 plot is shown for each of the satellite links that has been analyzed, which should be rather stable for reliable satellites at an altitude higher than 50°. Finally, once the in-depth post-processing is done, a plot with position solution variation, the receiver's temporary and final latitude and longitude values, and the position in the sky of the satellites that have been tracked is shown.

3.3.3.2 Automatic Gain Control

Thanks to the integrated Automatic Gain Control (AGC) system in the ASIC and the latter having an output pin which outputs a voltage proportional to the said gain, and the ADC, the core computer is capable of determining the amount of amplification needed by the received signal. Although the actual gain may vary from device to device and over time (atmospheric conditions, antenna orientation, and interferences, among others), it is possible to establish a baseline and afterwards determine whether the variations are due to interferences or not.

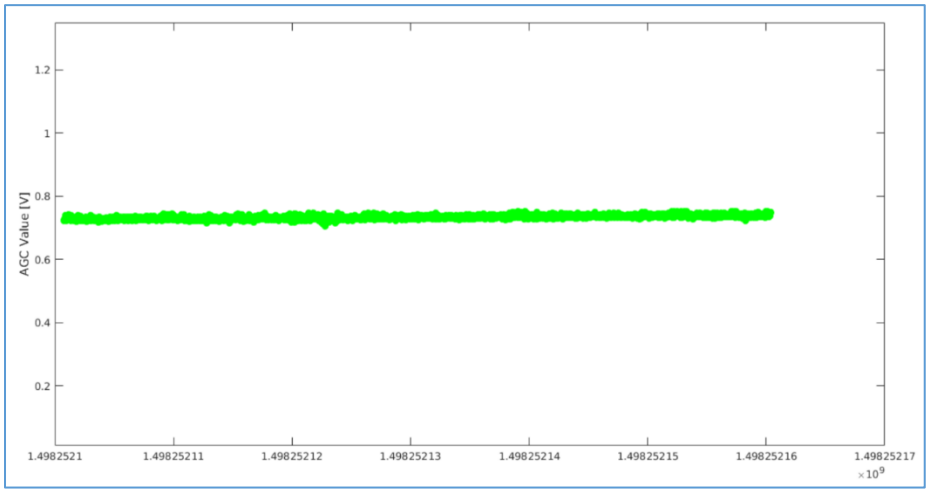

Figure 16: AGC post-processing results

As can be seen in the image above (see *Figure 16: AGC post-processing results*), the value obtained from post-processing the AGC data is rather stable (note plotted data has been gathered over a period of 1[min]). Moreover, it can be noticed how the average value is approximately 0.75[V]; this is extraordinarily high, but achieved thanks to an additional attenuator (used only while testing) in order to distinguish nominal behavior from extremely low values due to interferences.

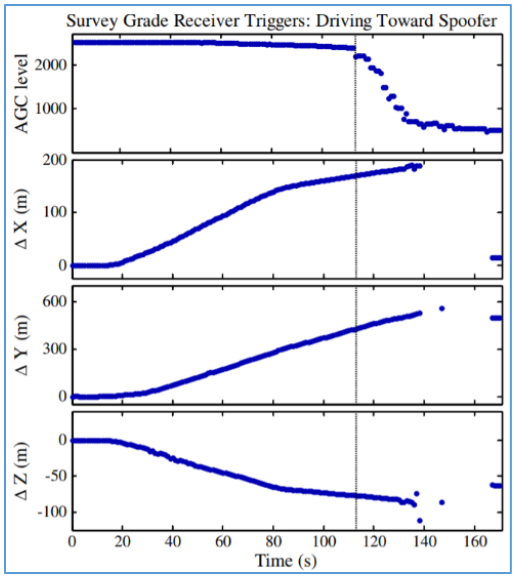

Figure 17: AGC under spoofer interferences

In short, the general idea for detecting interferences (particularly interesting for jammers) is by understanding how these interfering signals pass through the receiver's filter with a much higher power than the GNSS signal. This high-power non-useful signal that got into the system causes the AGC to drop as it is tricked to believe that not much amplification is needed. This drop in amplification causes the useful GNSS signal to have a too low power level to be detected and thus causes a loss in position tracking. An example of how this type of interferences may be visualized by analyzing the AGC data can be seen in the figure to the left (see *Figure 17: AGC under spoofer interferences*[25]). In it, it can be observed how as the interference gets closer, its higher power causes the AGC to drop down significantly and the receiver is not capable of delivering an accurate position solution.

[25] Akos, Dennis M., *"Who's Afraid of the Spoofer? GPS/GNSS Spoofing -Detection via Automatic Gain Control (AGC)"*, *J Inst Navig*, 59: 281-290, October 2012.

3.4 Manufacturing and Testing

Once the design revision has been completed, a production phase has been initiated, followed by testing of the manufactured products. More details on these two final phases have been included in the following subchapters.

3.4.1 Manufacturing

During this part of the project, both the PCBs and the housings have brought from the design phase to a final physical product. In order to do so, the following steps have had to be executed:

- File preparation.
- Manufacturer research.
- Production quotation.
- Order placement.

Nonetheless, additional steps might have been needed between the aforementioned parts during the process but since they are less relevant they have not been included this report. More specific details on the electronics and the casings can be found in the following sections.

3.4.1.1 Electronics

Regarding the electronics side of the SiGe modules, the first step has been to prepare the required files (see the end of *8.2 Annexure 2 – SiGe's Layout* in order to know how to obtain all the files). The ones typically needed for PCB production are:

- Gerber files.
- Drill files.
- Bill of Materials (BOM).
- XY Part Centroid.
- Special Assembly Notes.

About the Gerber files (.gbr), these are the layout files that contain all the information for each of the PCB layers. They mostly contain copper information, meaning where copper has to be placed in each layer, but there are some additional files in this set which also contain information about the silkscreen, which is a visual layer containing markings such as component designators, shapes, serial identifiers, and others, to help understanding and identifying the final product.

Secondly, the drill files are sometimes included in the same set as the Gerber, but they can also be found as a separate item. They contain information about all the holes that have to be drilled, such as position, diameter.

The next important file is the BOM (.xlsx), which has all the information about the parts needed for the assembly with the main goal of summarizing all the different parts that have to be sourced. There, product details such as manufacturer part number, manufacturer, supplier, total amount, special comments, footprint, and electrical and mechanical specifications can be found. Furthermore, each item has a set of component designators assigned, representing all the components that will be populated with a certain part.

Another important file for production is the XY Part Centroid (.txt) which despite the variable and strange name, it simply details for each component designator, its manufacturer part number and its exact

location on the board for automatic assembly positioning. The detailed location comprises information such as the central point X and Y coordinates, component rotation, and layer on which it has to be placed.

The last mandatory file that shall be provided is the Special Assembly Notes (.pdf). It details the guidelines for assembly, pointing to each file and its contents, specifying components that will be provided (don't have to be sourced by the manufacturer), those which do not have to be populated (also known as DNI for Do Not Install or DNP for Do Not Populate), specific details or care to be taken for some components (such as warnings about moisture sensitivity levels or electrostatic discharge resistance), standards to be followed, and packing and shipping details. In conclusion, this should contain (or point towards) all the information the manufacturer needs to know about the assembly.

Some additional files that might be interesting or sometimes needed are the Assembly and Drill Drawings (which are user-friendly versions of the Gerber and Drill files so it is easier to visualize and understand the final product), and the Polarity Markings file (in case some polarity or Pin1 markings are missing on the Gerber files).

The following step has been contacting the manufacturer. Previously, the SiGe modules were manufactured in California, but for this project it was decided that they should be built in Colorado mostly because of its proximity to CU Boulder and in order to try new manufacturers with potentially lower prices. Therefore, for this project Advanced Circuits (4PCB) has been contacted for the job so the first step here has been to provide all the files for a detailed quote. An initial negotiation phase has been conducted, as the original idea was to build as only four boards (two with a cheap TCXO and two with a more expensive one in order to test performances). However, obtaining these prototypes proved to be a complex and expensive process for the manufacturer, so it has been decided to go for an initial batch with the cheap TXC's 7Q-16.368MBG-T because a detailed comparison demonstrated its specifications were almost the same as those from the original oscillator. Afterwards, a brief discussion on which components should be sourced by CU Boulder and which ones by the manufacturer, exact specifications of the boards (such as standard or custom production, and array size), and timings has been conducted.

Once everything has been detailed, an 8-week custom production for 60 SiGe modules has been initiated. Even though there was a total amount of 255 SE4120L (limiting factor as these are no longer available on the market), the main reasons for initially building only 60 units are in order to test the results provided by the new manufacturer as well as payment constraints from CU Boulder.

Finally, prior to finishing this project, negotiations have been closed with Advanced Circuits for building 180 SiGe modules with an 8-week turn time and parts have been shipped in order to begin with production as soon as possible. The main difference between this production run and the previous one has been that due to the price and university constraints, it has been agreed that the RF shield frames (CAN1 and CAN2) would be provided by GNSS Lab in addition to the ones previously supplied. Furthermore, all parts have been shipped and production has been initiated.

3.4.1.2 Casing

In regards to the production of the housings for the SiGe modules, there have been mainly two options for production: 3D printing and injection molding.

3D printing is a growing manufacturing option with the main advantage being that it allows building plastic pieces with extremely complex shapes. Its main disadvantages at the current technology development stage are that it is a rather slow and costly process. Therefore, it is usually a solution picked for prototyping. On the other hand, injection molding is a much more mature technology, which consists in initially machining a (usually) metallic mold, which is afterwards used to cast the plastic pieces. The main advantages of the latter are a much faster production rate once the mold has been built and much lower cost per piece, whereas its main disadvantages are the lower piece complexity that can be manufactured and the high cost of small amounts of units (due to the mold costing typically about 1,000 the cost of one single piece).

Therefore, since the aforementioned are the main options, the first step has been preparing a STEP (.stp) file from the 3D model and a STereoLithography (.stl) file. The first one has been needed because it is the format typically requested by manufacturing companies, whereas the second one has been important in order to internally 3D print the housing at CU Boulder, required for conducting an initial testing phase to assess the design (see chapter *3.4.2.2 Casing*). Once the internal design assessment has been performed, multiple 3D-printing and injection molding companies have been contacted in order to obtain both quotes and feedback on how the 3D model has to be adapted for each manufacturing process.

As last production step, the company Yuyao Good Plastic Hardware has been chosen to build the housings using the technique of injection molding because of the price per unit, the total turn time, and the quality and risks of the production. In regards to the manufacturing phase, it has consisted of an initial mold production followed by building 10 samples, which have been shipped and evaluated in CU Boulder and, after approval, the remaining pieces have been manufactured and shipped all over 40 days.

3.4.2 Testing

Taking into account that during this phase of the project both the electronics and housings of the SiGe module have been manufactured, the results of both have been tested separately prior to assembling them into a complete module. Below in the following subsections the tests that have been carried out and their results have been detailed.

3.4.2.1 Electronics

Regarding the electronics, the very first test that has been performed has been to check whether or not the modules were recognized by a Windows computer with the proper drivers installed, followed by attempting to program them with the new version of the firmware using the CyConsole.

After succeeding with all of them, the RF performance of the modules has been tested. Two iterations of the same test have been performed in two separate days, each in one single run of approximately 2 hours. The first test has been executed at Discovery Learning Center's balcony at CU Boulder starting at 1500(MT) on June 23, 2017, and the second has been done at the same location but starting at 1627(MT) on June 28, 2017. Therefore, thanks to the single runs, each module would experience more or less the same atmospheric conditions and have the same satellites in sight, whereas running multiple tests in separate

days would allow dismissing some errors due to environmental factors (such as low C/N_0 or low signal power from certain satellites due to dense clouds or rain). In particular, each test has consisted mostly in acquiring 1 minute of both IF and AGC data with the operational mode number 1 (the tougher due to being narrow band and having the highest sampling frequency as detailed in *Table 3: SiGe's operational modes*) initially with a calibration module (an old one), and afterwards with all the new modules, which results have been contrasted with the calibration data.

In order to perform these tests, the setup used has been a U-blox GPS active antenna model ANN-MS-0-005 attached to the SiGe module through a 10dB attenuator in order to increase the baseline AGC voltage so low values due to interferences can be distinguished. Then, the module has been connected to a host computer using a USB cable, which has been running the data logging software.

Table 4: GPS satellites' ID and name

Satellite ID	Satellite name	Satellite ID	Satellite name
1	USA-232	17	USA-183 / IIR-14
2	USA-180	18	USA-156
3	USA-258	19	USA-177
4	USA-96 (reserve)	20	USA-150
5	USA-206 / IIR-21	21	USA-168
6	USA-251	22	USA-175
7	USA-201 / IIR-19	23	USA-178
8	USA-262	24	USA-239
9	USA-256	25	USA-213
10	USA-265	26	USA-260
11	USA-145	27	USA-242
12	USA-192 / IIR-16	28	USA-151
13	USA-132	29	USA-199 / IIR-18
14	USA-154	30	USA-248
15	USA-196 / IIR-17	31	USA-190 / IIR-15
16	USA-166	32	USA-266

Once all the data has been gathered, the first thing that has been checked with the Matlab software has been the amount of satellites in sight (at least 4 for properly acquiring a position solution) and their names/ID. This has been achieved by first checking the amount of signals (and their origin) which power was above a certain threshold (this had to sometimes be adjusted depending on environmental conditions in order to accept lower power values) and by translating the IDs to the satellite names using the table above (see *Table 4: GPS satellites' ID and name*), followed by comparing the list to that shown by an online application which contains a sky plot of satellites from multiple constellations which are passing over a specific position on Earth at a specific point in time (see *Figure 18: Detected satellites (left) and actual satellites in the sky (right)*[26]). The results for this part of the test have shown that the calibration module could detect 6 satellites, whereas the newer ones detected in average 4.8000 satellites with a standard deviation of 0.7916, having a minimum amount of 4 and a maximum of 7 detected satellites.

[26] Plot extracted from In-The-Sky.org, https://in-the-sky.org/satmap_worldmap.php

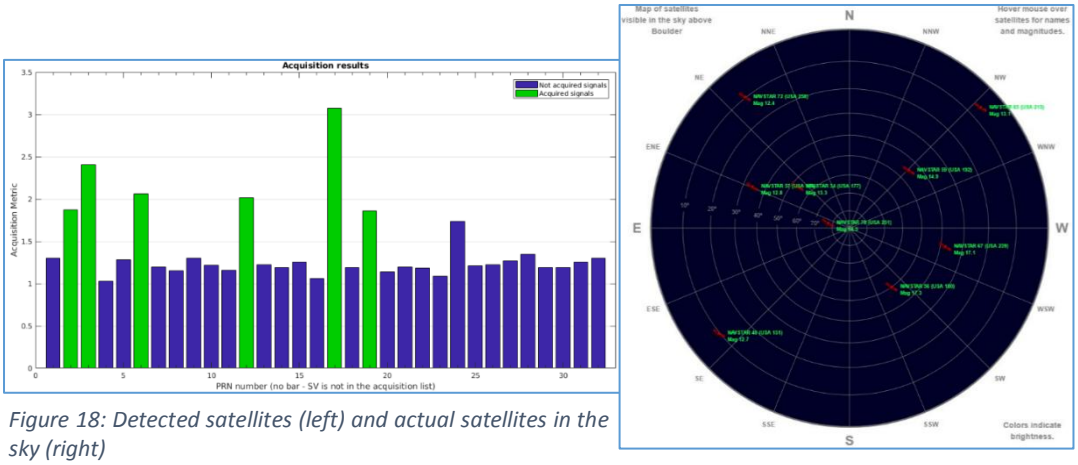

Figure 18: Detected satellites (left) and actual satellites in the sky (right)

The next step has been to start tracking at least 4 of the channels with the same Matlab software, with the goal of obtaining a position solution. The first data the software provided has been the evolution over time of the C/N_0 for each of the tracked channels, followed by the mean and standard deviation values. Immediately after that, the software also provided a position solution in the form of latitude and longitude, as well as the variation of such a solution in meters over the time, and a sky plot with the tracked satellites. From all this data, it has been concluded that the calibration module had an average C/N_0 of 46.6575[dB-Hz] with a standard deviation of 0.4871[dB-Hz] for tracked satellites with an altitude of at least 50°, whereas the newer modules displayed a total average of 46.5932[dB-Hz] with a Case 1 of standard deviation of 0.4070[dB-Hz] (calculated by averaging each of the module's total standard deviation of C/N_0), and a Case 2 of standard deviation of 0.5678[dB-Hz] (this time calculated from the averaged C/N_0 of all modules). Regarding the position solution, all the acquired results have been with an accuracy of less than 15[m] excluding a few which failed in one test due to external conditions, but were successful in the other test. The resulting sky plot (see *Figure 19: Sky plot of the tracked satellites*) has also been compared to the online application (again as in *Figure 18: Detected satellites (left) and actual satellites in the sky (right)*) where the same results have been visualized, only flipped around the vertical axis.

As a final step, the Matlab software has also been used in order to analyze the AGC file generated by the data logging software. From it, it has been observed that most of the modules provided stable values as expected, but some of them were rather noisy or showed particularly deep dips. Nonetheless, by analyzing the results of the second run of tests, most of these were not present anymore, resulting in a total average of 0.7590[V] with Case 1 of standard deviation of 0.0081[V], and a Case 2 of standard deviation of 0.0525[V], compared to the calibration average voltage of 0.7338[V] with a standard deviation of 0.0055[V] (equivalent to Case 1).

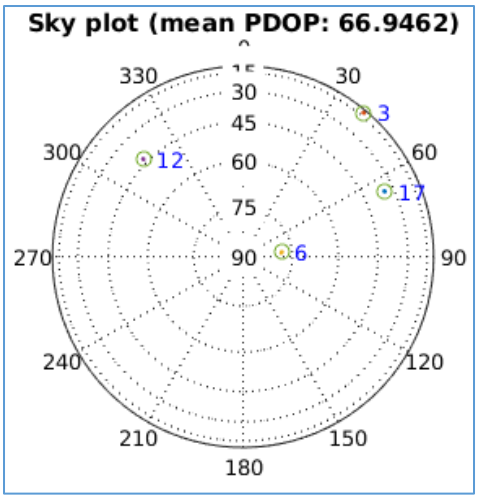

Figure 19: Sky plot of the tracked satellites

Table 5: SiGe's electronic tests results (1)

Module version	Average amount of satellites	Standard deviation of amount of satellites
Old	6	N/A
New	4.8	0. 7916

Table 6: SiGe's electronic tests results (2)

Module version	Mean C/N_0 [dB-Hz] (across the board)	Standard deviations of C/N_0 [dB-Hz] (Case 1)	Standard deviation of C/N_0 [dB-Hz] (Case 2)	Mean AGC [V] (across the board)	Standard deviation of AGC [V] (Case 1)	Standard deviation of AGC [V] (Case 2)
Old	46.6575	0.4871	N/A	0.7338	0.0055	N/A
New	46.5932	0.4070	0.5678	0.7590	0.0081	0.0525

In conclusion, as can be seen in the table below (see *Table 5: SiGe's electronic tests results (1)* and *Table 6: SiGe's electronic tests results (2)*) where all the results have been compiled, all new modules have provided performance values similar to those of the older versions. Furthermore, although it is true that some tests did result in some errors, such as instances where position solutions could not be obtained, these were wrong, or the AGC values were noisy, it has been determined that these were due to interferences and/or environmental conditions (such as bad weather) because they were not consistent throughout the multiple tests, but only occurred in one of them.

As a final note, it should be added that all the older SiGe modules found in the offices and laboratory have been collected and tested in order to separate the ones that did not work at all from those that could be recognized by a computer with the required drivers, the ones that could be programmed, and the ones where only IF data could be logged (no AGC), and those that were fully functional. The troublesome modules (not fully operational) have kept the old 0x1781/0x0B3F pair, whereas the older functional ones have been modified with the new 0x1781/0x0B36 pair, saving 0x1781/0x0B37 for the new modules.

3.4.2.2 Casing

In regards to the multiple tests performed on the casings for the SiGe module, it is important to bear in mind that not all of them have been post-production like in the case of the electronics. Instead, two out of the three tests have been carried out before entering a production stage.

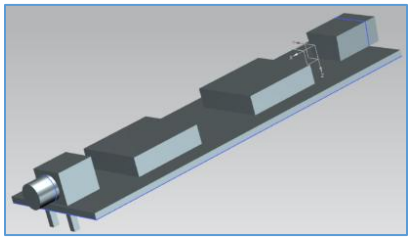

Figure 20: SiGe's PCB model

The first test has been a digital one, meaning that it has been performed using only the 3D models and a computer. In particular, once the 3D model of the housing has been completed (see *Figure 13: SiGe's new housing model v.2 inner view (left) and* outer view (right) in subchapter *3.2.2 Casing*), another model representing the electronics (see *Figure 20: SiGe's PCB model*) has also been prepared.

Afterwards, both the casing and the PCB models have been imported as an assembly in the same Siemens NX, where it has been possible to digitally test the fittings of the three (2 and 1 respectively). As can be seen in the figure below (see *Figure 21: SiGe's casing digital test*), first the three pieces have been presented. Afterwards, the PCB has been placed inside the lower half of the housing and it has been verified that there was enough room for protruding pins of the antenna connector and that the holes were big enough for both connectors. Next, the upper half of the casing has been brought down in order to check if the 4 interconnecting lids (2 per half) would match and fit inside their respective receptacles. Finally, the upper half has been completely brought down in order to check whether or not there was enough room on the upper half for the electronics and the connectors as well as to verify that both halves would perfectly fit.

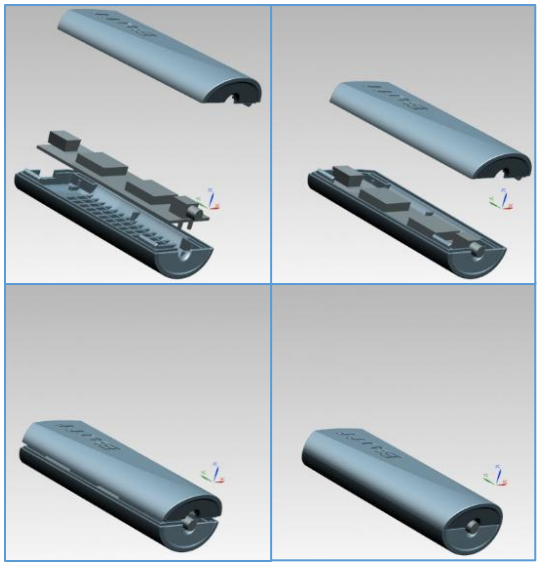

Figure 21: SiGe's casing digital test

Having completed the initial digital test, a 3D-printed version of the housing has been built internally at CU Boulder in order to further test the casing prior to entering a mass production stage. For this, two pieces (2 halves) have been printed using the Tier 1 3D Printer (Objet30) available at the Integrated Teaching & Learning Laboratory (ITLL) at CU Boulder, which is capable of printing white VeroWhitePlus pieces of up to 279.4[mm] by 190.5[mm] by 147.32[mm] using support material for more complex shapes. Once the support material has been removed from the pieces, these have been tested for physical fitting and toughness. Although the two halves fit perfectly, it has been noted that the prototype of the housing is rather brittle and may crack upon falling. However, these defects have been attributed to the manufacturing process and material. After this testing phase, a new module has been built using the new electronics, the newly printed housing, and two pieces of foam to prevent shacking (see *Figure 22: SiGe's casing prototype (top left), assembled module (top right), and comparison (bottom)*), reaching this way a production stage.

Figure 22: SiGe's casing prototype (top left), assembled module (top right), and comparison (bottom)

Although at the beginning of the project manufacturing and fully testing the SiGe's housings seemed to be feasible, due to this not being as relevant as other electronic parts (of this and other projects), production has been delayed to the point where the housings have been ordered and at the end of the project, with no time left for testing. For this reason, only the samples (see *Figure 23: SiGe's casing final parts (samples)*) have been assessed prior to initiating mass-production, demonstrating an increased toughness and an overall more polished finish with a smoother texture and bright white color. However, testing of the remaining parts has not been included in this project. Instead, a member of the GNSS Lab has been instructed on how to check said remaining casings parts provided by Yuyao Good Plastic Hardware, and how to assemble the complete modules (as done with the prototype printed at CU Boulder during this project).

Figure 23: SiGe's casing final parts (samples)

4. Phase 2: The New Generation Receiver

4.1 Introduction

4.1.1 The GN3S_PMOD Board

Figure 24: GN3S_PMOD Board

As seen before with the SiGe module (see chapter *3 Phase 1: The SiGe Module*), GNSS receivers are usually composed of two main parts: RF side and Computing side. In more complex cases, though, the module itself may be divided into two or more separate boards, having this way an RF front-end board and a Field-Programmable Gate Array (FPGA) or peripheral-controlling board.

Regarding the RF front-end, these boards usually consist of four antenna connectors and all the required electronics to digitize the I/Q components and transfer these to the other board.

An example of GNSS front-end is the GN3S PMOD Board (see *Figure 24: GN3S_PMOD Board*) developed by the GNSS Lab at CU Boulder and Space Sciences. It is, in particular, a 4-channel GNSS receiver based on the NTLab's NT1065 "Nomada" as its RF front-end chip capable of digitizing the RF at its 4 inputs. It also has two options for power input: 12[V] DC power jack and through the PMOD connectors; which may be selected via a jumper. Regarding the oscillator, it has three options (internal 10[MHz], internal 24.84[MHz], or external clock reference through an SMB connector) again selectable with a jumper. In regards to the outputs of this board, it provides two Peripheral Module (PMOD) connectors and a clock output (the latter not populated in the picture).

The main benefit of such a board is that it is an easily stackable solution using a standard PMOD configuration for receiving and digitizing up to 4 channels of any satellite-based navigation system. However, it also poses some quite important disadvantages when thinking of a more portable solution, such as the need for external RF signal pre-processing. In this regard, it particularly lacks a Bias Tee for removing the DC component from an active antenna, a power splitter which would allow using one single antenna, and dedicated SAW filters that would narrow the RF power to that of the useful band, even if the latter may be an advantage by allowing a higher configurability.

Finally, as this board is only the RF part of the receiver, it requires another board with the same PMOD connectivity which is capable of processing the signal. In this case, the GNSS Lab chose to use a Zed Board (see the following subchapter *4.1.2 The ZedBoard and the MicroZed Board*), which contains the FPGA, peripherals, and controllers for the latter.

4.1.2 The ZedBoard and the MicroZed Board

If the previous subchapter described the RF front-end boards and in particular the GN3S_PMOD Board, below in this one the FPGA or Computing boards have been included.

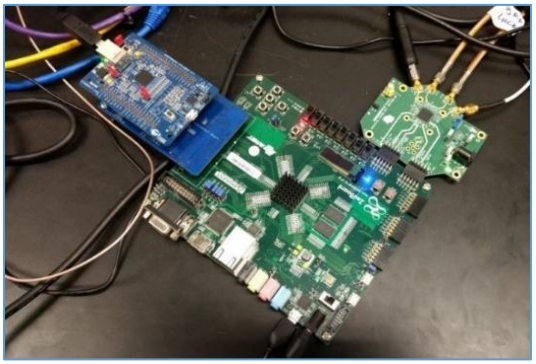

Figure 25: ZedBoard (center), GN3S_PMOD (right), and Cypress' EZ-USB FX3 (left) stack

As mentioned before, the GN3S_PMOD Board was designed in order to be used with the ZedBoard[27] (see *Figure 25: ZedBoard (center), GN3S_PMOD (right), and Cypress' EZ-USB FX3 (left)*), a board which contains a central FPGA for processing, and multiple peripherals and their controllers so it is possible to communicate with external devices while operating in one of multiple selectable modes.

The core of the board may be divided into 4 different sections: FPGA, memory, power supply, and peripherals. The FPGA of choice, around which the whole board has been designed, is Xilinx's Zynq 7000 series, which provides the computing capabilities. Regarding the memory, the board contains two instances of DDR3 Random Access Memory (RAM), a 4-bit SPI Flash, and a Secure Digital (SD) Card Interface. Furthermore, in terms of peripherals, the board offers five PMOD (two of which are used by the GN3S PMOD Board) and other expansion headers (like the FPGA Mezzanine Card or FMC, and the Agile Mixed Signaling or AMS), USB, Ethernet, Display and Audio, push buttons, Dual In-line Package (DIP) switches, Light-Emitting Diodes (LED).

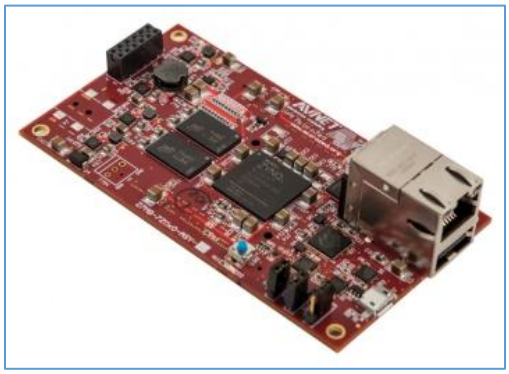

Figure 26: MicroZed Board

However, since most of the connectors are useless for the GNSS Lab's main usage of GNSS data collection and processing, it has been planned to migrate to a newer and smaller version of 101.6[mm] by 57.15[mm], the MicroZed[28] Board (see *Figure 26: MicroZed Board*). It offers similar features as the ZedBoard, with the main advantage being a smaller form factor and providing only a USB and a USB-to-Universal Asynchronous Receiver/Transmitter (UART) bridge, an Ethernet connector, an SD Card Interface, two PMOD connectors, and two MicroHeader connectors, while also doubling the amount of RAM and Flash memory available.

Therefore, thanks to this board providing better specifications than the ZedBoard while being smaller, it makes it a more attractive solution as a computing board for a GNSS receiver. For this reason, the new generation receiver has been designed being compatible with the MicroZed Board.

[27] See datasheet on http://zedboard.org/sites/default/files/documentations/ZedBoard_HW_UG_v2_2.pdf
[28] See datasheet on http://microzed.org/sites/default/files/documentations/MicroZed_HW_UG_v1_4.pdf

4.1.3 The Receiver

As a first iteration of the new generation 4-channel GNSS receiver (also known internally by GNSS Lab members as NT1065_MicroZed Board), the main goal of this project has been to obtain the design of an initial two-board solution capable of receiving 4 GNSS channels at once (any combination of constellations and bands) while being able to mate with the MicroZed Board in order to overcome most of the main disadvantages of the previous GN3S_PMOD Board and ZedBoard stack. Although components have been chosen to be easily replaced by others thanks to having the same form factor, the first design has been that which allows the reception of GPS-L1, GLONASS-L1, GPS-L2, and GLONASS-L2.

In order to achieve that, an initial review of the GN3S_PMOD Board design and the reference material of the MicroZed Board has been performed. This way the original design has been taken as a basis, in this case including additional components such as a Bias Tee, a power splitter, and the four SAW filters in order to minimize the amount of external components, as well as replacing the PMOD connectors by a pair of MicroHeaders able to mate with those of the MicroZed Board. Moreover, some other minor changes to the internal clock and the power supply unit have been applied in order to optimize the circuitry and allow a better interconnection and power options with the new MicroZed. However, for more details regarding the design process refer to the following chapter *4.2 First Iteration - Hardware Design*.

On a final note, it should also be borne in mind that originally, the project was also intended to include a second iteration where a single-board solution would be designed so as the new design and the most essential components of the MicroZed Board would be merged into one board. Nonetheless, after a first assessment and once the MicroZed schematics had been imported into Altium Designer, it was concluded that due to time and budget constraints this part would be delayed and executed in the future. Also about the scope of the project, the housing has been excluded again due to time and budget constraints.

4.2 First Iteration - Hardware Design

The hardware design phase for the new NT1065_MicroZed Board has been different from that of the SiGe module in a few aspects. First off, taking into account that it is a first version of the design, the focus has initially been on reviewing the reference design material provided mostly by Avnet [29] (MicroZed distributor) as well as NTLab[30] (new receiver's ASIC manufacturer) in order to properly understand the behavior of both the MicroZed Board and the main ASIC, followed by the other components', in order to provide each of the basic functioning blocks with the circuitry they require for the specific operation needed by this project. Secondly, a set of schematic files has been prepared according to the information gathered in the previous step, and additional research on specific components (such as manufacturer part numbers, footprints, availability, potential replacements, and others) has been carried out. Afterwards, the complete schematic files have been forwarded to the company Metro Logic, which has been subcontracted for the layout design.

[29] Datasheet and Carrier Cards reference design among other files extracted from MicroZed's dedicated website: http://zedboard.org/product/microzed

[30] Datasheet and additional material such as evaluation kids extracted from NT1065's dedicated website: http://ntlab.com/section/sec:v:36729.htm

4.2.1 Schematics

As mentioned above, the schematics for the new board have been partially based on a series of reference designs provided by board and component manufacturers. During this design phase, real products (manufacturer part numbers) have been checked and assigned for each of the components in order to also complete the BOM and the footprints required for the layout design, while at the same time paying attention to their availability, minimum order amount, and price in order to optimize costs. On a side note, taking into account that the schematic files are rather extensive, they will be described below in this chapter by parts and in alphabetical order, but the whole files can be seen in *8.3 Annexure 3 – NT1065_MicroZed's Schematics*.

The first file is the MicroHeader (.SchDoc), which contains the schematics related to the MicroHeader connectors and some additional Light-Emitting Diode (LED) indicators. The first relevant parts of this schematic file (see *Figure 27: Battery connector and Power Enable*) are the battery connector (X1) with its associated capacitor in case a battery shall be used as well as the power enable (PWR_EN) signal, which is a design requirement for carrier cards which are supposed to mate with the MicroZed Board (more details on how this signal is generated below when discussing about the file Power (.SchDoc)).

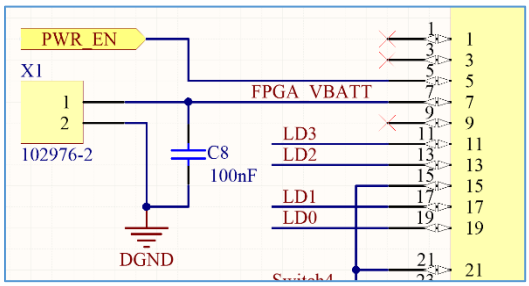

Figure 27: Battery connector and Power Enable

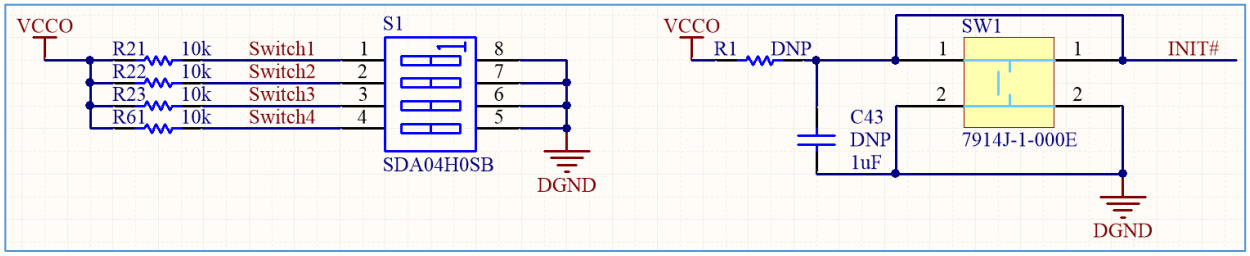

Figure 28: In-Line switch and initialization button

Regarding the different switches and buttons present in the schematic (see *Figure 28: In-Line switch and initialization button*), the switch (S1) is mostly used for operational purposes (having pull-up resistors and being directly connected to the MicroHeader (JX1) pins 31, 29, 25, and 23), whereas the button (SW1) is used to send the MicroZed Board an initialization signal.

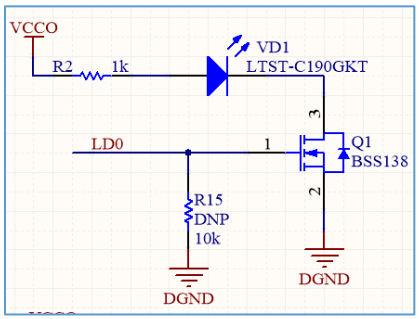

Figure 29: LED indicator and circuitry

The final relevant part of the first file would be the four LED indicators and their respective circuitry (see *Figure 29: LED indicator and circuitry*). These circuits are based on an N-Channel Power Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) which is used to allow conduction through the LED depending on the signal at their gate. Said signal is directly supplied by the MicroZed Board through the MicroHeader connector (JX1) via pins 19, 17, 13, and 11. The main goal of these indicators will be to provide visual information about the current operational status of the receiver.

The second file has been the NT1065_MicroZed (.SchDoc), where some the circuitry related to the ASIC (NT1065) can be found. The first and most important bit of this file are the RF lines which provide the GNSS signals (see *Figure 30: Incoming RF line to the ASIC*). To start with, this part of the RF lines has to

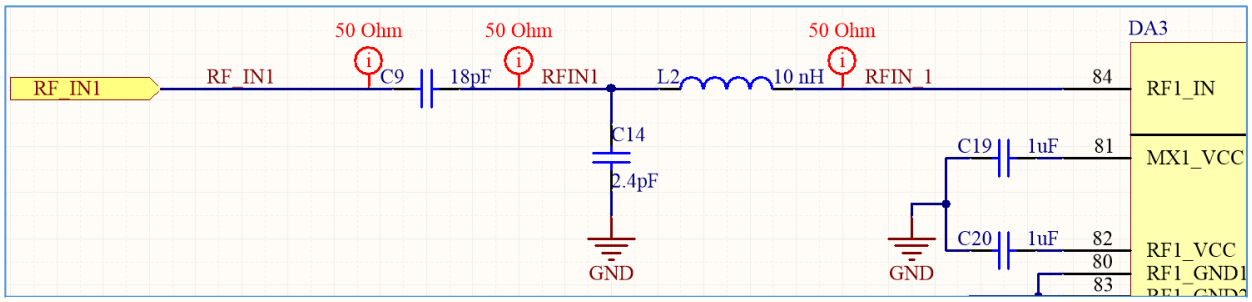

Figure 30: Incoming RF line to the ASIC

have an impedance of 50[Ω] as specified by NTLab, fact which has had to be taken into account when designing the layout and choosing the board's support material. Furthermore, the present passive components have been chosen in order to adapt the impedance at a specific frequency band. On this topic and as mentioned in the introduction of this chapter (see chapter *4.1.3 The Receiver*), the lines reaching the ASIC's input pins 84, 5, 18, and 27 have been adapted at the frequency bands of GPS-L1, GLONASS-L1, GPS-L2, and GLONASS-L2 respectively.

Another important section of the NT1065_MicroZed (.SchDoc) would be the core oscillator (see *Figure 31: ASIC's oscillator*). Although originally there were three options available, only two made it to the current version of the design, namely the 10[MHz] internal clock (DA1) and its associated components, and the external clock connection (X8). However, the internal one is intended to be used in nominal operation. It is also important to mention that the clock line (reaching the ASIC's pin 34) is also supposed to have an impedance of 50[Ω] and consequently the same applies as for the RF lines in terms of board material and layer stack design.

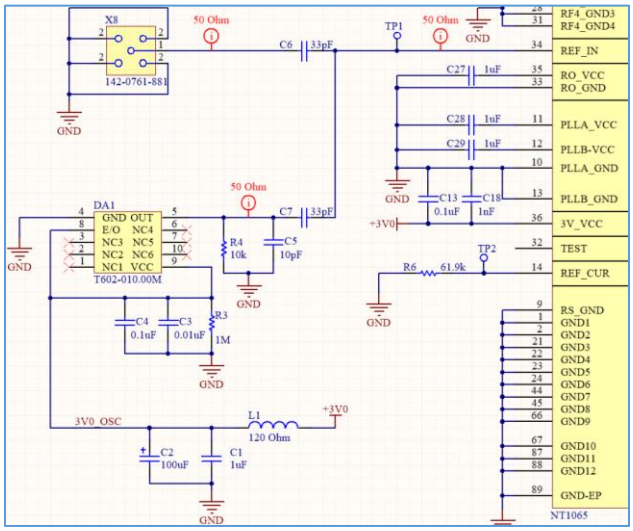

Figure 31: ASIC's oscillator

On a final note regarding the second schematic file, there are many more components used in both Input/Output (IO) pins as well as status LED and an output clock option. Said clock provides both a Low Voltage Differential Signal (LVDS) and single end lines, even though the latter is not yet available as the LVDS receiver (T5) has not been populated in this iteration.

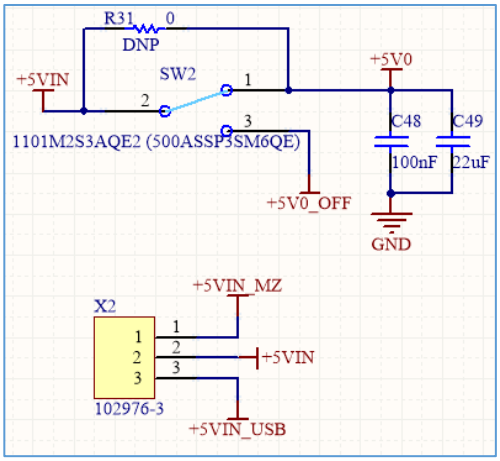

Figure 32: Power selection components

The third file has been the Power (.SchDoc) and it contains all the power supply components along with those needed for generating and utilizing the power enable (PWR_EN) and IO power enable (VCCIO_EN) respectively as required by the MicroZed Board. Taking into consideration that most of the circuitry in this file has been determined by the reference design files provided by the supplier, only the new parts designed in this project have been included in the discussion below. The first components that have been included in the design have been the power selection components (see *Figure 32: Power selection components*), namely the switch (SW2) and its related parts, and the jumper (X2). Thanks to SW2, and ON/OFF feature has been added to the board. On the other hand, the jumper X2 allows choosing the source of power between the USB and the MicroHeader (assuming the DC power jack and its related components are populated on the MicroZed Board, which aren't by default). This way, it will be possible to power up the new NT1065_MicroZed board without it being connected to the MicroZed for both testing purposes and usage along with default MicroZed Boards. However, the very same design may be used with altered MicroZed Boards with said power jack in order to minimize the amount of wired connections and simplify the test/operation setup.

Following with the idea of power source and keeping in mind that the reference designs already include a USB connector with a Zenner diode which prevents power from being fed back into the USB, an additional protection unit has been designed for the power provided by the MicroZed Board through the MicroHeader connectors (see *Figure 33: Power supply protection circuit*). This unit is basically a DC-DC linear voltage regulator that converts the MicroZed-supplied voltage to a stable 5[V] and a high enough current rating (750[mA]) to power the board. Nonetheless, it has been decided that the voltage converter will not be initially populated in order to optimize production costs of the first boards. It is also worth mentioning that, although there are both linear and switching voltage regulators, a linear solution has been picked mostly in order to prevent interferences associated with switching voltage regulators, and because of only needing a small voltage downconversion, rendering the benefits of a switching unit almost irrelevant.

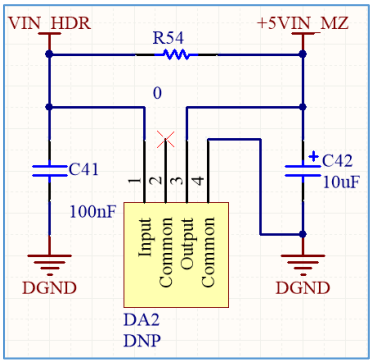

Figure 33: Power supply protection circuit

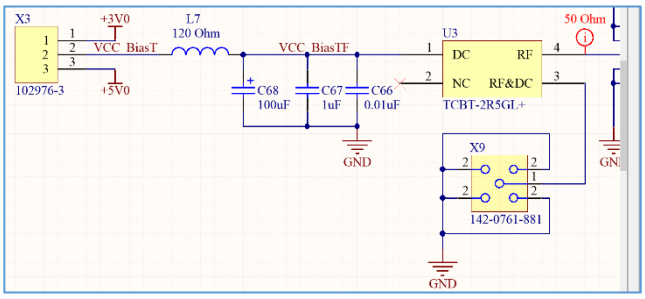

Figure 34: Bias Tee and antenna connection

Finally, the last schematic file that has been generated has been the RFInput (.SchDoc), which contains all the RF components from the antenna connector (X9) to the SAW filters (U5, U7, U4, and U6) prior to the 50[Ω] RF lines mentioned in the file NT1065_MicroZed (.SchDoc). The first block found after the antenna connector is the Bias Tee (U3) and its DC selection unit (see *Figure 34: Bias Tee and antenna connection*). As can be

seen, the voltage provided to the Bias Tee can be selected between 3.3[V] and 5[V] using a jumper (X3) depending on the requirements of the antenna used in the system. In addition, a low-pass filter (L7, C68, C67, and C66) has been included before the Bias Tee in order to ensure a very low frequency (ideally DC).

The RF output of the Bias Tee (which already should have an impedance of 50[Ω] as before for onboard RF lines) is connected to a power divider (U2), which at its turn provides the four instances of RF signal to the four SAW filters (see *Figure 35: Power divider and SAW filters*). Thanks to this power-dividing unit, it is possible to use one single antenna connector, thus minimizing the total dimensions and amount of components required while still being able to work with four lines. When the real component has had to be picked, two options have been taken into account: 1x 4-channel splitter (single solution) or 3x 2-channel splitters (cascade solution). After an assessment of the different alternatives in the market (see *Table 7: Power divider options (1)*, and *Table 8: Power divider options (2)*), it has been concluded that a 4-channel chip, and in particular Minicircuit's SCA-4-20+, would be the most interesting solution. The arguments for such a decision have been that this part has one of the lowest unbalances (both in phase and amplitude), the lowest losses, and the second lowest area, even though it is the most expensive and its typical isolation between channels is neither too high or too low in comparison to the other component's.

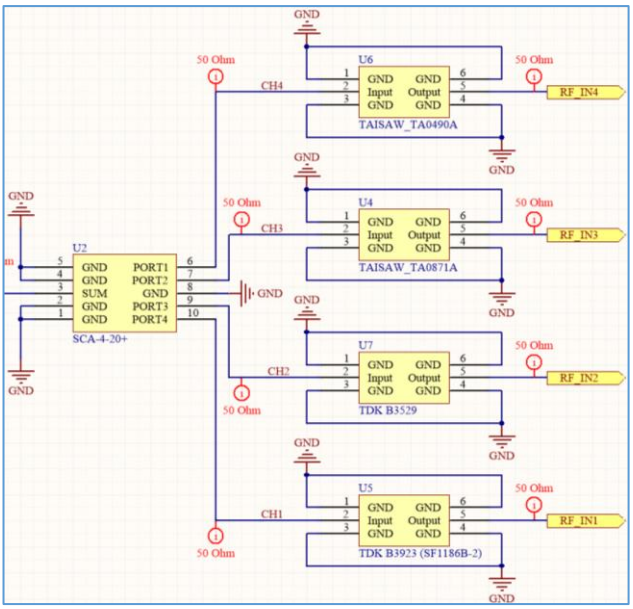

Figure 35: Power divider and SAW filters

Table 7: Power divider options (1)

Manufacturer Part Number (MPR)	Manufacturer	Channels	Frequency [GHz]		Isolation [dB]		Phase unbalance [°]
			Min	Max	Typ	Max	
SCA-4-20+	Mini-Circuits	4	1.00	2.00	15	8	5
SBTC-2-25+ /L /LX+ /X+	Mini-Circuits (A)	2	1.00	2.50	20	14	14
TCP-2-33+ /X+	Mini-Circuits (B)	2	1.00	3.00	18	15	5
PD0922J5050S2HF	Anaren (C)	2	0.95	2.15	10	N/A	3
SBTC-2-25+ /L /LX+ /X+	3x 2-Channel A	4	1.00	2.50	20	14	28
TCP-2-33+ /X+	3x 2-Channel B	4	1.00	3.00	18	15	10
PD0922J5050S2HF	3x 2-Channel C	4	0.95	2.15	10	N/A	6

Table 8: Power divider options (2)

MPR (as in the previous table)	Amplitude unbalance [°]	Total loss S1 [dB]		Total loss S2 [dB]		Total loss S3 [dB]		Total loss S4 [dB]		Package [inches]	Cost [$]
		Min	Max	Min	Max	Min	Max	Min	Max		
SCA-4-20+	0.9	6.80	7.31	6.44	6.97	6.33	6.94	6.84	7.38	0.250 x 0.300 x 0.045	7.00
SBTC-2-25+ /L /LX+ /X+	1.2	3.80	4.10	3.83	4.63	N/A	N/A	N/A	N/A	0.166 x 0.150 x 0.155	2.00
TCP-2-33+ /X+	0.9	3.70	4.12	3.76	4.53	N/A	N/A	N/A	N/A	0.160 x 0.150 x 0.160	2.00
PD0922J5050S2HF	0.3	3.50	3.80	35	3.8	N/A	N/A	N/A	N/A	0.079 x 0.051 x 0.021	0.74
(3x) SBTC-2-25+ /L /LX+ /X+	2.4	7.70	8.20	7.66	8.73	7.66	8.73	7.66	9.26	0.332 x 0.300 x 0.155	6.00
(3x) TCP-2-33+ /X+	1.8	7.30	8.24	7.41	8.65	7.41	8.65	7.52	9.06	0.320 x 0.300 x 0.160	6.00
(3x) PD0922J5050S2HF	0.6	7.00	7.60	7.00	7.60	7.00	7.6	7.00	7.60	0.158 x 0.300 x 0.021	2.22

Furthermore, the filters have been required so the original RF signal can be selected from the required bands, preventing nearby interferences and their harmonics from reaching and potentially saturating the following stages. In particular, SAW filters have been chosen because of their sharpness and how well they perform in subsampling architectures operating in high interference environments. Regarding the SAW filters, it is important to mention that the selection process has taken into account not only the bands but also the footprint and availability of the filters, meaning that products available in the market with the most common footprint have been chosen for this board. This way, it is possible to easily replace the filters by others with similar specifications (in case of availability issues) or others with different ones (in case of working with a different set of RF bands) without having to change the design itself so both costs and delays can be minimized. On a final note regarding the SAW filters, although it is true that including them in the board may limit the options compared to those of the GN3S_PMOD Board (where the Bias Tee, the power divider, and the SAW filters were excluded from the board), taking into consideration their dimensions (and by consequence the ease with which they can be manually soldered/de-soldered) and how other components can be found that fit in the design (as explained a few lines above), including them in the board seems to be the best solution in order to minimize the total dimensions of the receiver.

It is also worth mentioning that the outputs of the ASIC providing the GNSS data to the MicroHeader connectors, and consequently to the MicroZed Board, have been designed so they can work both in digital single end or analog differential modes, this feature being determined via firmware. However, for the initial version, only the single end functionality will be tested.

4.2.2 Layout

Once the schematics have been completed, the following step has been to generate an appropriate PCB layout, phase during which the board's dimensions, structure, and component placement have been defined. Taking into consideration the complexity of the design and its constraints, this part of the project has been subcontracted to Metro Logic Incorporated.

The first design requirement that has been imposed has been to have dimensions as close to those of the MicroZed Board as possible, so both boards can be nicely stacked. Secondly, the amount of layers should be minimized in order to not only optimize the size but also the cost of production. Thirdly, considering the boards should mate via the MicroHeader connectors, all components except for said MicroHeaders should be mounted on the top layer, and these connectors on the bottom one. Moreover, all the jumpers should be as close to the edge as possible, oriented in such a way that if they have to be replace by right angle alternatives, they would stick out of the board for an easy operation. Furthermore, the sensitive RF parts should be protected by the RF Shield (especially the RF Front-End chip, the SAW filters for the RF lines, the oscillator, and their respective passive components). The final requirement has been regarding the PCB base material, as it affect the design of the layer stack and that of some of the traces which need specific impedances (in particular the RF lines and the differential pairs). On that note, two materials are commonly used, namely FR-4 and Roger, being Roger a much higher quality series. However, due to Roger being also much more expensive and this project being the first iteration (or prototype version), it has been decided to design the layout for an FR-4 board in order to lower the overall cost.

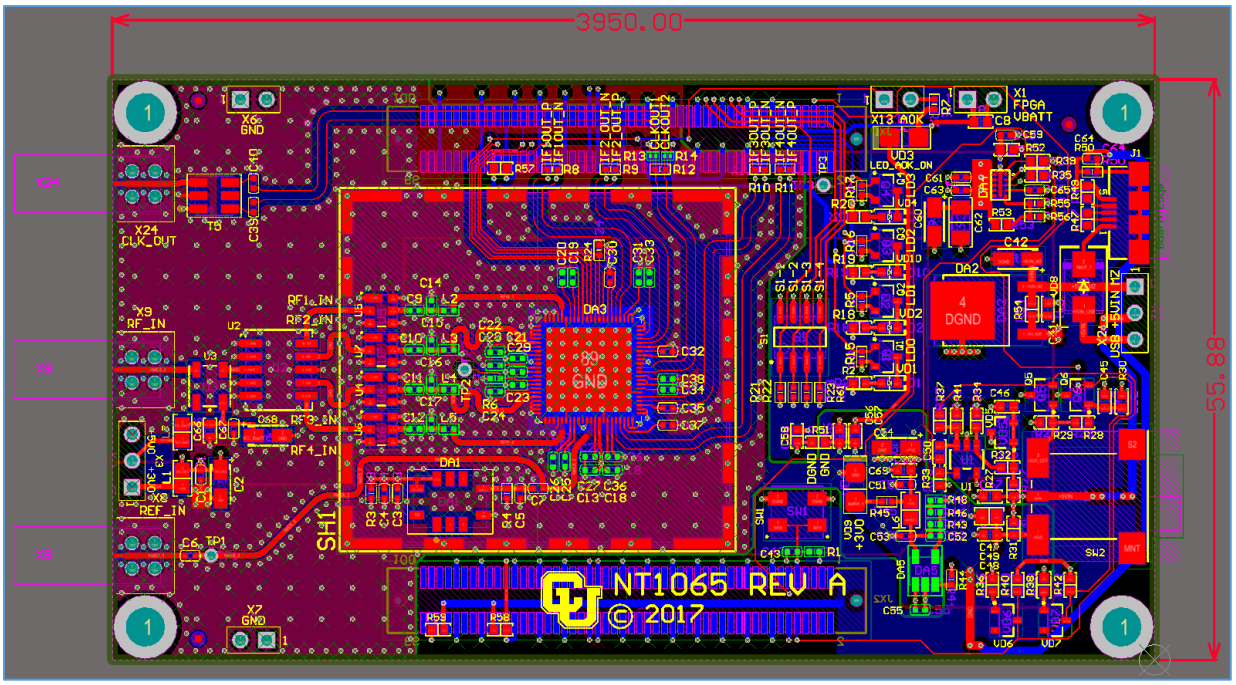

Figure 36: New generation 2-board receiver layout design

The results of the layout design phase can be observed in the picture above (see *Figure 36: New generation 2-board receiver layout design*). As can be seen and in accordance with the requirements, the resulting layout has been a bit smaller than the MicroZed it has to be mated with (note that the X dimension in the figure above is in mils and the Y in millimeters), and only 4 layers have been needed. Furthermore, it is also appreciable that the MicroHeader connectors are placed at the center, right where the MicroZed has its own, and two different ground planes have been used for the analog RF section (left side) and the digital (right side). Moreover, it can also be seen how the jumpers are all parallel to the edges allowing right-angle pieces to stick out, and the RF shield (which will require some mechanical modifications, namely removing the two middle tabs from the left side, in order to allow the RF lines to reach in) covers the sensitive RF parts. The results of adapting the layout design to the reference material for FR-4 can be seen in the picture below (see *Figure 37: New generation 2-board receiver layer stack design*). In addition to said layer stack, special fabrication notes have been mentioned in the Special Assembly Notes so the RF lines and the differential pairs on layer 1 have 50[Ω] and 200[Ω] respectively (specifically 0.6[mm] thickness and 0.17[mm] ground separation for RF lines, and 0.12[mm] thickness and 0.75[mm] separation between each other for differential pairs).

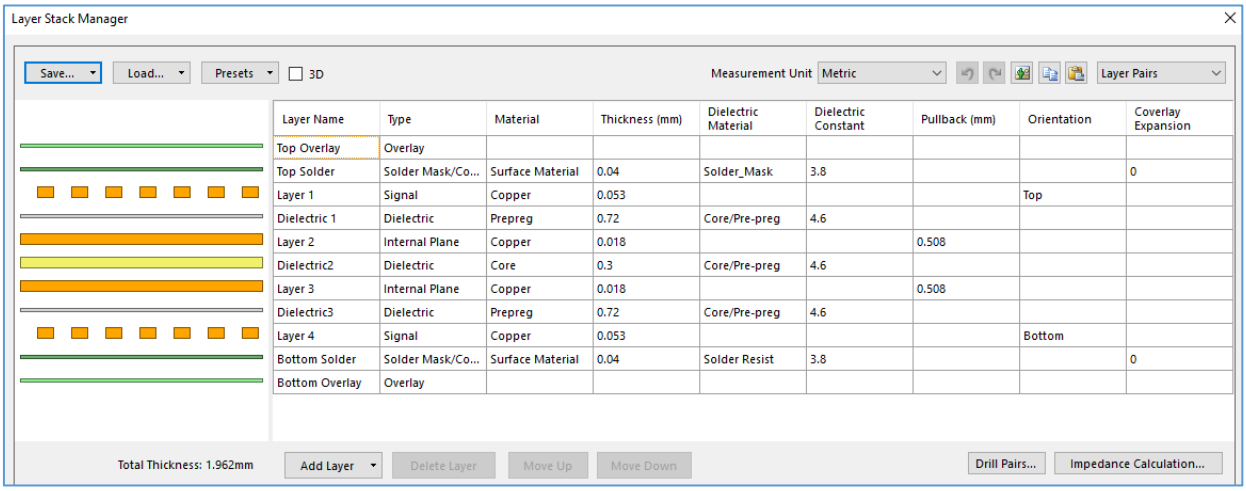

Figure 37: New generation 2-board receiver layer stack design

For more details regarding the layout files, board and traces dimensions, and component placement, see *8.4 Annexure 4 – NT1065_MicroZed's Layout*.

4.3 First Iteration – Manufacturing and Testing

Similarly to the manufacturing and testing process carried out for the SiGe modules (see chapter *3.4 Manufacturing and Testing*), a manufacturing phase has been initiated as soon as the layout has been completed. Below in this section are the details of the manufacturing activities that have been carried out during this project.

4.3.1 Manufacturing

As mentioned in the introduction of this phase (see chapter *3.1 Introduction*), only the electronics side of the receiver has been manufactured due to time and budget constraints. Therefore, the same steps that had been carried out for the SiGe modules have again been replicated. Below is the list of said steps:

- File preparation.
- Manufacturer research.
- Production quotation.
- Order placement.

In regards to the preparation of all the required files for PCB production, they have been listed below (see the end of *8.3 Annexure 3 – NT1065_MicroZed's Schematics* and/or the end of *8.4 Annexure 4 – NT1065_MicroZed's Layout* in order to be able to obtain the original files):

- Gerber files.
- Drill files.
- BOM.
- XY Part Centroid.
- Special Assembly Notes.

For the sake of concision, descriptions of the aforementioned files has not been included in this chapter as they are the same as in Phase 1 (for more details, refer to chapter *3.4.1 Manufacturing*).

Following the preparation of the files, a couple of companies in Colorado (namely Advanced Circuits and Circuits West) have been contacted in order to obtain their respective quotes for building between 4 and 10 boards during a period of 2 to 4 weeks. After a brief discussion with each of them, it has been decided that Circuits West would be the one in charge of production due to them offering a more attractive price, ease of performing split and delayed payments, being recommended by the layout designer personally, and in order to be able to test a new company so these multiple experiences may help making the right decision in future projects.

Once the payment has been done, board production has been initiated for 10 units with a total turn time of 2 weeks. Meanwhile, some components have been sourced by CU Boulder and have been shipped to Circuits West prior to the beginning of the assembly phase. It has been during the board printing phase and while components were being procured that, asides from the two radiation-proof sealed trays of NT1065 (totaling 336 units) sourced with this project in mind, 5 single NT1065s in a static bag left from the previous production of GN3S_PMODs were found in the GNSS Lab. Therefore, after a brief internal discussion, it has been concluded that since this was a first design and production iteration, the new trays would not be opened and instead only five out of the ten new boards would be populated with the NT1065, and if tests were successful the remaining would be populated in the future.

4.3.2 Testing

Taking into consideration that the new NT1065_MicroZed Boards are more complex than the other boards built and tested during this project, a more extensive test plan has been prepared while in the production stage in order optimize the testing phase and not miss any important bit. Furthermore, and in order to get into more detail while performing the tests, this phase has also been divided into three major blocks: Raw Single Tests, Raw Composite Tests, and GNSS Signal Tests.

Before discussing the tests and their results in the following subchapters, it should be mentioned that a couple of minor design flaws have been identified while performing the tests. The first issue has been with the USB protection diode (VD8), which was not the same type of diode as in the reference designs and therefore did not work as expected, so it had to be shorted in order to achieve nominal operation. It should be noted, though, that shorting this protection component has had no effect in terms of operation safety as in this environment it could be ensured that it would not be needed. The other problem has been regarding two N-channel MOSFET's used for processing the OFF and VCCIO_EN signals (Q6 and Q5 respectively), which footprints had the wrong pin assignment, meaning that even though the schematic was right and they fit the components, the signals at two of the pads were switched. These issues have been temporarily fixed on four out of the five boards (so an original could be kept) during the testing phase and long term solutions have been considered for future phases. Finally, the results included in this tests have been those after the issues have been fixed, and therefore only the four modified boards have been considered.

4.3.2.1 Raw Single Tests

In regards to the first block, the Raw Single Tests, these have been performed while the NT1065_MicroZed Board (not connected to the MicroZed Board as seen in *Figure 38: NT1065_MicroZed Board*) has been powered only using the USB connector, so any issues would not damage the MicroZed Board, and consequently the jumper selector X2 has be set to short pins 2 and 3 (input power from USB).

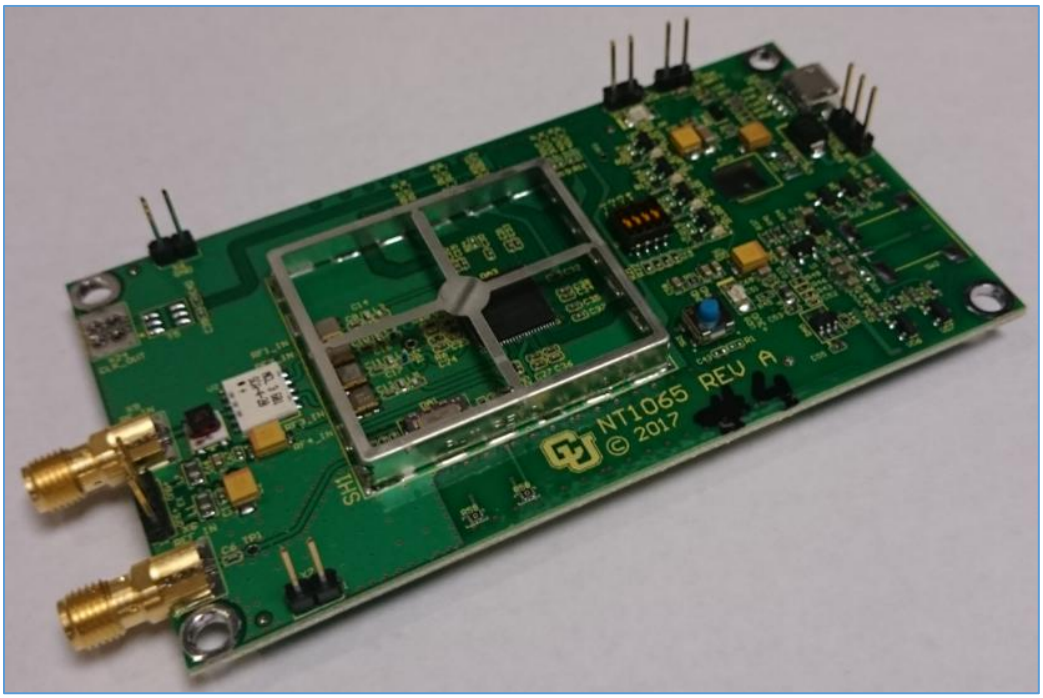

Figure 38: NT1065_MicroZed Board

This test block has been further divided according to the type of measurement, be them basic power supply voltage levels, signal voltage levels, frequency values independent from the GNSS input signals, and frequency response of the SAW filters.

Table 9: Raw Single Tests – Power supply voltages

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
X2	2	Voltage [V]	5.00	5.02	0.01	0.30%	Input voltage.
VD5	1	Voltage [V]	2.50	2.47	-0.03	-1.37%	2.5[V] reference voltage.
SW2	1	Voltage [V]	5.00	5.02	0.01	0.30%	Make sure SW2's pins 1 and 2 are shorted, as SW2 will not be populated.
L6	2	Voltage [V]	3.30	3.27	-0.03	-0.86%	3.30[V] supply voltage. Pin 2 is the uppermost when looking at the board from below. Also VD9 should be lit when in nominal operation.

The testing plan and the results of the first part of this test have been compiled in the table above (see *Table 9: Raw Single Tests – Power supply voltages* for the results of all measurement of this block each averaged over the four boards). In it, it can be easily appreciated that the points of interest have been the power supply jumper selector (or X2, where the USB-supplied voltage can be measured), the 2.50[V] reference generator (or VD5), the output pin of the power ON/OFF switch (or SW2, which has not been populated on this batch), and the 3.3[V] generator (which output can be easily measured on L6).

Table 10: Raw Single Tests – Signal voltages

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
TP1	1	Voltage [V]	1.20	1.17	-0.03	-2.50%	Reference oscillator output voltage.
DA3	79	Voltage [V]	3.30	3.23	-0.07	-2.22%	Output OK signal from the NT1065. If everything is ok (it started up), this pin should be higher than 3.30[V] and the AOK LED should be OFF.
Q6	2	Voltage [V]	0.00	0.01	0.01	0.82%	PWR_EN at LOW, when SW2's pins 2 and 3 are shorted. Pin 2 is the uppermost when looking at the board from below.

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
Q6	2	Voltage [V]	1.80	1.83	0.03	1.76%	PWR_EN at HIGH, when SW2's pins 1 and 2 are shorted. Pin 2 is the uppermost when looking at the board from below.
X9	1	Voltage [V]	3.30	3.27	-0.03	-0.85%	Antenna BIAS DC at 3.30[V] when X3 has pins 1 and 2 shorted.
X9	1	Voltage [V]	5.00	4.98	-0.02	-0.35%	Antenna BIAS DC at 5[V] when X3 has pins 2 and 3 shorted.

About the second part of this first testing block, both the plan and the results have been compiled again in the table above (see *Table 10: Raw Single Tests – Signal voltages* for the results of all measurement of this block each averaged over the four boards). In this case, though, emphasis has been put on signals other than mere power supplies and how some parts of the board react to them. In particular, the interesting measurement points have been the Test Point 1 (or TP1, where the voltage of the reference oscillator's voltage can be obtained), pin 79 of the NT1065 (or DA3, where the output OK signal can be obtained), the output of the PWR_EN generator (or Q6), and the output of the Bias Tee (easily reached through the central pin of the connector X9 in order to test whether or not it sets the DC voltage to both 3.3[V] and 5[V] depending on the selector X3).

Table 11: Raw Single Tests – Signal frequencies

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
TP1	1	Frequency [MHz]	10.00	10.00	0.00	0.00%	Reference oscillator output frequency.
C39	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's CLKOUT1_P. *
C40	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's CLKOUT1_N. *

* Should be able to see the frequency even if the amplitude is considerably low (LVDS).

As mentioned before, the third part of the first tests is that regarding signal frequencies, which plan and results can be seen in the table above (see *Table 11: Raw Single Tests – Signal frequencies* for the results of all measurement of this block each averaged over the four boards). The first relevant measurement is that of TP1 (where the reference oscillator can be checked). The second and last points are the positive and negative lines of the differential pairs containing the output clock (which can be measured from capacitors C39 and C40). In this testing round, digitized IF data lines (which can be measured from resistors R8, R9, R10, and R11, even though these lines will be initially programmed as single end) can not be tested as the NT1065 requires the MicroZed Board to be attached in order for these lines have a specific frequency.

Table 12: Raw Single Tests – Frequency responses

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
U5	5	Frequency Response	1,575.42	1,575.52	0.10	0.01%	GPS-L1 SAW filter.
U7	5	Frequency Response	1,601.50	1,601.60	0.10	0.01%	GLONASS-L1 SAW filter.
U4	5	Frequency Response	1,237.50	1,237.60	0.10	0.01%	GLONASS-L2 SAW filter.
U6	5	Frequency Response	1,228.00	1,228.10	0.10	0.01%	GPS-L2 SAW filter.

The last part of this first set of tests has consisted in measuring the frequency response of the SAW filters. In particular, the central frequency for each of the four filters has been measured (see the results in the table above *Table 12: Raw Single Tests – Frequency responses* for the results of all measurement of this block each averaged over the four boards) in order to demonstrate that they are properly positioned (right order per frequency channel) in order to allow the respective GNSS signals to reach the NT1065.

4.3.2.2 Raw Composite Tests

Secondly, the Raw Composite Tests block has been executed by connecting the NT1065_MicroZed Board and the MicroZed Board (see *Figure 39: NT1065_MicroZed and MicroZed Board stacked*) once single operation has been determined to be optimal and the MicroZed Board has been programmed with its firmware.

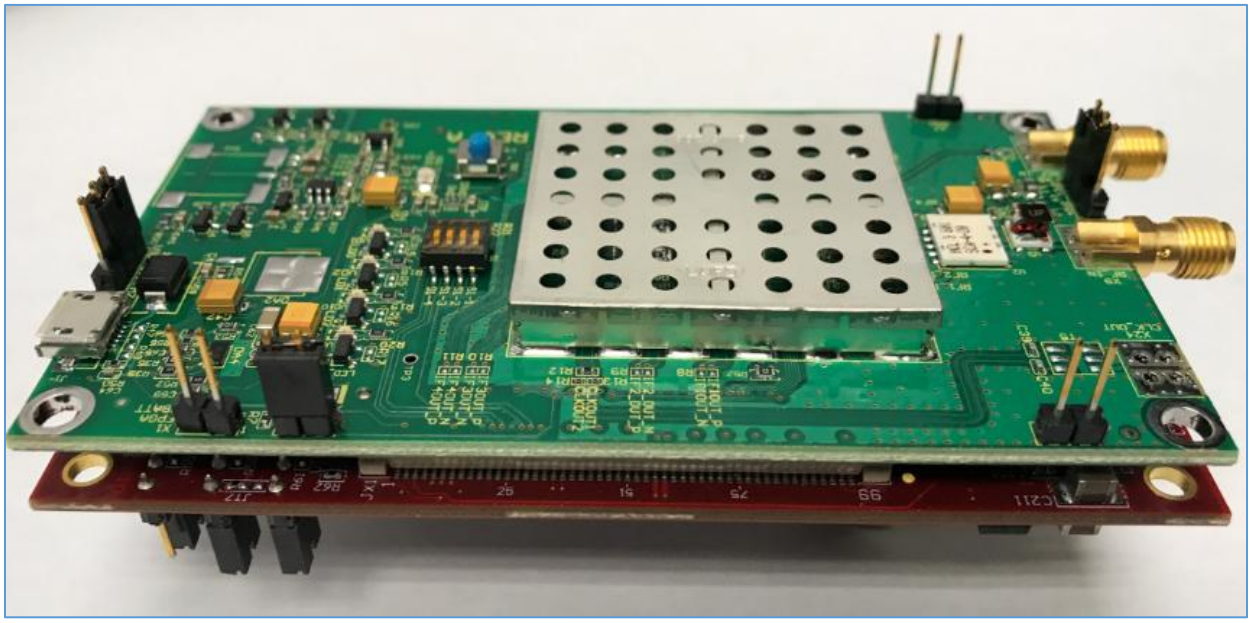

Figure 39: NT1065_MicroZed and MicroZed Board stacked

Originally, the MicroZed was supposed to power the NT1065_MicroZed via the MicroHeader connectors, while the first was powered via USB. However, it has been noted that this option was not possible, and so both boards have been powered via their respective USB connectors). Consequently, the jumper selector has been set to short pins 1 and 2 (input power from USB), even though if the MicroZed Board is powered via Power Jack (not populated during this project), then the NT1065_MicroZed would not require power via USB connector and thus X2 should have its pins 2 and 3 shorted (input power from MicroZed). The same measurements performed in the previous block have been executed again but in this case, thanks to the boards being mated, both have communicated some signals such as VCCIO_EN (MicroZed Board allowing to initiate IO banks' power generation by the NT1065_MicroZed Board), PWR_EN (NT1065_MicroZed board letting the MicroZed Board know it is switched off), and PG_MODULE (NT1065_MicroZed telling the MicroZed Board that the IO banks are properly powered). This signal exchange has been especially interesting to demonstrate that both boards can be mechanically and electrically mated, even though further testing has been required in order to fully verify their electrical and logical compatibility.

Table 13: Raw Composite Tests – Power supply voltages

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
X2	2	Voltage [V]	5.00	4.98	-0.03	-0.50%	Input voltage.
VD5	1	Voltage [V]	2.50	2.48	-0.02	-0.72%	2.5[V] reference voltage.
SW2	1	Voltage [V]	5.00	4.97	-0.03	-0.60%	Make sure SW2's pins 1 and 2 are shorted, as SW2 will not be populated.
DA4	C	Voltage [V]	3.30	3.31	0.00	0.15%	3.30[V] supply voltage. Port C is the furthest to the left when looking at the board from below.
L6	2	Voltage [V]	3.30	3.27	-0.03	-0.86%	3.30[V] supply voltage. Pin 2 is the uppermost when looking at the board from below. Also VD9 should be lit when in nominal operation.

The plan and results of the first part of this second test iteration with power provided by the MicroZed Board have been reported in the table above (see *Table 13: Raw Composite Tests – Power supply voltages* for the results of all measurement of this block each averaged over the four boards). In this case, the only differences have been that the input voltage has been selected and measured by shorting pins 1 and 2 of the jumper selector X2, and a measurement for checking the 3.3[V] output of DA4 has been added (as it depended on the signal VCCIO_EN provided by the MicroZed Board). Needless to say, the other measurements have also been performed as in the previous phase in order to verify the overall stability while mated.

Table 14: Raw Composite Tests – Signal voltages

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
TP1	1	Voltage [V]	1.20	1.15	-0.05	-3.85%	Reference oscillator output voltage.
DA3	79	Voltage [V]	3.30	3.23	-0.07	-2.06%	Output OK signal from the NT1065. If everything is ok (it started up), this pin should be higher than 3[V] and the AOK LED should be OFF.
Q6	2	Voltage [V]	0.00	0.01	0.01	0.81%	PWR_EN at LOW, when SW2's pins 2 and 3 are shorted. Pin 2 is the uppermost when looking at the board from below.
Q6	2	Voltage [V]	1.80	1.89	0.09	4.78%	PWR_EN at HIGH, when SW2's pins 1 and 2 are shorted. Pin 2 is the uppermost when looking at the board from below.
DA4	A2	Voltage [V]	0.00	0.02	0.02	0.72%	PG_MODULE at LOW, when 3.30[V] are not properly generated by DA4.
DA4	A2	Voltage [V]	2.97	2.79	-0.18	-5.98%	PG_MODULE at HIGH, when 3.30[V] are properly generated by DA4.
X9	1	Voltage [V]	3.30	3.27	-0.03	-1.03%	Antenna BIAS DC at 3.30[V] when X3 has pins 1 and 2 shorted.
X9	1	Voltage [V]	5.00	4.97	-0.03	-0.65%	Antenna BIAS DC at 5[V] when X3 has pins 2 and 3 shorted.

Similarly to the previous part of this second test iteration, the same tests as in the first one have been repeated, this time adding a couple of measurements for High and Low PG_MODULE (generated by DA4, and which indicates to the MicroZed Board that the 3.3[V] are stable and ready to be used by the IO banks). The results of these test have been compiled in the table above (see *Table 14: Raw Composite Tests – Signal voltages* for the results of all measurement of this block each averaged over the four boards).

Table 15: Raw Composite Tests – Signal frequencies

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
TP1	1	Frequency [MHz]	10.00	10.00	0.00	0.00%	Reference oscillator output frequency.
C39	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's CLKOUT1_P. *
C40	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's CLKOUT1_N. *
R8	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF1OUT_P. **
R8	2	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF1OUT_N. **
R9	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF2OUT_P. **
R9	2	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF2OUT_N. **
R10	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF3OUT_P. **
R10	2	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF3OUT_N. **
R11	1	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF4OUT_P. **
R11	2	Frequency [MHz]	53.00	53.00	0.00	0.00%	NT1065's IF4OUT_N. **

* Should be able to see the frequency even if the amplitude is considerably low (LVDS).
** Even if level transitions are random (noise), the frequency should still be observable.

Next, the frequency measurements have been repeated in order to check frequency stability of the signals as before independently of the power source and without significant interferences (see results in the table above *Table 15: Raw Composite Tests – Signal frequencies* for the results of all measurement of this block each averaged over the four boards).

Table 16: Raw Composite Tests – Frequency responses

Component Designator	Pin	Meas. Type [Units]	Exp. Value	Meas. Value	Difference (Exp. - Meas.)	Difference (%)	Notes
U5	5	Frequency Response	1,575.42	1,575.52	0.10	0.01%	GPS-L1 SAW filter.
U7	5	Frequency Response	1,601.50	1,601.60	0.10	0.01%	GLONASS-L1 SAW filter.
U4	5	Frequency Response	1,237.50	1,237.60	0.10	0.01%	GLONASS-L2 SAW filter.
U6	5	Frequency Response	1,228.00	1,228.10	0.10	0.01%	GPS-L2 SAW filter.

Again, in order to verify that being mated to the MicroZed Board has no effect on the filters, their frequency responses have been double-checked and compiled (see *Table 16: Raw Composite Tests – Frequency responses* for the results of all measurement of this block each averaged over the four boards) with power coming from said board.

4.3.2.3 GNSS Signal Tests

The remaining testing block has consisted in a logical evaluation of the boards, meaning that the output files generated after nominal operation of the two have been analyzed. The original test plan has been designed in order to thoroughly analyze the files so every single frequency band from each board is tested (see *8.5 Annexure 5 – NT1065_MicroZed's Original GNSS Signal Test Plan*). However, by the end of the project an issue with IO ports of the MicroZed Boards acquired from Avnet has been discovered: the currently available revision (Rev F) had issues with data communication ports. This has been verified once communication tests with a computer have been initiated, and confirmed once the new revision schematics (Rev G) have come out with several modifications to the aforementioned ports.

In order to fix this communication issues and progress with the board testing, the firmware has been edited allowing some data extraction, which resulted in being extremely slow so the original tests could not be executed. However, due to it being so slow, the final GNSS signal tests have been simplified to gathering only a few seconds of data for one band (GPS-L1 signal generated with a simulator in the laboratory) so the amount of information to be transferred could be minimized while still providing valuable evidence of good performances.

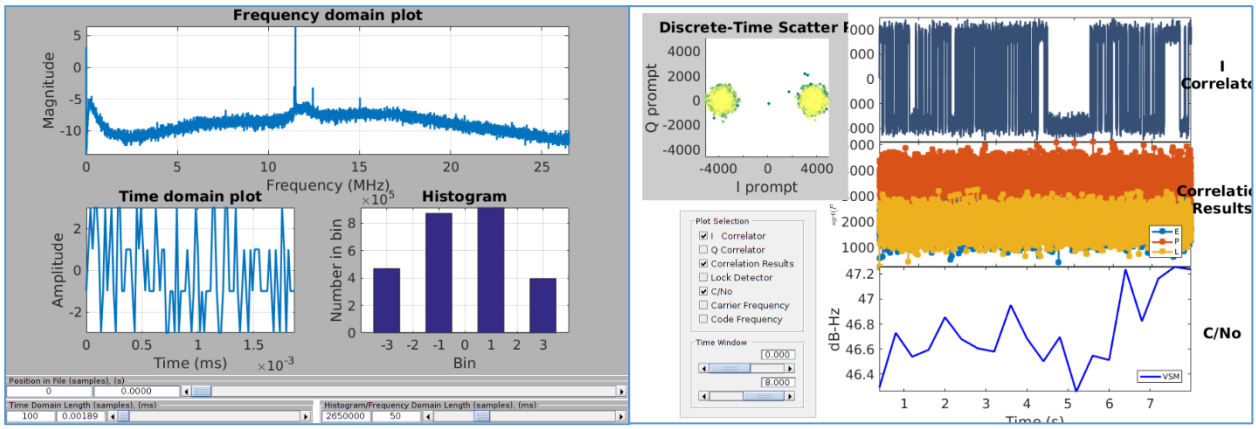

Figure 40: GPS-L1 generated spectrum and tracking results

As can be seen in the figure above (see *Figure 40: GPS-L1 generated spectrum*), a small interference has been received by the designed board around the data of interest (see the Frequency domain plot) However, further analysis of the data such as that of the Histogram, the Discrete-Time Scatter plot, or the C/N_0 (this one showing very similar results to the SiGe modules) has led to the conclusion that said interference spike was not affecting the signal much. In addition and regarding the origin of said spike, it is safe to say that it does not seem to be originated by the board because there is no component inside the RF shield that operates at approximately 11.5[MHz] (the clock works at 10[MHz], the NT1065's sampling frequency is 6.625[MHz], and the output data frequency is 53[MHz]). Therefore, the interference may have gotten into the system through the filters in the RF path. However, thanks to it being a spike (small bandwidth) with not so high amplitude, it has not saturated any of the components so the GPS

signal has still been received with enough power. Finally, the effects of the interference have been mitigated by decoding the GPS signal, process which at its turn has "encoded the spike and spread its power and originally small bandwidth.

Therefore, after testing the GPS-L1 branch of the receiver, knowing the NT1065 is properly configured and the SAW filters have been populated in their respective branches correctly, and assuming the latter all operate nominally, all the remaining branches for signal reception (starting at the signal divider) should provide the correct data for obtaining a final navigation solution with any of the GNSS signals for which the board has been designed. Nonetheless, it is recommended to perform the original tests planned for the GNSS signals once a new revision of the MicroZed Board is available at the laboratory or, at the very least, perform said tests with the old version but with an increased amount of time and for all the possible signals, either fully demonstrating the correctness of the design.

4.3.2.4 Conclusions

Regarding the phase as a whole and compared to the testing done to the SiGe modules (see *3.4.1.1 Electronics*), the ones carried out for the NT1065_MicroZed Boards have been a lot more extensive and detailed. Furthermore, once the tests described in the previous chapters (see chapters *4.3.2.1 Raw Single Tests*, *4.3.2.2 Raw Composite Tests*, *4.3.2.3 GNSS Signal Tests*) have been completed and the results analyzed, the following conclusions have been drawn.

First of all, the initial electronic tests (both the single and the composite) have been a key element to identify two design flaws (part of choice for diode VD8, and MOSFET's Q5 and Q6 having a wrong pin assignment in their footprints), which have been fixed before proceeding with the data compilation provided in this report. Said data has successfully proven that the design and production phases have been properly fixed, resulting in the measured parameters being in average within a 2.50% and 5.98% of the expected ones and the worst individual cases being 5.00% and 6.94% for each testing phase respectively.

Secondly, the original GNSS Signal Test have not been possible to perform due to errors in the design of the MicroZed Boards currently available at the GNSS Lab. Nonetheless, a new and simplified test plan including a shorter period of time and a simulated GPS-L1 signal has been carried out. During this test an interference spike has been logged around the data of interest (dismissed due to not having much effect on the signal) and similar C/N0 values as those of the SiGe modules (around 46.5[dB-Hz]) have also been recorded.

Despite encountering some errors (in both the NT1065_MicroZed and the MicroZed Board designs), it has been concluded that the current modified boards can operate as expected at the beginning of the project. Furthermore, the results obtained during these tests can also be used for future testing phases as reference values, even though it is recommended to perform some extended tests by either analyzing the remaining signals for a longer period of time or using the new MicroZed Board revision (Rev G).

5. Phase 3: Additional Work

5.1 Introduction

5.1.1 FPGA – System on Chip Boards

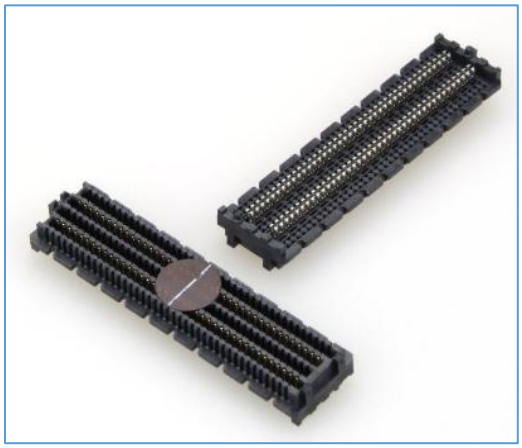

Figure 41: FMC connector

VMEbus Manufacturers Group, which became VMEbus International Trade Association (VITA) in 1984, has the goal of uniting manufacturers and users through the acceptance and implementation of open technology standards. In regards to the FPGA boards and their connectors, VITA 57.1[31] defines the FMC connector as the standard (see *Figure 41: FMC connector*), which is a High Pin Count (HPC) 400 IO high-speed array system also mechanically compatible with Low Pin Count (LPC). Furthermore, VITA has promoted the creation of the FMC Marketing Alliance (some of the members being Intel Corporation, Samtec, and Xilinx) with the goal of establishing an ecosystem of interested parties which creates and encourages name recognition as well as grow adoption of the FMC connector.

As a result from the aforementioned standard, some of the most renowned FPGA – System on Chip board manufacturers include the FMC as the main connector. Moreover, although FPGA IO typically operated at 5[V], it is being brought down to lower values (3.3[V], 1.8[V], 1.5[V], 1.2[V], and even lower) for newer generations.

Finally, and in order to conclude this introduction with some examples, some of the most well-known and broadly used FPGA – System on Chip Boards are Xilinx's Zynq Ultrascale+, MicroSemi's SmartFusion2, Intel's Arria 10, Avnet's ZedBoard and its smaller evolution the MicroZed Board (see chapter *4.1.2 The ZedBoard and the MicroZed Board*), the latter requiring a carrier board that provides the conversion from MicroHeader to FMC.

5.1.2 The Interface Board

The GNSS Lab has been recently working with a GNSS receiving setup consisting of the GN3S_PMOD Board (see chapter *4.1.1 The GN3S_PMOD Board*) connected to the PMOD ports of the ZedBoard (see chapter *4.1.2 The ZedBoard and the MicroZed Board*), so the FMC interface was not needed at all. Moreover, the most recent efforts have been put on developing a carrier card for the new and smaller MicroZed Board (again more details in chapter *4.1.2 The ZedBoard and the MicroZed Board*) as described in this report (see chapter *4 Phase 2: The New Generation Receiver*).

However, in order to continue doing research with the GN3S_PMOD and increase its compatibility with other FPGA boards that have the standardized FMC connectors but not the right PMOD setup, it has been agreed that an initial step would be to design and build an Interface Board that would adapt from the

[31] ANSI/VITA 57.1-2010 - http://www.vita.com/Standards

PMOD connectors working at 3.3[V] to a male FMC connector that could work at a variety of voltages (such as 3.3[V], 1.8[V], and so on). Therefore, having such a board that also uses standard and common packages for it components (especially regarding a voltage regulator used for setting the output voltage) would be extremely beneficial in order to allow almost any FPGA board to be used in conjunction with the GN3S_PMOD.

Contrary to the initial intentions, it should also be mentioned that manufacturing and testing have been excluded due to this project depending on another project executed by other members of the GNSS Lab and also due to budget constraints. However, all files required for manufacturing the boards have been generated and quotes from both Advanced Circuits and Circuits West have been obtained, becoming this way ready to initiate production activities.

5.2 The Interface Board - Hardware Design

In regards to the hardware design of the Interface Board, this phase has consisted mostly in an initial assessment of what kind of boards should be interconnected, their respective voltage values, and the different power supply sources. Once the analysis has been completed, it has been concluded that the GN3S_PMOD Board will be used along with the Xilinx's Zynq Ultrascale+, working at 3.3[V] and 1.8[V] respectively. Afterwards, once the voltages and all the signals have been identified, a market research has been carried out in order to determine the types and amount of voltage regulators that would make the most attractive solution. Moreover, considering that one of the signals to be transferred is a LVDS, a similar analysis has been performed for the LVDS receiver. Next, once all the components have been determined and their connections completed, the FMC connector pins have been reviewed in order to optimize their usage and make sure shorter paths and no crisscrossing occurred. Lastly, the layout of the board has been prepared and all the files needed for production have been generated, even though the boards have not been built as explained above (see chapter *5.1.2 The Interface Board*).

5.2.1 Schematics

Below in this chapter the different parts of the schematic have been displayed in detail and discussed, bringing up some points considered while designing them. Nonetheless, for a complete version of the schematics refer to *8.6 Annexure 6 – Interface Board's Schematics*.

The first part of the schematic that has been implemented have been the two identical PMOD connectors' schematic drawings and footprint but with different signals assigned to each pin, (see *Figure 42: PMOD connector*). This way, all the signals could be labeled and the other parts of the schematics could be more easily developed.

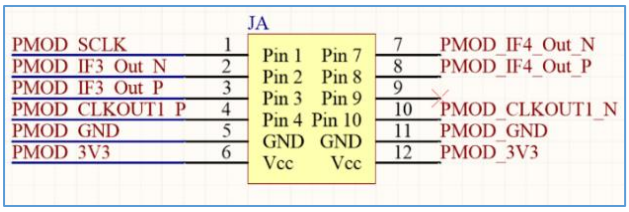

Figure 42: PMOD connector (JA)

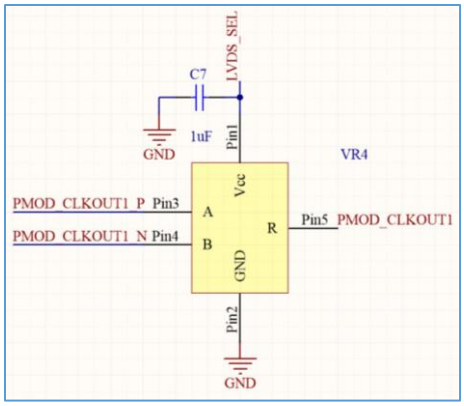

Figure 43: LVDS receiver

Secondly, it should be borne in mind that, even if most of the signals on this board are single-ended (meaning they are referenced to ground), there is one which is a LVDS, namely the clock signal. For this reason, before translating its voltage to the appropriate level, it has had to be converted to single end using a LVDS receiver (see *Figure 43: LVDS receiver*). During the selection process an important parameter that has had to be taken into account has been the operational frequency, as the signal to be converted is, as its name suggests, a clock. However, in case the Interface Board is supposed to be used with a single end clock as an input instead, the LVDS receiver can be easily removed pre-production (or in other word not populated) and pins 3 and 5 can be shorted in the schematics or, if the design is not supposed to be altered, manually post-production.

Another part of the schematics would be that including the actual voltage translation. Taking into consideration that a maximum of 16 signals had to be converted from 3.3[V] to 1.8[V], there were multiple options in terms of channels per chip. After comparing multiple combinations, in particular in terms of costs and total area, it has been concluded that the most interesting solution would be to use two 8-channel translators even if some lines had to be left unconnected at the end. In the figure to the right (see *Figure 44: Voltage translator (VR1)*), the result of one voltage translator in particular can be seen, having its input (Vcca) and output (Vccb) voltage references and the required passive components according to the datasheet.

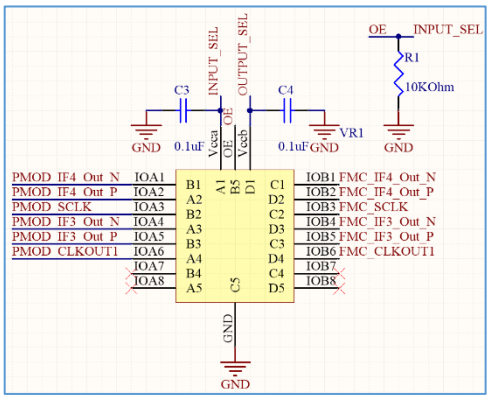

Figure 44: Voltage translator (VR1)

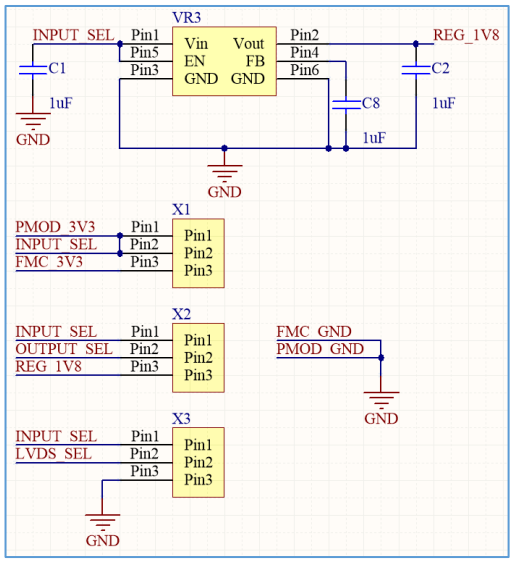

Figure 45: Power supply unit

One last part of the schematics has been the unit in charge of controlling all the power options for this board. As can be seen in the figure to the left (see *Figure 45: Power supply unit*) it comprises mainly three blocks, namely a voltage regulator (top), three jumper selectors (bottom left), and a common ground setting (bottom right). The simplest in terms of reasoning would be the common ground, which is basically a short between the grounds provided by each board so all signals have the same reference. Next, the first of the three jumper selectors (X1) is used to choose which board provides the 3.3[V]. Moreover, taking into consideration that if the voltage is provided by the FMC connector it should also be forwarded to the PMOD. To achieve this, X1's pins 1 and 2 have to be shorted, meaning that effectively this selector is just for enabling power supply from the FMC connector. Secondly, the middle jumper

selector (X2) is used in order to allow more flexibility of applications to the board, as it allows selecting the output voltage level between the input voltage (resulting in no voltage translation whatsoever) or the output of the voltage regulator (thus translating the signal voltages to the desired value). The last selector (X3) is only used as an ON/OFF option for the LVDS receiver as if no LVDS signal has to be translated, the chip has no purpose on that specific build and should consequently not be powered. A voltage regulator has also been added in order to generate the 1.8[V] reference for the voltage translators, taking as input the voltage selected from either the PMOD or the FMC connector.

On a side note regarding the schematics, it should be mentioned that the FMC connector and its footprint have also been designed, but these have not been included in this report due to the component being too big (it has 400 pins) and it would not be properly displayed.

As mentioned above, a few iterations have been performed involving the schematics and the layout in order to rearrange pin connections (signals on each pin) in order to optimize route distribution or, in other words, minimizing length and trace intertwining.

5.2.2 Layout

The board layout for this part of the project has had mainly five design constraints. The first constraint has been that the board's dimensions should be as small as possible (especially on the Y axis) in order prevent extra unnecessary board surface and allow it to fit when connected to other boards with much free space around the FMC or PMOD connector. Secondly, the connectors have to be placed on two opposing ends, having the FMC at the bottom and the PMODs at the top. Also regarding the PMODs, they had to be spaced an exact distance, as it is the configuration used by other boards. Next, the board should have the minimum amount of layers possible, ideally 2 in order to minimize the total cost. Next, all components (except the aforementioned connectors) should be placed on the bottom layer so layer changes with vias can be avoided and the price minimized.

Designing the layout for this board has not been an independent phase from the schematic design after the completion of the latter. Instead, after having an initial version of the schematics, also an initial version of the layout has been prepared where components and traces have been placed while trying not to oversize trace lengths and preventing both crisscrossing and possible "isles" of copper planes isolated from the rest of the plane. Following, a signal-pin rearrangement has been carried out in order to further optimize the traces. Afterwards, vias have been created in the remaining and unavoidable copper "isles" so it would be possible to interconnect those using simple lines on the opposite layer. As a last step, the ground (bottom) and 3.3[V] (top) copper planes have been poured and it has been ensured that there were no areas left unconnected.

As displayed in the picture to the right (see *Figure 46: Interface board's layout (bottom view)*), board dimensions have been minimized as much as possible, especially regarding the Y axis so the board support does not get in the way when connecting it to another board. Furthermore and regarding the second constraint, it can be observed how the surface-mounted FMC connector (JC) has been placed on the bottom layer, while the thru-hole PMOD connectors (JA and JB) have been placed on the upper layer (note the reversed silkscreen designators). In regards to the separation between PMODs, it has been ensured that there is a distance 22.784[mm] between the same pin of the two connectors, which is the exact same one as for the GN3S_PMOD Board. In terms of layer optimization, the minimum amount of layers needed by this board has been two, having all the components except for the PMODs and the jumper selectors on the bottom layer. It is also worth mentioning that the jumpers have been placed parallel to the edge as in the NT1065_MicroZed Board, so the same design may be used even if they are replaced by their right-angle counterparts.

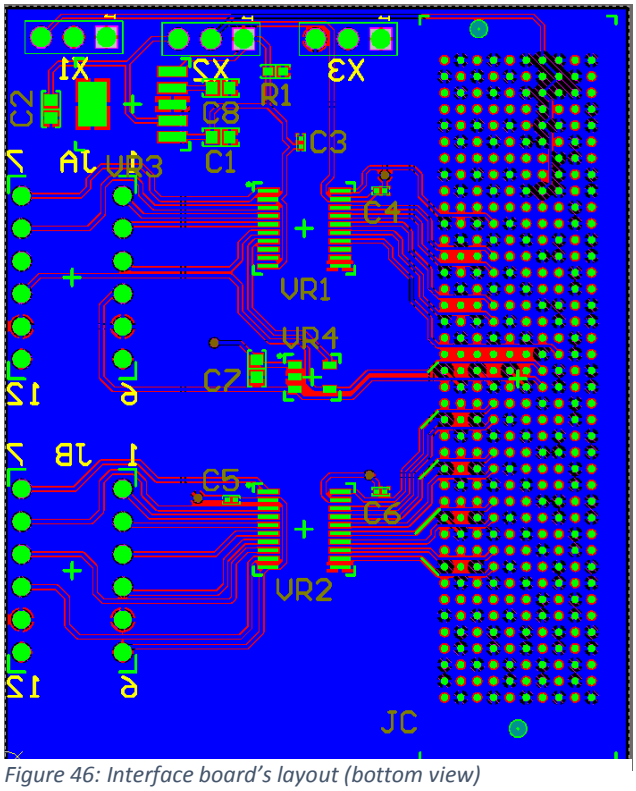

Figure 46: Interface board's layout (bottom view)

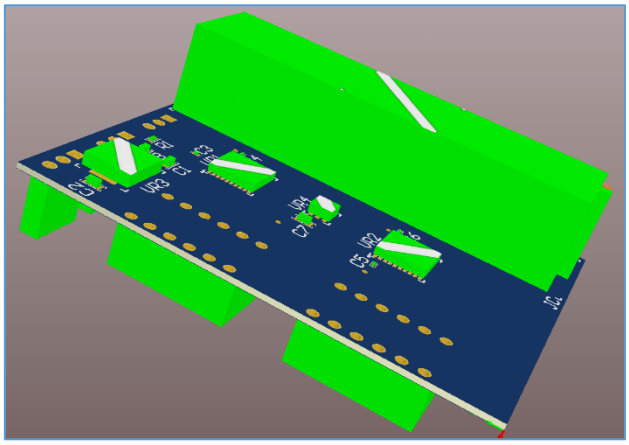
Figure 47: Interface Board's 3D model (upside down)

Finally, in the figure below (see *Figure 47: Interface Board's 3D model (upside down)*), a 3D view of the design can be observed. As mentioned, the picture has been rotated 180° on the X axis, so the two right-angle PMOD connectors and the jumper selectors can be seen on the upper layer, the first being centered in the image and the latter on the left-hand side.On the other hand, the FMC connector and the remaining components can be located on the bottom layer, the connector being at the back and the other parts being closer to the PMOD connectors.

For a complete version of the layout, refer to *8.7 Annexure 7 – Interface Board's Layout*.

6. Conclusions and Future Steps

6.1 Conclusions

From a general point of view, this project has been especially rewarding not only in terms of GNSS and electronics technical knowledge, but also regarding the practice in electronics and 3D design software. Furthermore, a rather important part of the project has consisted in logistics such as obtaining components and quotes and placing orders, and has consequently helped further develop negotiation and communication skill with different suppliers and manufacturers.

Continuing with project-wide observations, it's worth stressing the importance of early decision-making, a good version control, and file sharing system for such engineering projects with many people involved and especially when parts of it are outsourced. It has been noticed during the project that often times the latest version had to be double-checked. Moreover, it should also be mentioned that some simple decisions were still made quite late into the project, which made it harder to update all the existing files, such as that time when a thru-hole component has been replaced by its surface-mounted counterpart.

As a final general point, it has been discussed multiple times among the research team how part manufacturers usually only provide physical dimensions on paper (datasheet), but almost never provide a digital file which includes 3D models, footprints, etc. Although back in the days having a datasheet would suffice, now that computerized design is so extended it would make much more sense for manufacturers themselves to provide all the digital files along with the datasheet on any online electronics store. This way, instead of having to build the files when needed or having to look into a multitude of libraries which often times do not include what is needed, each individual datasheet would have everything attached to it. On this topic, it is true that some companies have been providing this kind of files lately, but this activity should be promoted in the sector.

In regards to the specific conclusions for each of the phases executed throughout this project, these can be found in the following subsections.

6.1.1 Phase 1

The main goal of Phase 1 has been to obtain fully functional SiGe Modules with their respective casings while getting to know the research group and the different systems and parts involved in both the design, building, and operation of these modules.

In regards to production and testing, and taking into account previous experiences while manufacturing these modules, 1 or 2 were expected to fail (because of either component malfunction or soldering/routing issues). Although when performing the first tests some modules did show non-nominal behavior (such as unstable AGC values or wrong position acquisition or simply were unable to acquire a position solution), it has been later demonstrated with a second testing round that the previous issues were due to environmental conditions and that the modules were all in fact in perfect standing. On the other hand, the 3D models for the housings that have been printed at CU Boulder have also shown great fitting, but they seemed to be a bit too brittle. However, this brittleness has been assumed to be due to the manufacturing method (3D-printing) and the material (VeroWhitePlus), and has been completely fixed as assessed from the mass-production samples manufactured by injection-molding. It should be noted that since the mechanical part of the modules (casings) was not as critical, it has been delayed until the

electronics proved to work fine, and consequently complete tests for all the housings have not been included in this report even if all the parts have been received right at the end.

Regarding the secondary objectives of this phase, it has been possible to deeply understand the design of the modules, their firmware and the different pieces of software needed for setting them up and operating them. This way, VID/PID pairs have been changed in order to distinguish the newly built modules from the older and functioning, and the older damaged ones. Also the Matlab analyzing software has been modified in order to accommodate the newer frequencies used by the latest modules.

6.1.2 Phase 2

During the execution of this phase some errors have been detected, errors that can be classified into two different categories: NT1065_MicroZed errors and MicroZed errors.

In regards to the first group, two design flaws have been spotted when performing the initial tests. The first one consisted in the USB protection diode (VD8) not being the exact same kind of diode as specified in the reference schematics and it therefore didn't perform as expected. In order to solve this, it has been decided to short the diode as it would never be used as a protection diode anyway (power can never be outputted anyway) and thus nominal operation has been achieved. Secondly, the footprints designed for the MOSFETs Q6 and Q5 (used for processing the OFF and VCCIO_EN signals) had the pin assignment corresponding to the original thru-hole components instead of the chosen surface-mounted. In order to fix this, both transistors have been removed, which means that the NT1065_MicroZed board will always be operating if connected to the power source. As can be observed, these two errors have been temporarily fixed for the current existing boards and only limit their degrees of operation by a small amount. Nonetheless, it has been possible to successfully carry out the first parts of the voltage and frequency tests, obtaining always values as far as 6.94% from the expected results.

Regarding the MicroZed Board design errors, it has been noted during the testing phase that the IO ports were not working as expected and, by the end of the project, a newer design revision has been published for the board with multiple hardware changes in the IO ports that confirmed the initial suspicions. By modifying the firmware and simplifying the tests to only one frequency band (GPS-L1) and a shorter period of time. Thanks to these changes, the tests have provided positive results (with the exception of an interference spike which has been concluded to have little to no effect on the signal) such as similar spectrum plots and C/N_0 as the SiGe modules (around 46[dB-Hz]). Although comparison between the SiGe modules and the NT1065_MicroZed should not be directly made, these similarities suggest that the performance of the other branches should be correct as well. Nonetheless, it is still recommended to perform the extended original tests in order to ensure the overall correctness by either using the MicroZed Boards currently available at the laboratory (highly increased data transfer times) or the newest revision once it is purchased.

In conclusion, it is fair to say that in spite of detecting errors in both the new design and the MicroZed Board, it has been possible to test the new boards in order to find said errors and fix them, so it is possible to know what needs to be changed in future design iterations.

6.1.3 Additional Work

Once the main bulk of the project has been completed, additional work has been carried out in order to support the GNSS Lab. Although originally the goal was to work on the second design iteration, meaning that a single-board solution would be designed, it has been discussed that this would take too much time and would not be feasible and two alternatives have been envisioned: modifying the current design to include an ADC or designing a new Interface Board. It has been decided that the part that would help the GNSS Lab the most at that time would be an Interface Board, which would increase the flexibility of the GN3S_PMOD Board in regards to the amount of FPGA boards it can be used with, and so the ADC part has been left as future steps for Phase 2 (see chapter *6.2.2 Phase 2*).

The design stage has been extremely useful in order to improve schematics and layout design skills while obtaining a design which satisfied all the requirements. Furthermore, PCB printing and assembly quotes have been received from two different Colorado-based companies, but production and testing have been excluded from the project due to it depending on another project and also due to budget constraints. However, it is expected to push the Interface Board forward and manufacture 5-10 units in the near future.

6.2 Future Steps

As explained in some of the previous chapters, this project has been the first iteration of a bigger one. Therefore, there are many steps that were already planned before this project began, some even were meant to be included at first but, due to time and budget constraints, were removed and left for future iterations.

6.2.1 Phase 1

After a successful initial production of 60 modules and having 193 SE4120L left (note that 2 were damaged and lost during production), 180 additional modules were expected to be built at the end of this project's execution. Taking into consideration the costs for building the boards, sourcing the components, and assembling the modules ($1,742.40, $5,016.60, and $ 5,697.40 respectively), with a total turn time of 8 weeks, some payment negotiations have been started in order to initiate production. These negotiations have included suggesting that the GNSS Lab would acquire some additional components in order to lower the parts cost below the $5,000.00 mark, so an initial credit card payment for board printing followed by another credit card payment for the parts and a purchase order for board assembly (the last two one month into production). However, due to summer vacations falling right at the end of this project, there have been significant delays, but it has been possible to reach an agreement, and production has been initiated.

In regards to the plastic casings, mass production has also been completed, after having the initial samples successfully tested and the manufactured being notified. However, the main bulk of parts have only been received, with no time left for an in-depth testing.

Therefore, the following steps to be executed for this phase would be to keep track of the board manufacturing and assembly processes and make sure all issues that may arise are taken care of. Next, once production is completed and the modules are received, these shall be tested for performance as done for the previous 60-unit batch. On the other hand, the plastic casings shall also be assessed in order to dismiss those parts with any major defects. Once successfully both the mechanical and electronic parts

have passed the tests, complete SiGe modules shall be assembled at CU Boulder as instructed to one of the members.

6.2.2 Phase 2

Taking into consideration that the tests carried out in this phase have had to be altered due to some problems with the currently available MicroZed Boards, the first step to take care of in the future would be to perform the originally planned tests, which will either require a much longer execution time or buying the new version of the MicroZed Board.

After completing the tests for the boards built during these project, the very first step should be to further review and edit the design files in order to fix the issues identified while testing (namely the protection diode VD8 and the MOSFETs Q6 and Q5). Moreover, during this review, other parts like the Jumpers (both 2- and 3-pin parts) shall be replaced by other shorter parts as in the MicroZed Board in order to lower the profile of the board.

Furthermore, there are two potential lines of development for the NT1065_MicroZed Board. The first one would consist in a redesign of the board that has been built during this project, so it would be able to accommodate an LVDS 4-channel ADC. The main reason for this change would be that when the NT1065 is configured to output its four IF channels as digital single-end channels, it uses 2-bit internal ADCs, which in some applications might not provide enough resolution. Therefore, if external 12- or 14-bit ADCs (such as the AD9253[32] provided by Analog Devices) are added to the design, it would be possible to select not only between digital and analog outputs, but also different resolutions, highly improving the added value of the receiver.

On the other hand, the other development line would be obtaining a single-board solution by merging the design schematics of the NT1065_MicroZed Board. In order to achieve that, the schematics for the MicroZed Board have already been developed during the execution of this project even though they have not been included as a relevant part to the project. In the future, though, further development shall be carried out in order to select the required parts of the circuitry from the MicroZed Board as well as a rather complete layout redesign in order to accommodate the new components into one single board without compromising other elements of the receiver (mostly the analog high-frequency parts).

[32] Datasheet provided by Analog Devices: http://www.analog.com/media/en/technical-documentation/data-sheets/AD9253.pdf

6.2.3 Additional Work

In terms of the additional work done during this project, it has been mentioned that only the design of the Interface Board has been performed in order to allow a greater flexibility in terms of which FPGA board may be used with PMOD GNSS front-ends (especially the GN3S PMOD Board as it is the one used by the research group here at CU Boulder). Therefore, also bearing in mind that manufacturing files and quotes have already been obtained, the next step to be taken would be to get back to the preferred manufacturer and begin production, followed by testing the boards

The next step in terms of design that has been planned mainly consists on adapting the design so the Interface Boards can be stacked. This way, it will be possible to have multiple signal routing patterns to the FMC connector (different board level versions) so the FMC connector and FPGA usage can be maximized by adding more input channels. In order to achieve this without having to move parts around the board, the following actions should be carried out:

- The jumper selectors should be replaced by their right-angle counterparts.
- A second FMC connector (in this case a female part) should be placed on the upper layer.
- Every single pin of the male FMC should be shorted to its homonym of the female FMC by using vertical vias going through the whole board.
- New stackable boards should all have a unique routing pattern so the new RF inputs are all connected to a different FMC pin compared to the other stackable board that are intended to be used together.
- Potentially, an FMC spacer (board with only a male FMC at the bottom and a female FMC at the top) should be used between Interface Boards to provide additional room for the PMOD connectors if required.

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- NASA, https://www.nasa.gov
- Information and Analysis Center for Positioning, Navigation and Timing, https://www.glonass-iac.ru/en
- ESA, http://www.esa.int/ESA
- Navipedia, http://www.navipedia.net
- GNSS Lab at SAESD, https://ccar.colorado.edu/gnss/
- DigiKey, https://www.digikey.com/
- Avnet, https://www.avnet.com/wps/portal/us
- Xilinx, https://www.xilinx.com/
- NTLab, http://ntlab.com/index.htm
- Several other web pages accessed from google.com

8. Annexure

8.1 Annexure 1 – SiGe's Schematics

Below in this annexure, the complete latest version of the schematics of the SiGe module can be observed (see *Figure 48: SiGe's schematic*).

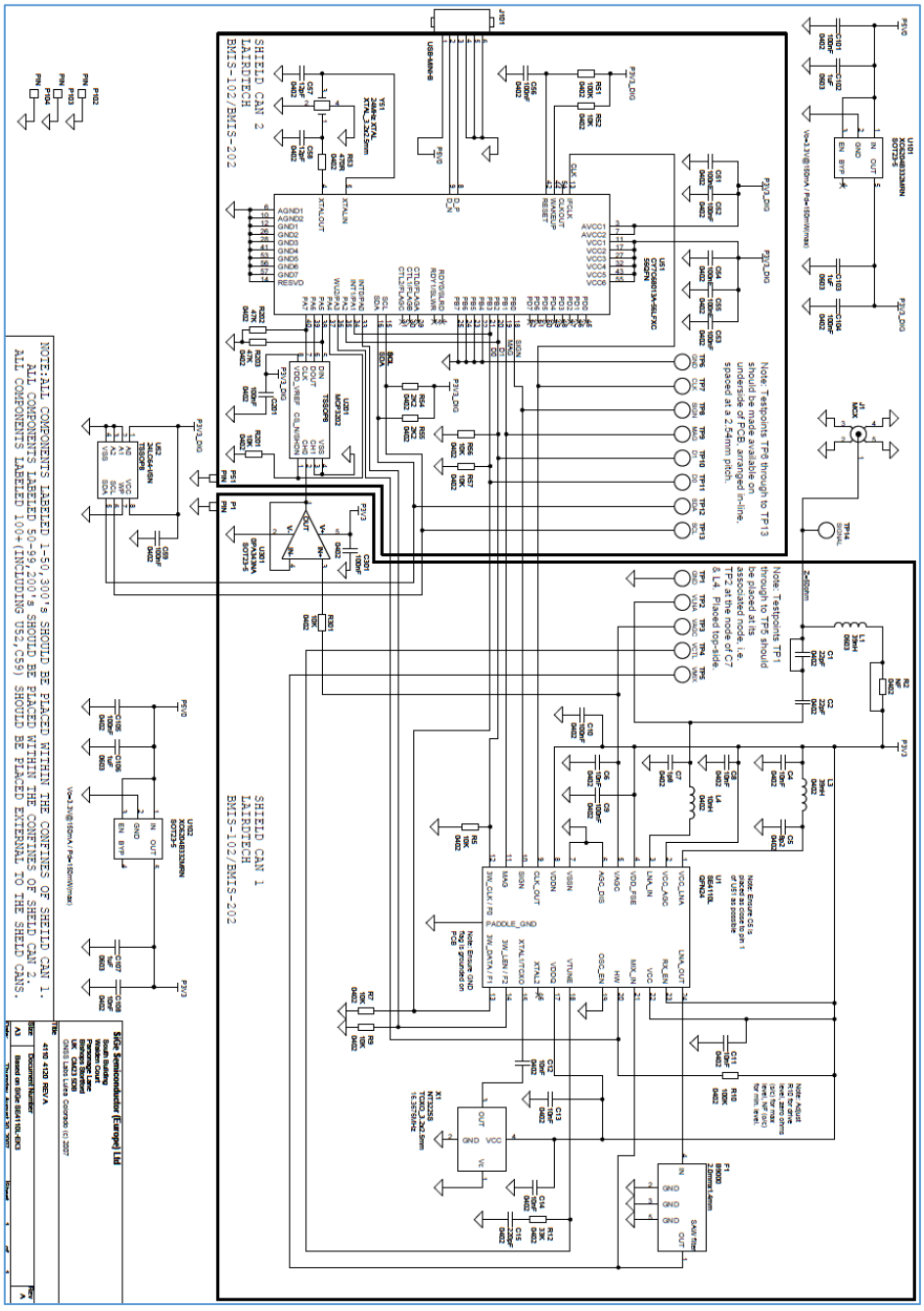

Figure 48: SiGe's schematic

In order to obtain the .pdf versions of the schematics, please contact the author of this report or refer to the DVD provided with the physical copy of this report.

8.2 Annexure 2 – SiGe's Layout

The original design of the SiGe module was done using Zuken's CADSTAR, out of which the following figure has been extracted (see *Figure 49: SiGe module on CADSTAR*).

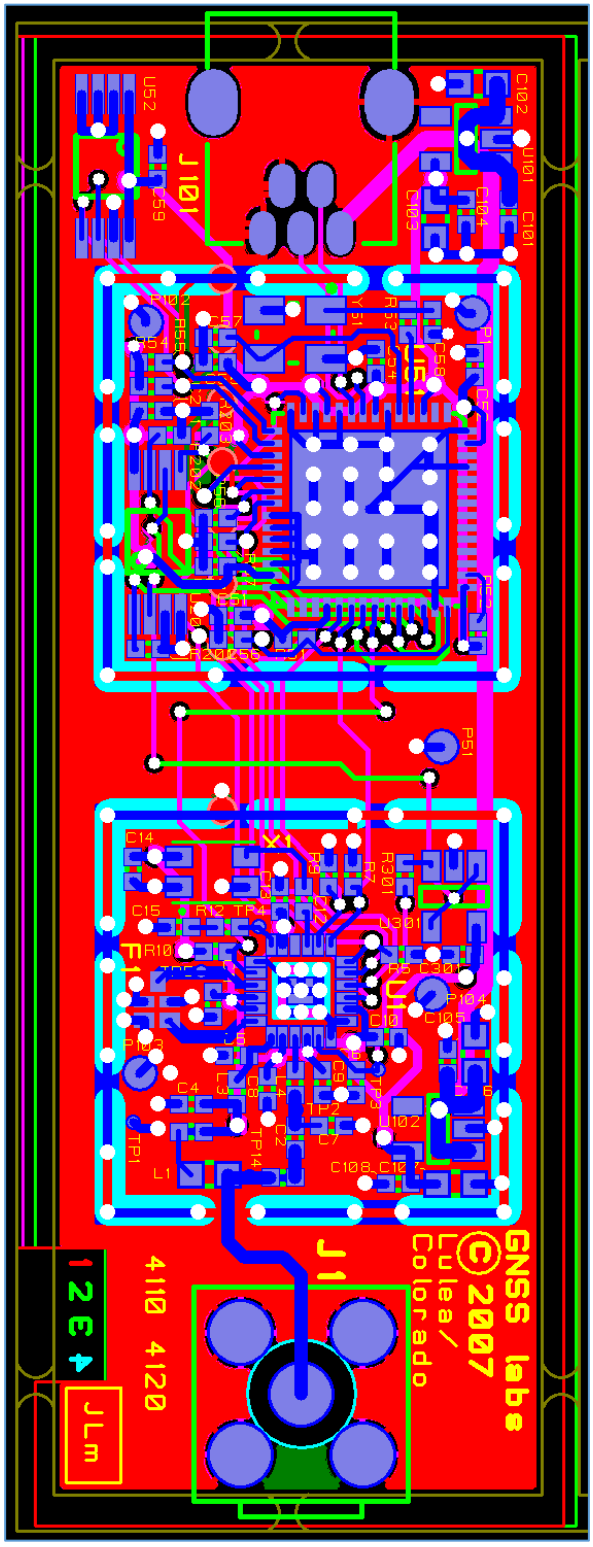

Figure 49: SiGe module on CADSTAR

In order to easily locate each component and find those in the BOM, the figure below (see *Figure 50: SiGe's silkscreen*) represents the SiGe's silkscreen with each of the component designators.

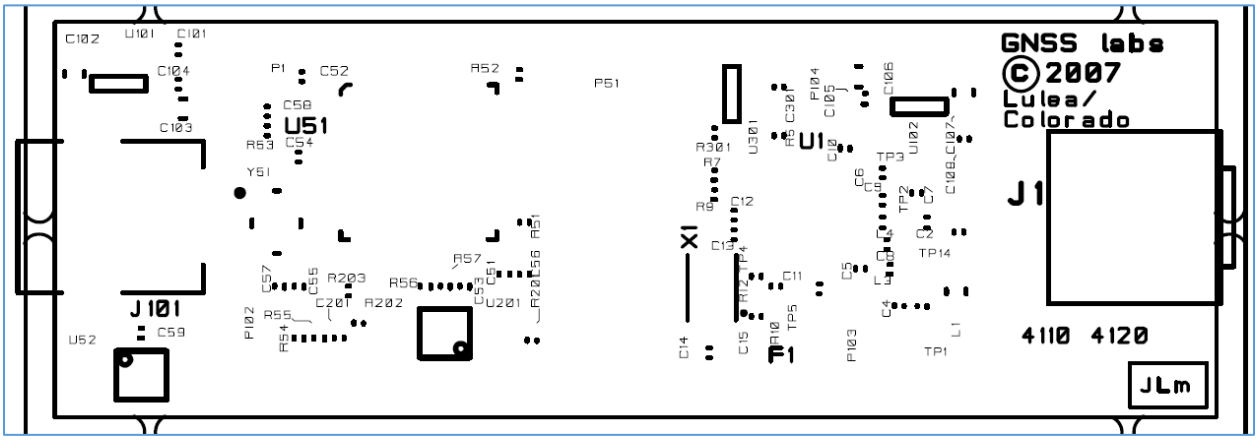

Figure 50: SiGe's silkscreen

The remaining figures (see *Figure 51: SiGe's Layer 1*, *Figure 52: SiGe's Layer 2*, *Figure 53: SiGe's Layer 3*, and *Figure 54: SiGe's Layer 4*) depict the different layers of the module with their routes.

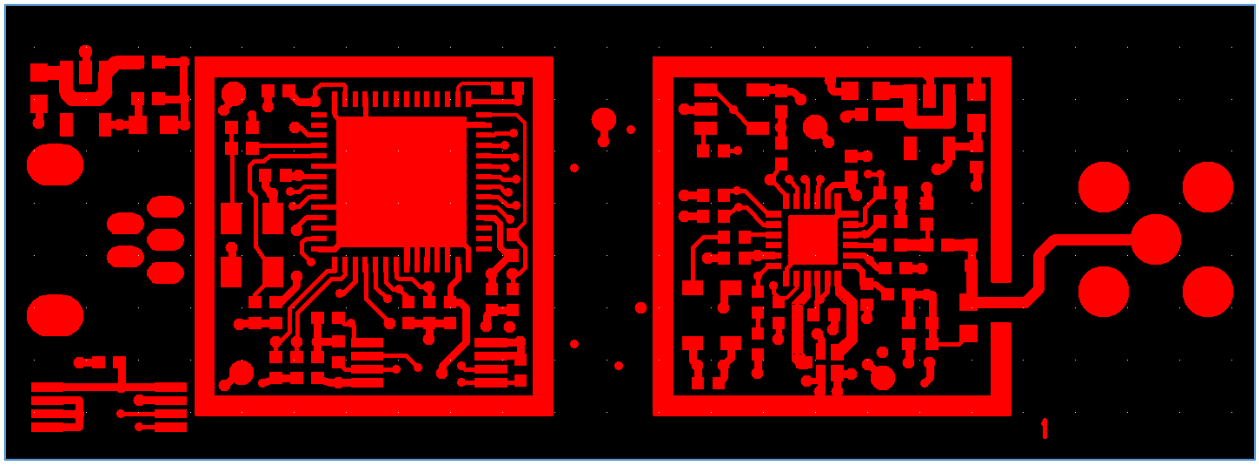

Figure 51: SiGe's Layer 1

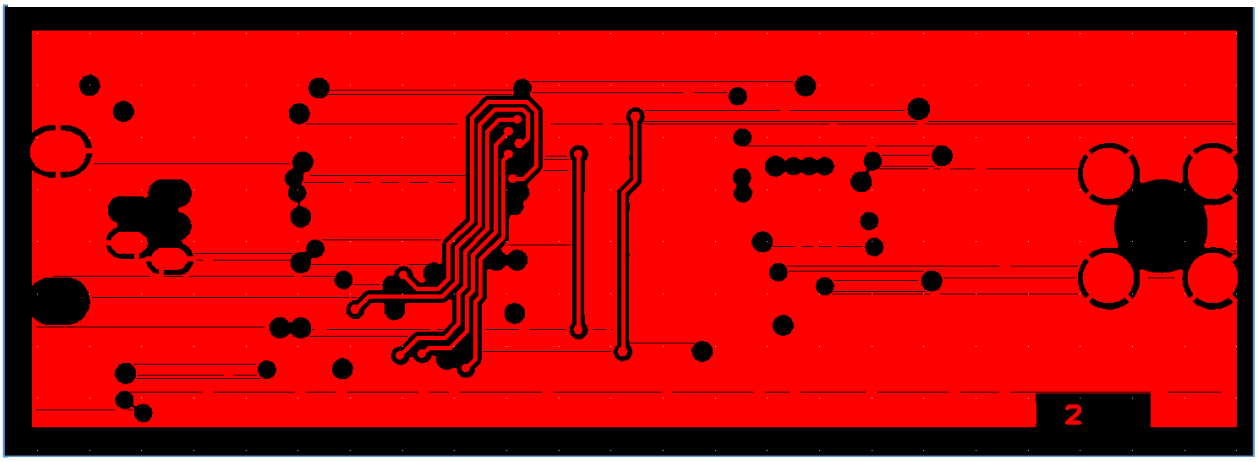

Figure 52: SiGe's Layer 2

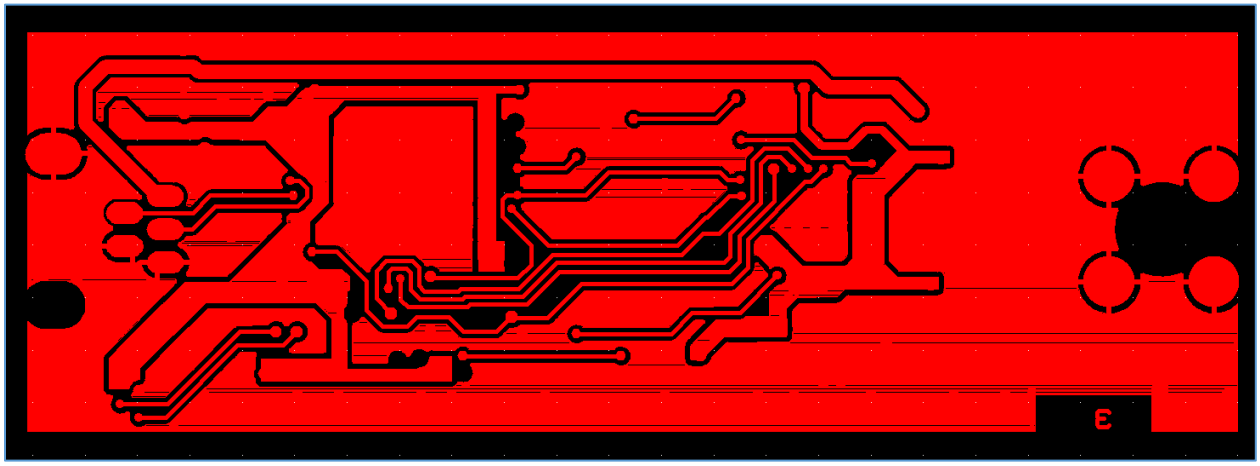

Figure 53: SiGe's Layer 3

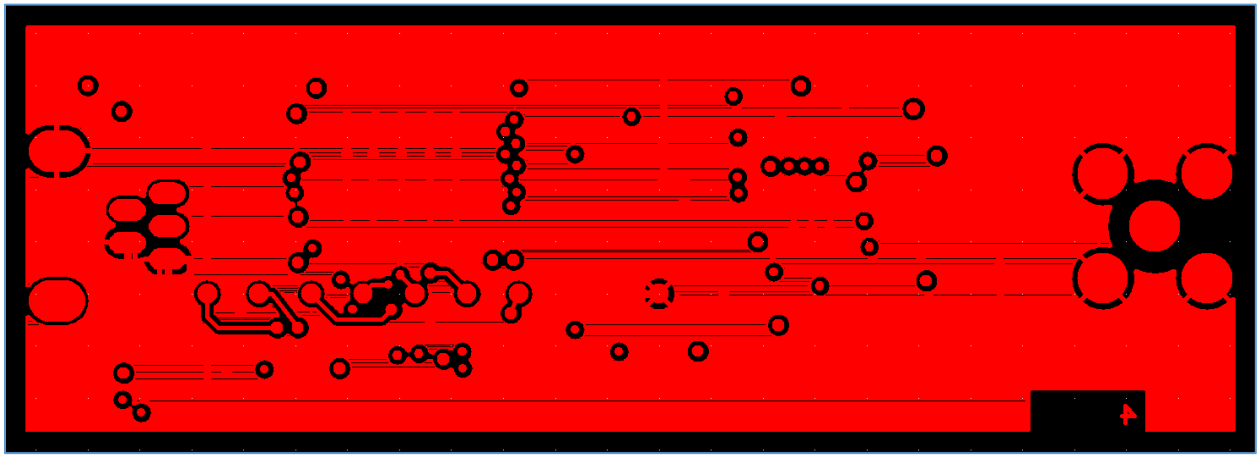

Figure 54: SiGe's Layer 4

Finally, in order to obtain the .pdf versions of the design files as well as the other files required for production, please contact the author of this report or refer to the DVD provided with the physical copy of this report.

8.3 Annexure 3 – NT1065_MicroZed's Schematics

Below in this annexure enlarged images of the NT1065_MicroZed Board's schematics can be found in alphabetical order. The first displays the MicroHeaders along with some LED indicators (see *Figure 55: NT1065_MicroZed's MicroHeaders*).

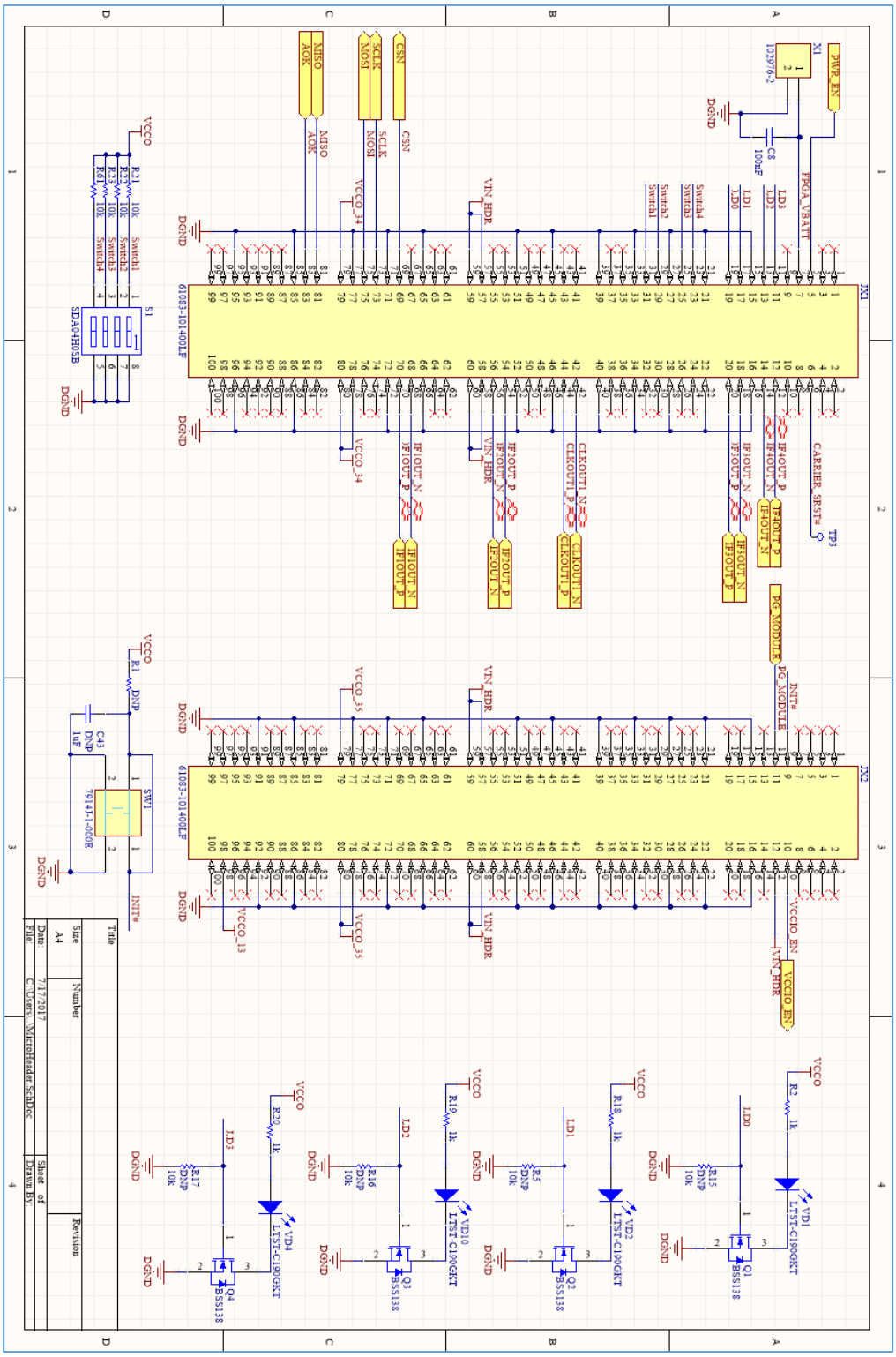

Figure 55: NT1065_MicroZed's MicroHeaders.SchDoc

The following contains details regarding the main ASIC and clock generation (see *Figure 56: NT1065_MicroZed's NT1065_MicroZed.SchDoc*).

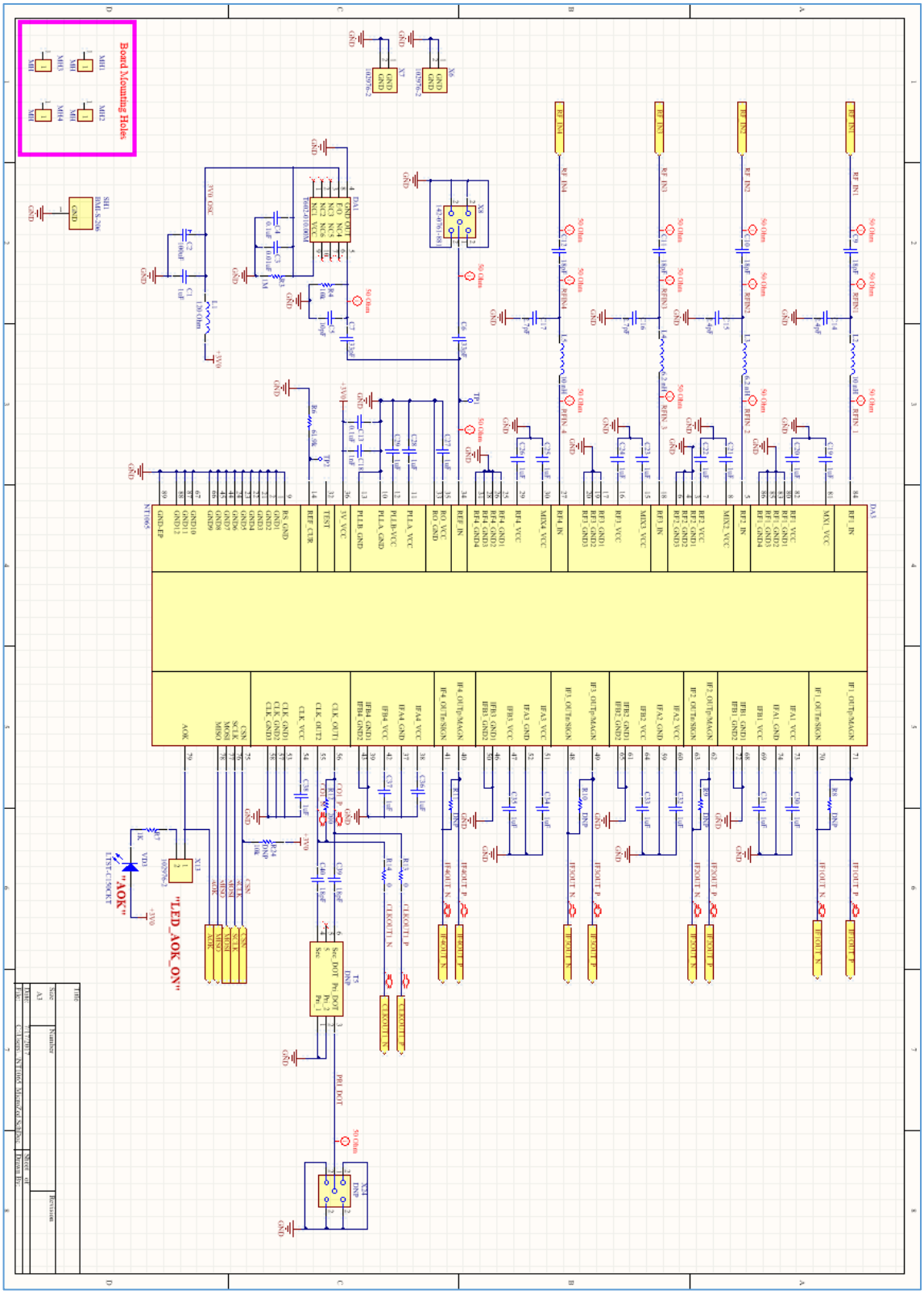

Figure 56: NT1065_MicroZed's NT1065_MicroZed.SchDoc

Below is a picture of the power supply circuitry (see *Figure 57: NT1065_MicroZed's Power.SchDoc*).

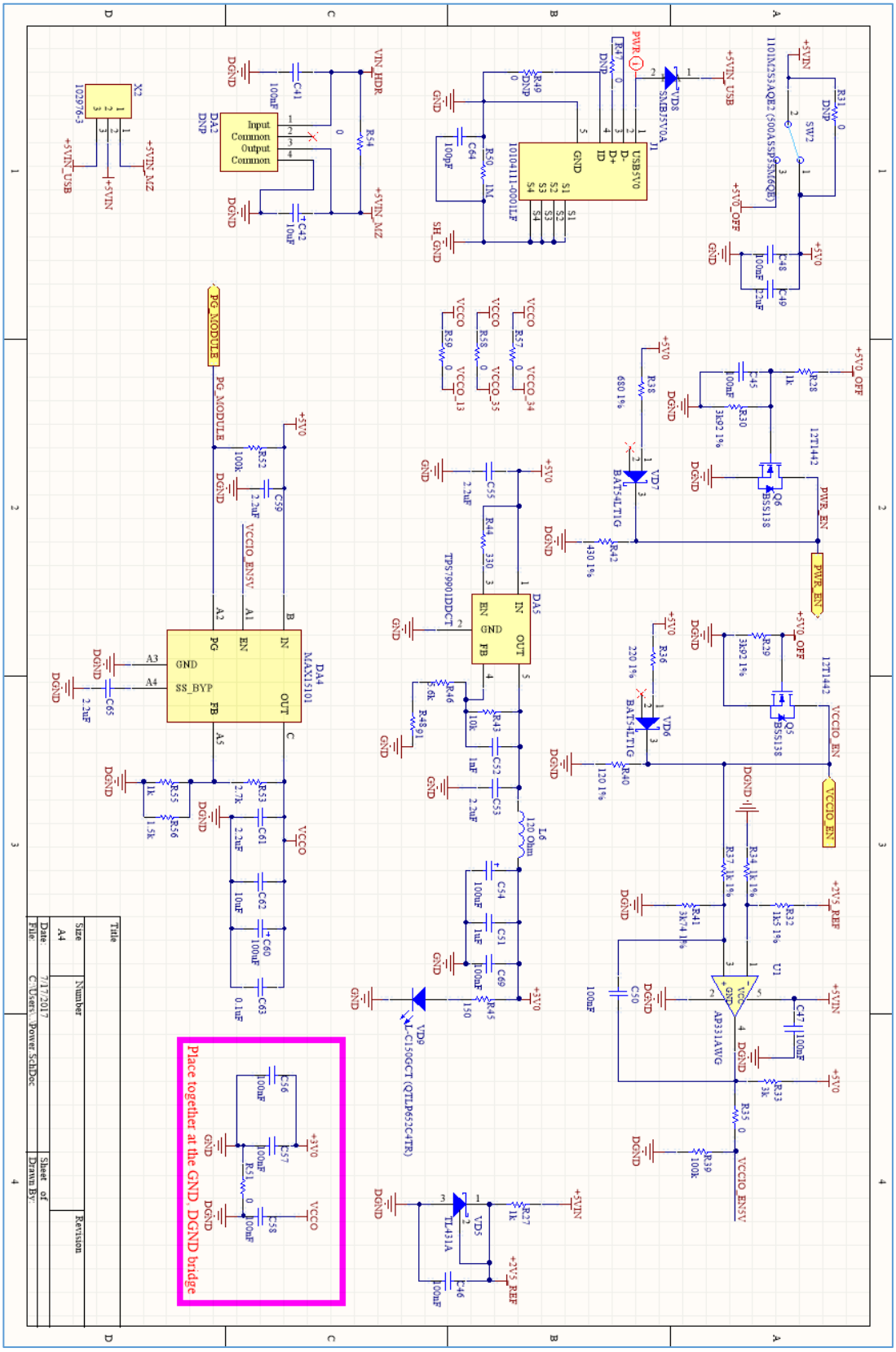

Figure 57: NT1065_MicroZed's Power.SchDoc

Last but not least, the remaining RF components such as the Bias Tee, the power splitter and the SAW filters can be seen in the following picture (see *Figure 58: NT1065_MicroZed's RFInput.SchDoc*).

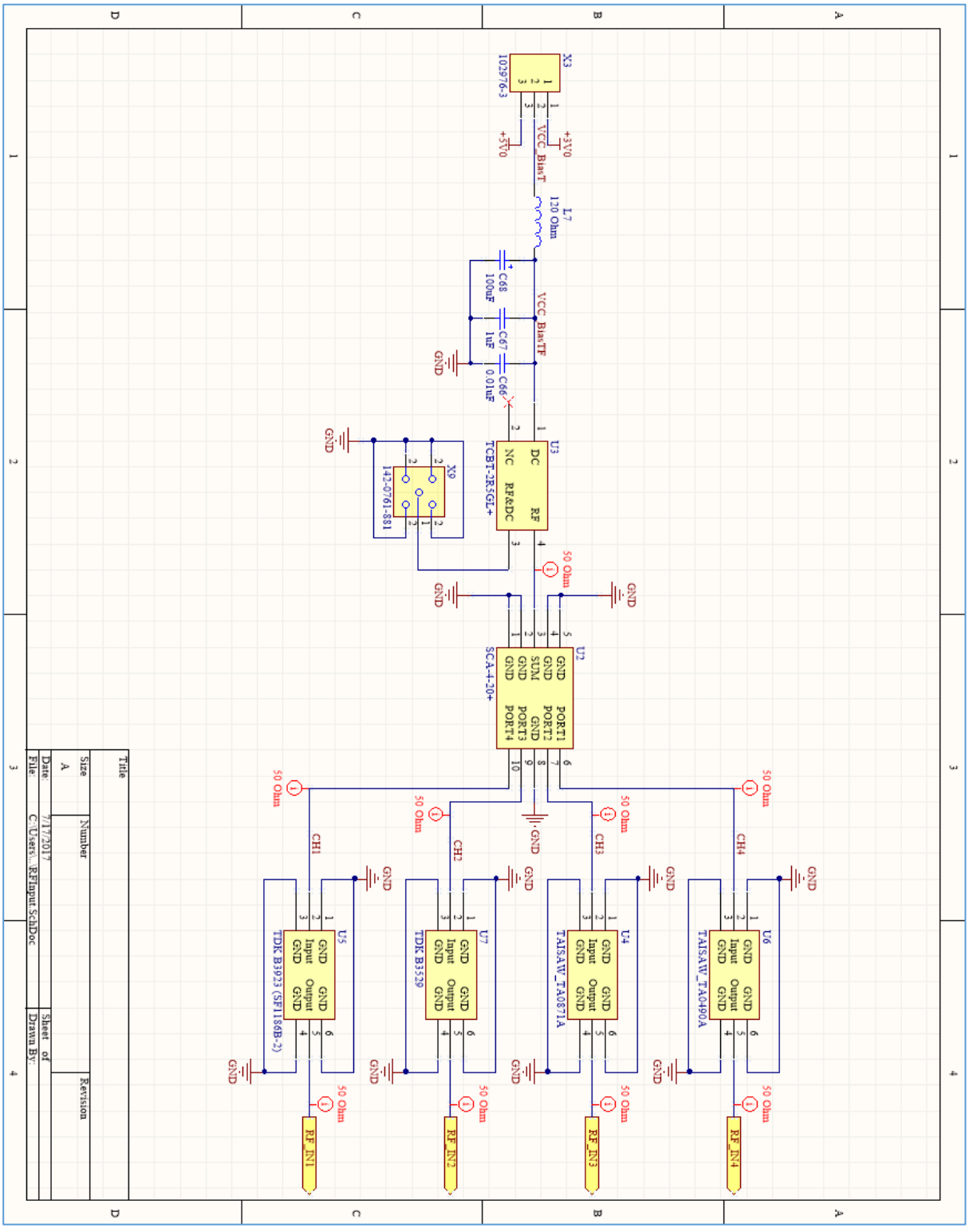

Figure 58: NT1065_MicroZed's RFInput.SchDoc

Finally, in order to obtain the .pdf versions of the schematics, please contact the author of this report or refer to the DVD provided with the physical copy of this report.

8.4 Annexure 4 – NT1065_MicroZed's Layout

This annexure contains more details about the NT1065_MicroZed Board, specifically regarding its layout. The first picture represents an overall view of the layout design (see *Figure 59: NT1065_MicroZed on Altium Designer*).

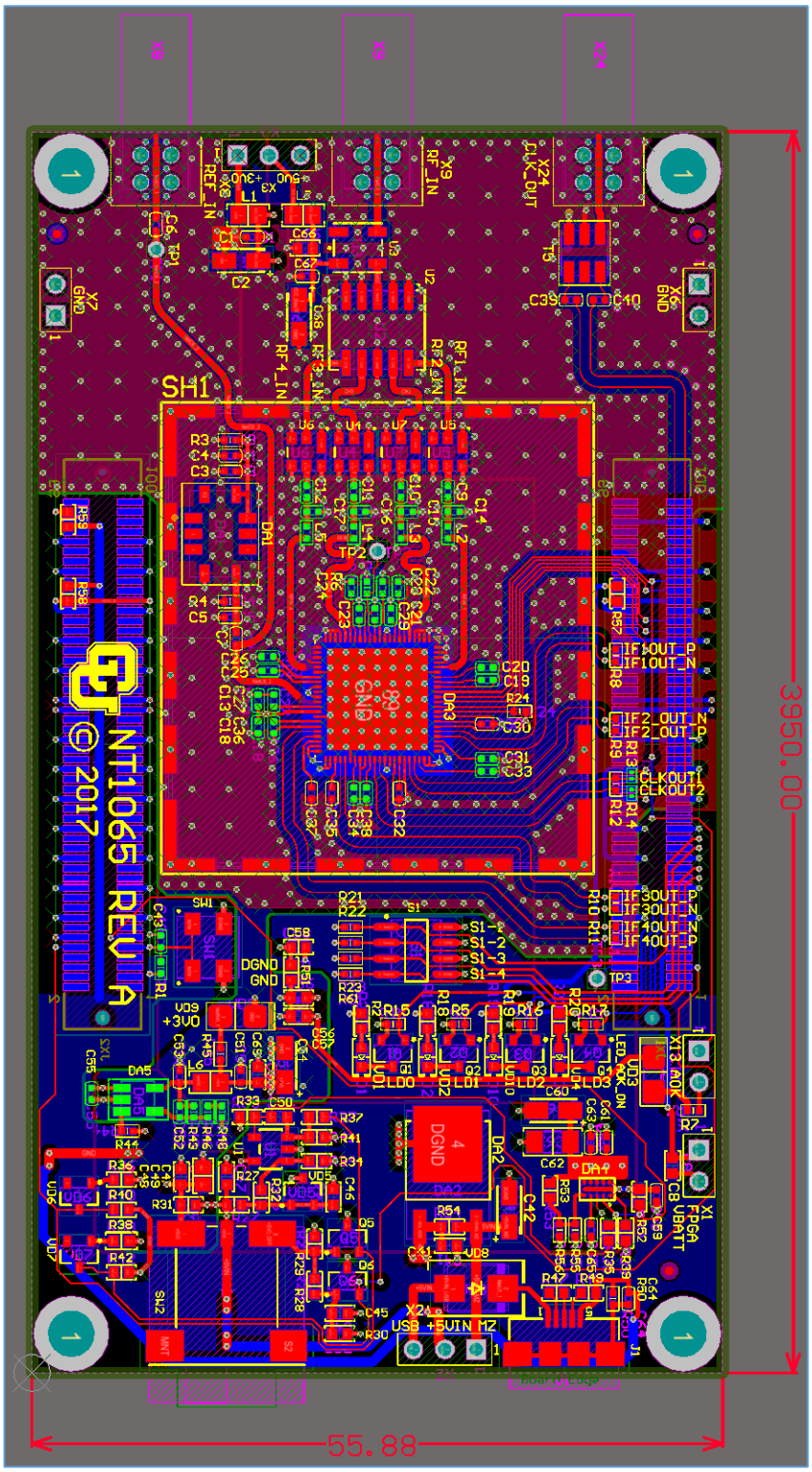

Figure 59: NT1065_MicroZed on Altium Designer

In order to easily locate each component and find those in the BOM, the figure below (see *Figure 60: NT1065_MicroZed's*) represents the NT1065_MicroZed's silkscreen with each of the component designators (solid black for top layer and grey for bottom layer).

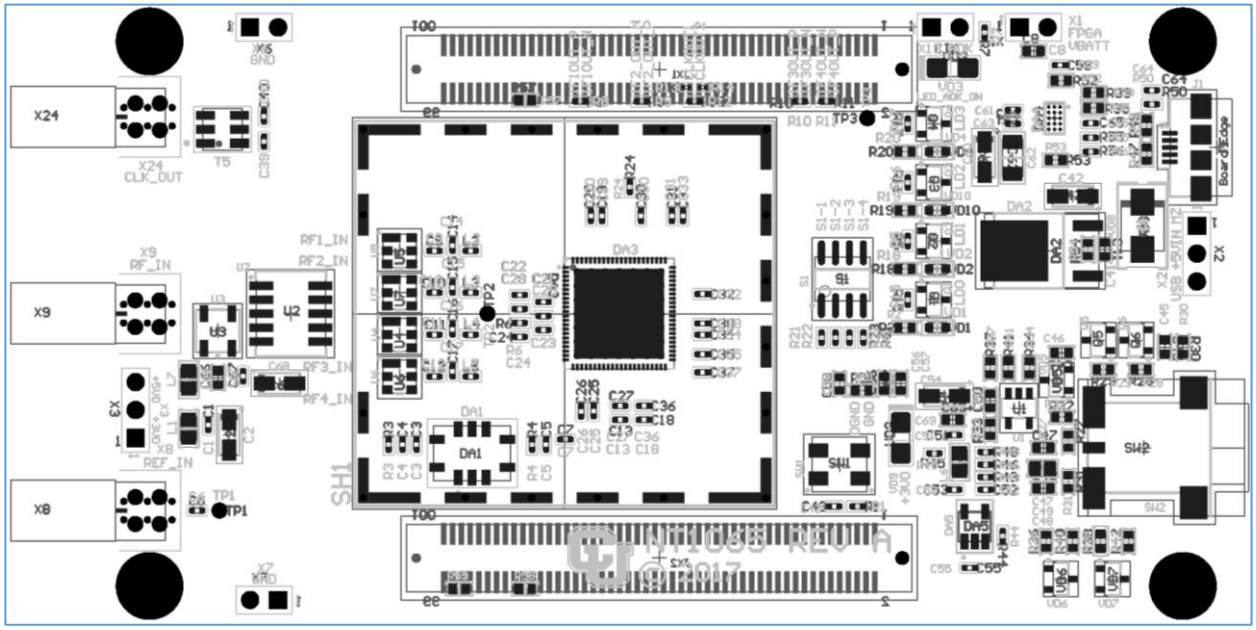

Figure 60: NT1065_MicroZed's assembly drawing

Moreover, the remaining figures (see *Figure 61: NT1065_MicroZed's Layer 1*, *Figure 62: NT1065_MicroZed's Layer 2*, *Figure 63: NT1065_MicroZed's Layer 3*, and *Figure 64: NT1065_MicroZed's Layer 4*) depict the different layers of the board with their routes.

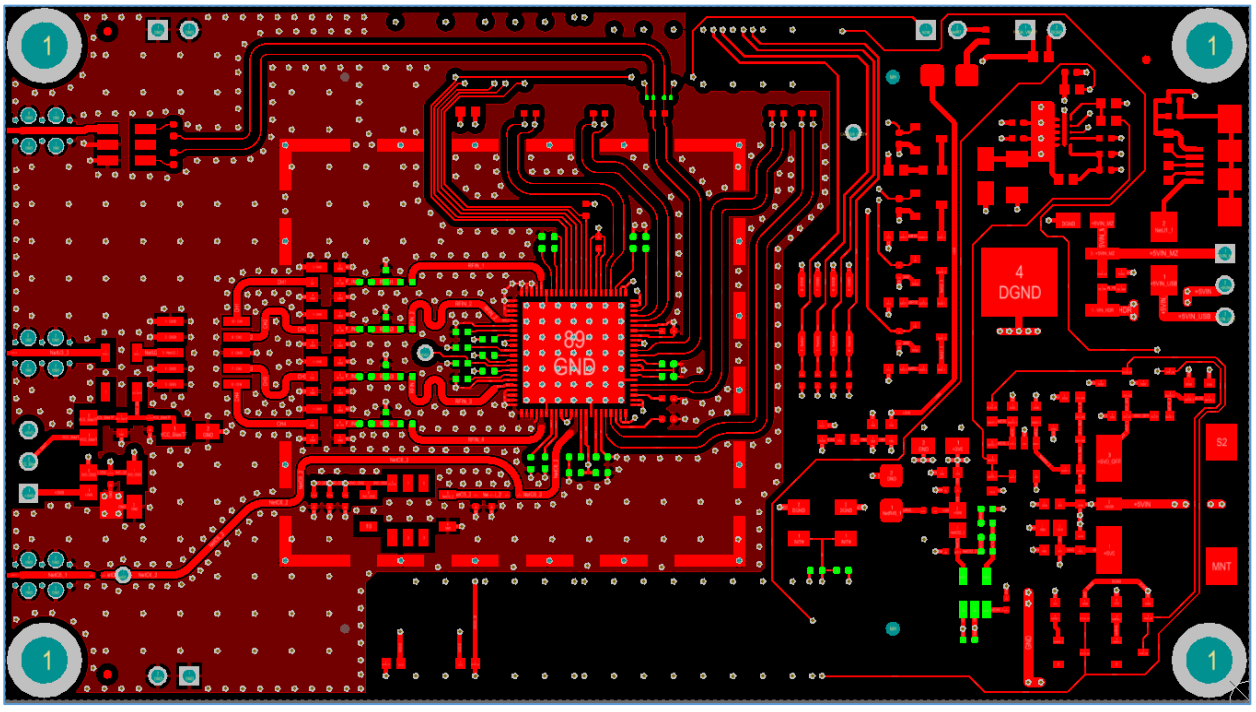

Figure 61: NT1065_MicroZed's Layer 1

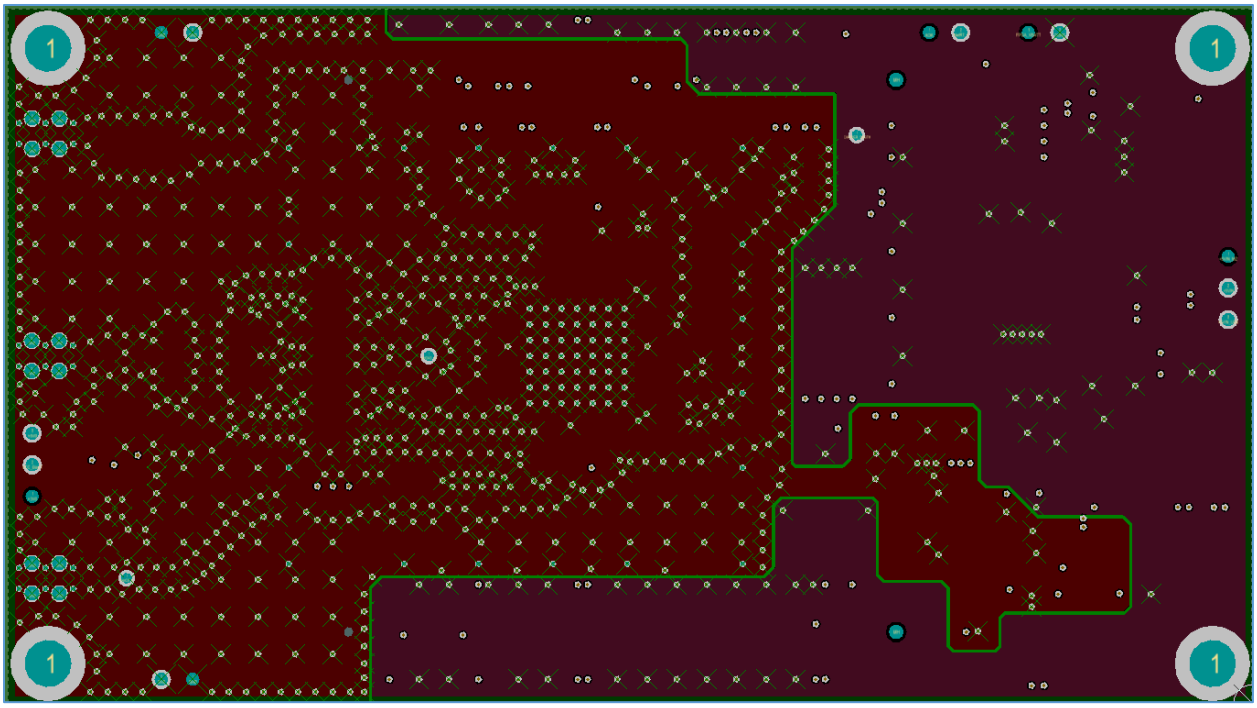

Figure 62: NT1065_MicroZed's Layer 2

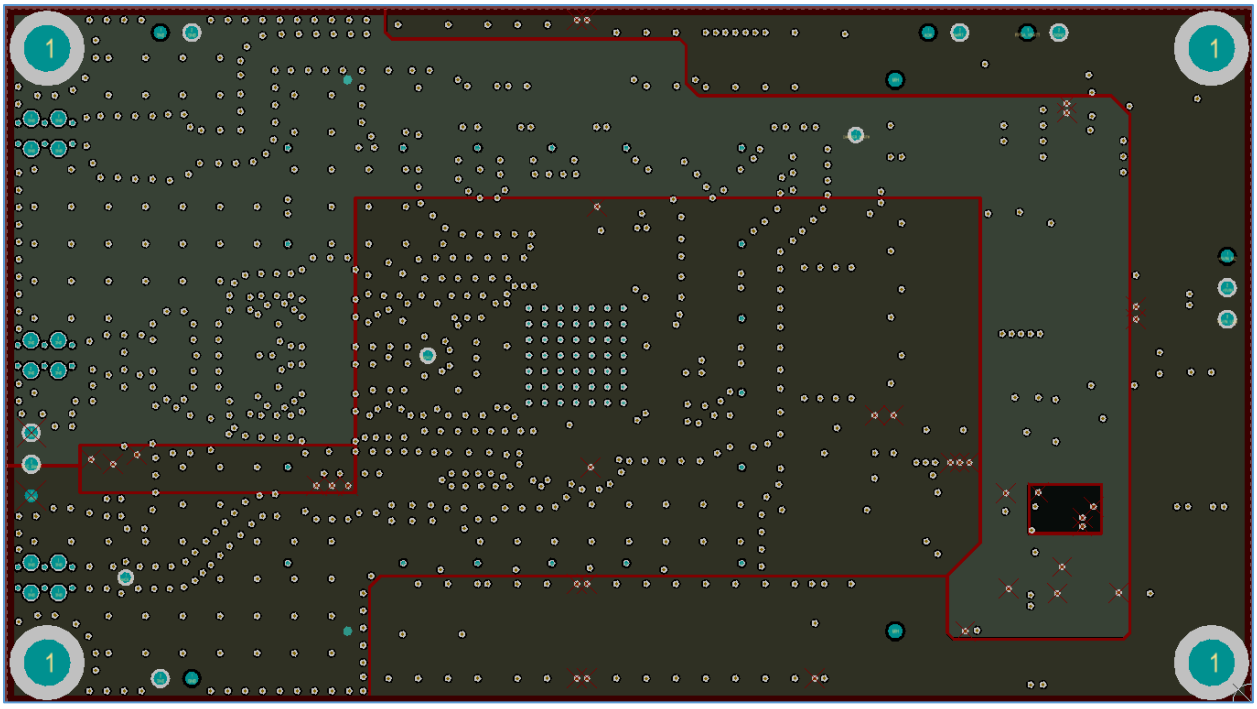

Figure 63: NT1065_MicroZed's Layer 3

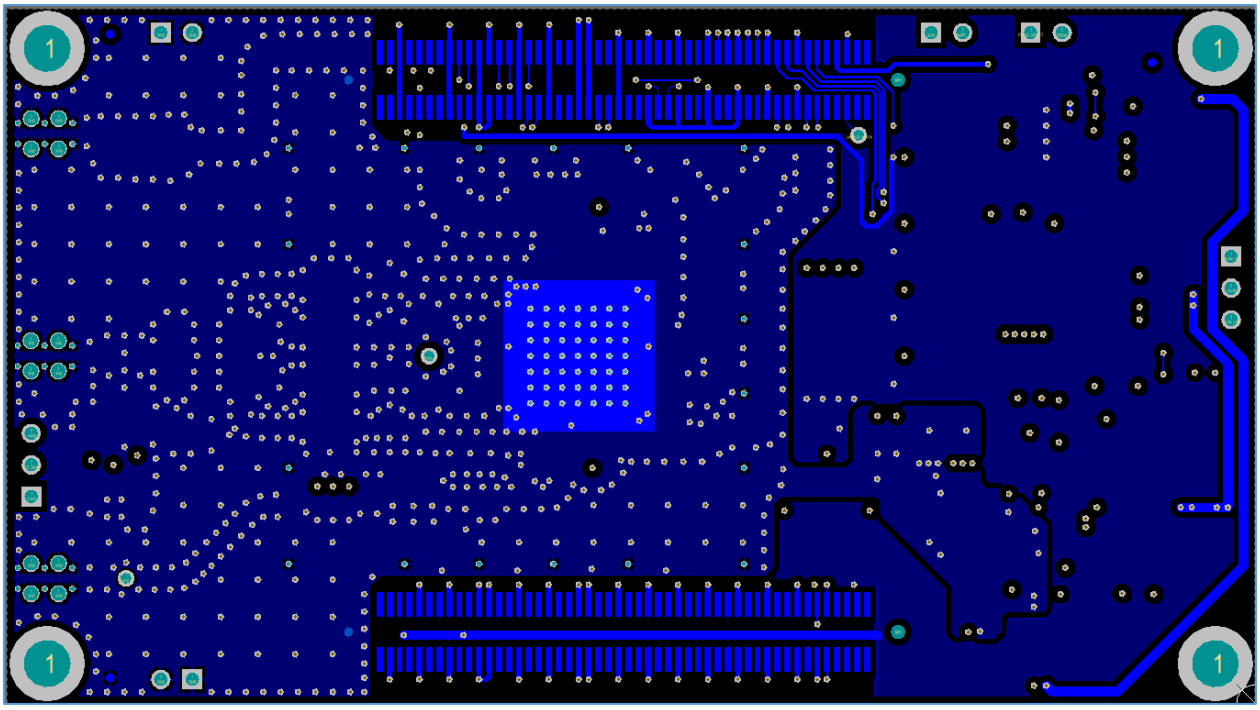

Figure 64: NT1065_MicroZed's Layer 4

Finally, in order to obtain the .pdf versions of the design files as well as all the files required for production, please contact the author of this report or refer to the DVD provided with the physical copy of this report.

8.5 Annexure 5 – NT1065_MicroZed's Original GNSS Signal Test Plan

This annexure contains the original test plan for the GNSS signal data gathered using the new NT1065_MicroZed along with the MicroZed Board. This plan had been developed before realizing that a new revision for the MicroZed had come out fixing many issues with the IO ports (such as the Ethernet, the USB, and the microSD card). Therefore, due to the new MicroZed Board revision not being available and to the GNSS Lab in Boulder, the firmware has been modified in order to partially test the signal reception performance of the newly designed and built boards. However, the previous test plan can still be found below in this annexure for future reference once the new MicroZed Board revision is available.

The test setup should consist of a MicroZed Board attached to the new NT1065_MicroZed and to a computer via USB, a multi-constellation GNSS antenna connected to the NT1065_MicroZed's port X9 allowing the reception of all the different GNSS signals, and, depending on the baseline AGC value upon signal reception, an attenuator between the antenna and the connector X9. This testing phase should been executed like the one for the SiGe modules (see chapter *3.4.2.1 Electronics*) so the results should be compiled in the tables below, followed by a brief discussion,.

Table 17: NT1065_MicroZed Board satellite detection results per band

Band	Expected amount of satellites	Average amount of satellites	Standard deviation of amount of satellites	Minimum amount of satellites	Maximum amount of satellites
GPS - L1					
GPS - L2					
GLONASS - L1					
GLONASS - L2					

The first part of this phase should consist in an analysis of the amount and IDs of the satellites that can be detected versus those that were expected. As can be observed in the table above (see *Table 17: NT1065_MicroZed Board satellite detection results per band*), the amount of satellites that have been flying over the sky when acquiring the data should be compared to the amount of satellites detected using the SDR code on Matlab (averaged for all the boards) after specifying the threshold. Although the table above only includes statistical values, it should be noted that when analyzing each individual board, the minimum amount of detected satellites should always be higher than four for acquiring a proper position.

Table 18: NT1065_MicroZed Board C/N_0 and AGC results

Band	Average C/N_0 [dB-Hz] (across the board)	Standard deviation of C/N_0 [dB-Hz] (Case 1)	Standard deviation of C/N_0 [dB-Hz] (Case 2)	Average AGC [V] (across the board)	Standard deviation of AGC [V] (Case 1)	Standard deviation of AGC [V] (Case 2)
GPS - L1						
GPS - L2						
GLONASS - L1						
GLONASS - L2						

Following, the actual IF data and the AGC values should be analyzed for each module and band, and the overall results should compiled in the table above (see *Table 18: NT1065_MicroZed Board C/N0 and AGC results*). Although there are no reference boards to which these results can be compared, C/N_0 should be expected somewhere around 50[dB-Hz] and AGC values should be expected close to 0[V] assuming no additional attenuator is used as in the SiGe modules. Once tested, the results may be used as a reference for future design and production iterations and testing phases.

In regards to the table, its contents have been described below:

- Average values: values obtained by averaging the value (either C/N_0 or AGC) of all the modules, the latter consisting in the already averaged samples of each module.
- Standard deviation (Case 1): values calculated by averaging the standard deviations (of either C/N_0 or AGC) of all the modules, each having been obtained when averaging the samples per module.
- Standard deviation (Case 2): this standard deviation is independent of any previously calculated one, and it is the result of averaging all the modules together (either their C/N_0 or their AGC).

Having the previous definitions, and considering the individual values it should be easy to see whether or not the values of C/N_0 and AGC provided by each board for a specific band are rather stable (Case 1). Moreover, it should also be observable whether the values obtained from each board and per band are quite similar due to small standard deviations (Case 2).

Finally, the Matlab SDR should also be used in order to determine a final navigation solution, which in case of being close to the real location (by a few meters) should finally demonstrate the well performance of the boards.

8.6 Annexure 6 – Interface Board's Schematics

This annexure comprises two images extracted from the schematic of the Interface Board (see *Figure 65: Interface Board's components (1)* and *Figure 66: Interface Board's components (2)*).

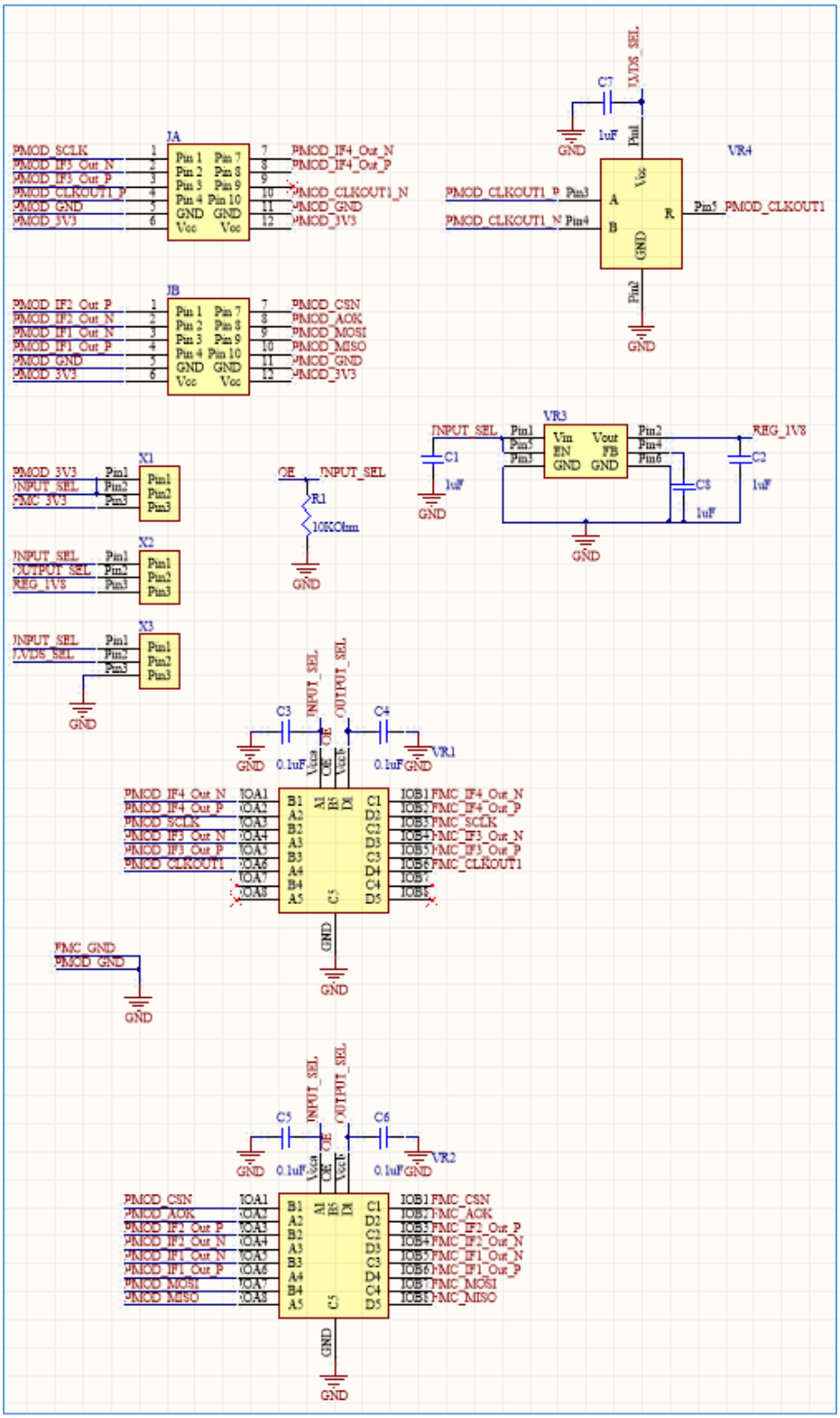

Figure 65: Interface Board's components (1)

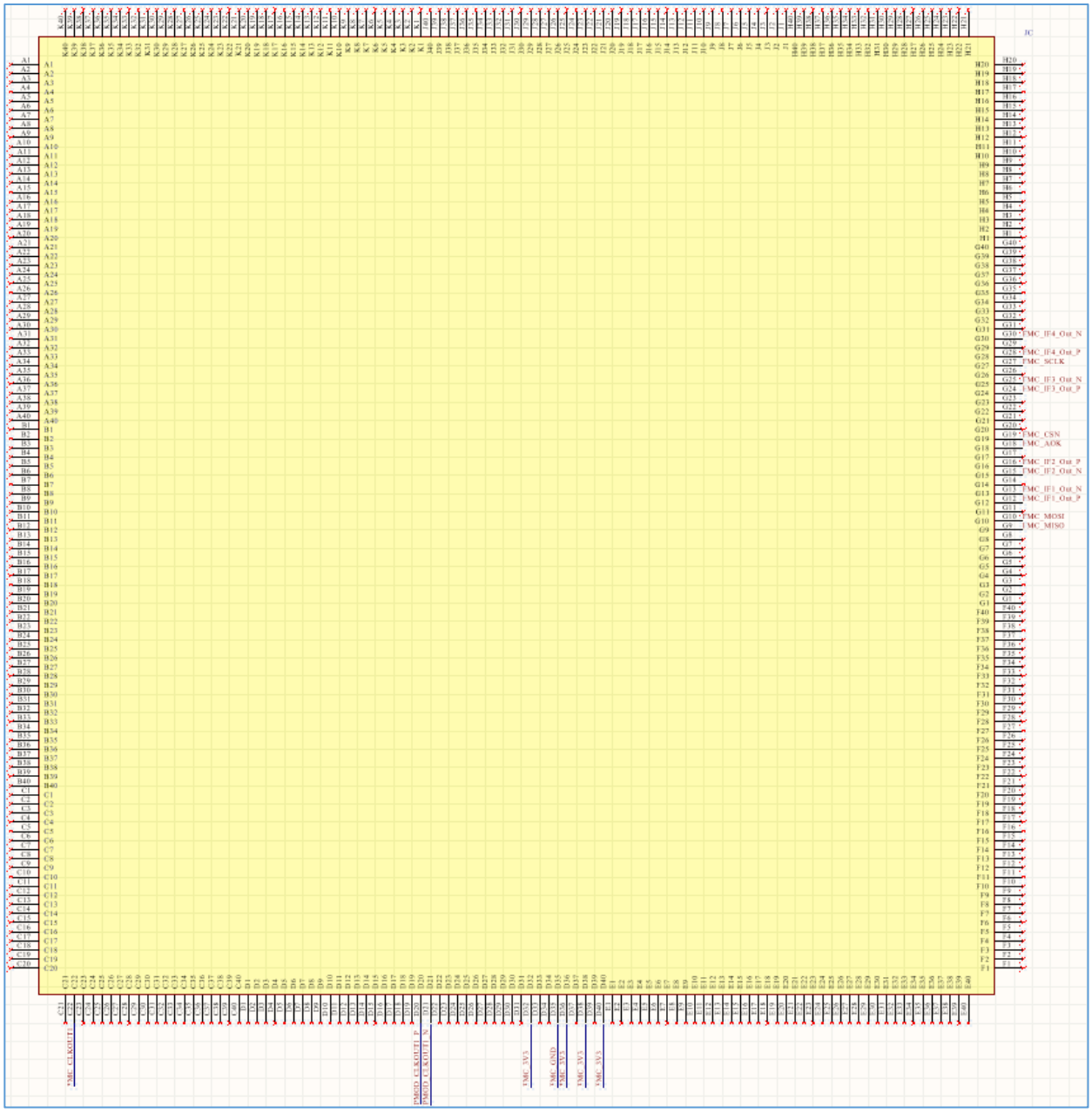

Figure 66: Interface Board's components (2)

Finally, in order to obtain the original schematics, please contact the author of this report or refer to the DVD provided with the physical copy of this report

8.7 Annexure 7 – Interface Board's Layout

This annexure comprises more detailed information about component placement and board layout. In the first picture (see *Figure 67: Interface Board's layout on Altium Designer*), a general view of the board from the top can be observed.

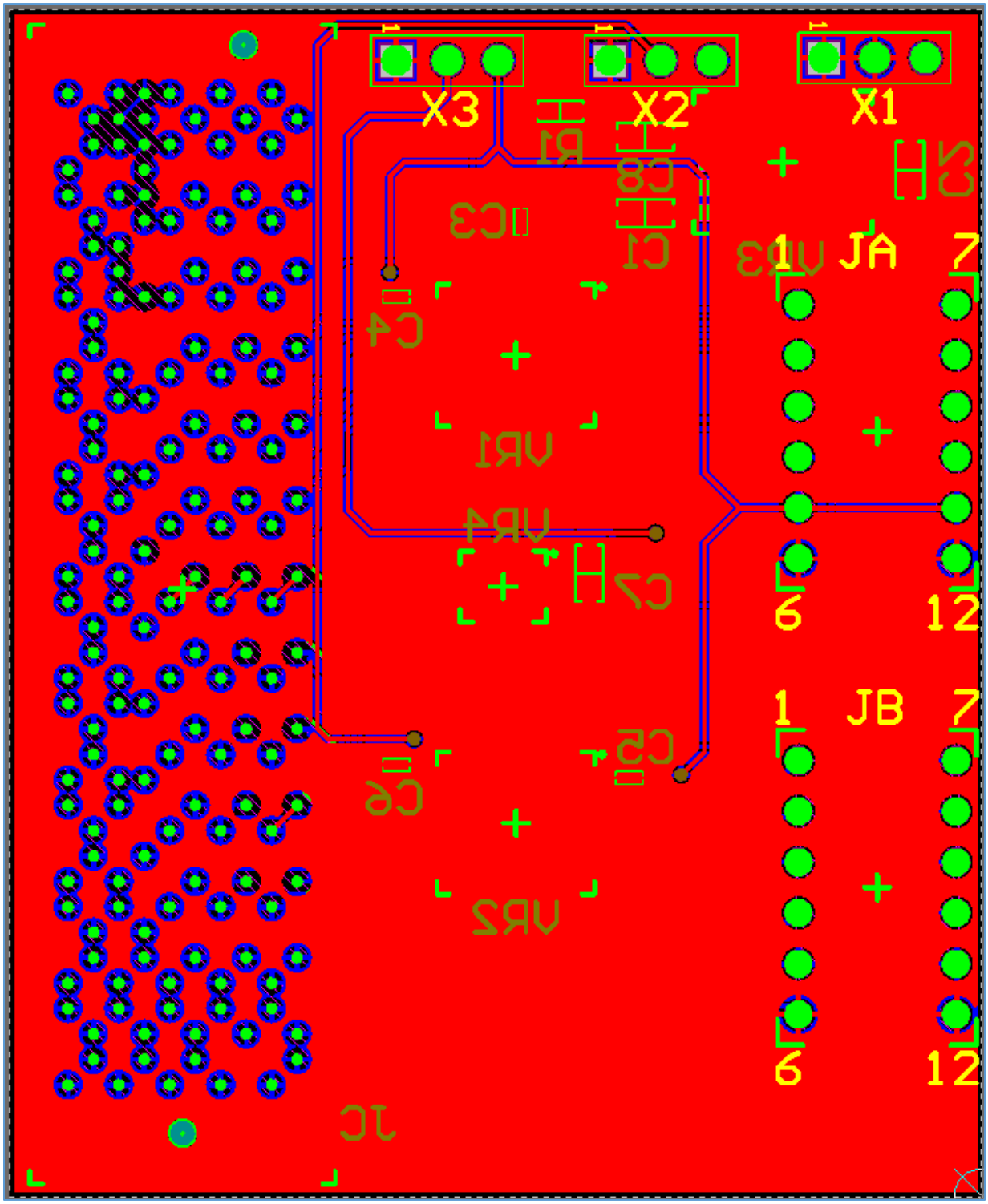

Figure 67: Interface Board's layout on Altium Designer

Secondly, the following image contains information about the component placement on the upper layer (see *Figure 68: Interface Board's assembly drawings (upper layer)*), whereas the next one contains the same information but regarding the lower layer seen from above (see *Figure 69: Interface Board's assembly drawings (lower layer*)).

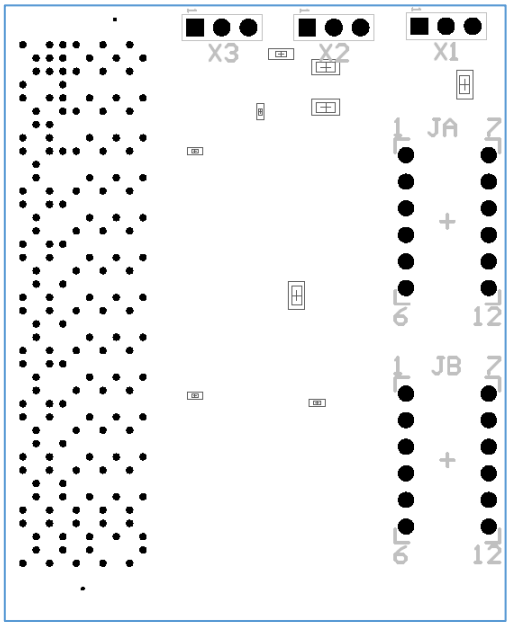

Figure 68: Interface Board's assembly drawings (upper layer)

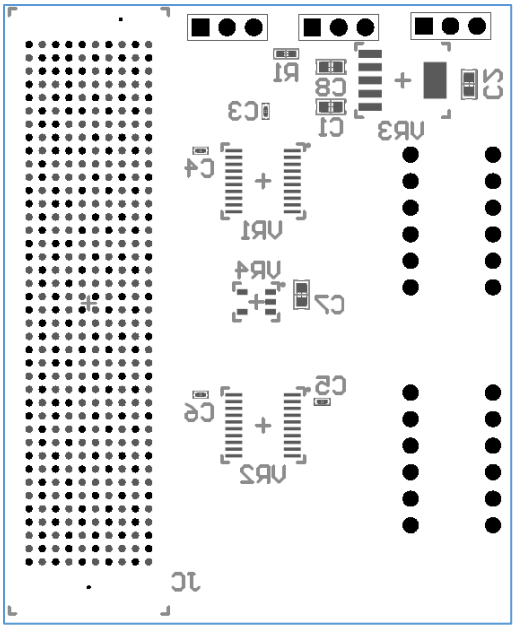

Figure 69: Interface Board's assembly drawings (lower layer)

Furthermore, the following two figures show the two different layers of the board (see *Figure 70: Interface Board's layout (upper layer)* and *Figure 71: Interface Board's layout (lower layer)*).

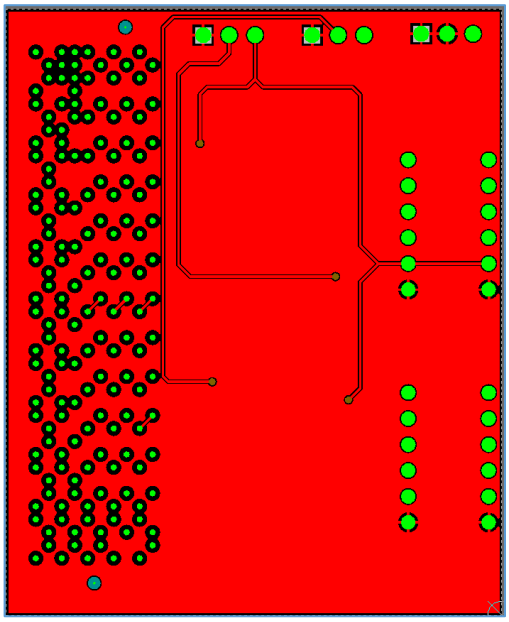

Figure 70: Interface Board's layout (upper layer)

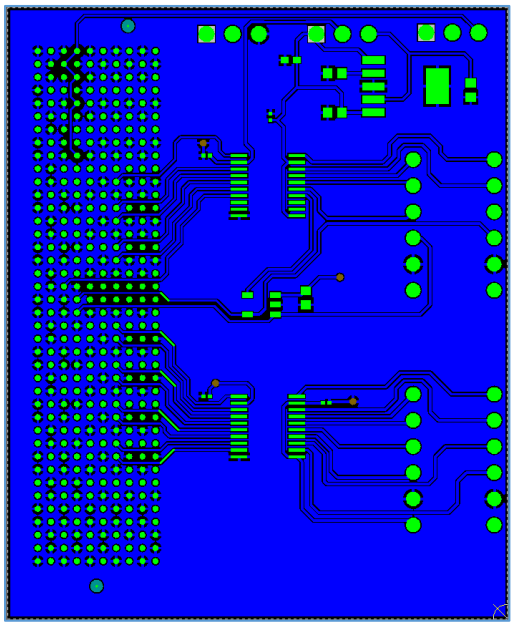

Figure 71: Interface Board's layout (lower layer)

Finally, in order to obtain the design files as well as all the files required for production, please contact the author of this report or refer to the DVD provided with the physical copy of this report.