Analysis and Design of Analog Interface Circuits for Capacitive Detector Readout Systems

by

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Abstract

Advances in sub-micron complimentary metal-oxide semiconductor (CMOS) technologies have enabled implementation of ultra-low-power circuits and systems for variety of applications including readout systems for capacitive radiation detectors. As state-of-the-art readout systems may integrate thousands of electronic channels on chip, designing low-power and low-noise interface circuits is of great interest. The focus of this work is on developing a design methodology for such readout circuits with an emphasis on interfacing with capacitive sensors, in general, and solid-state radiation detectors, in particular. The critical aspects of the design from analyzing the specifications to noise optimization and circuit design are taken into account and the proposed circuits offer improved performance for the readout system.

To facilitate the noise analysis of modern readout systems, the equivalent noise charge equations of the system are derived analytically. The analysis takes into account the stringent requirements of modern readout systems as well as the noise sources associated with deep submicron CMOS technologies. The analysis is based on the EKV (Enz, Krummenacher, and Vittoz) model of MOS transistors which is a model valid for all regions of operation.

As a proof of concept, the analysis and design of three low-power and low-noise interface circuits are presented. The proposed circuits are fabricated in a 0.13 μm CMOS process. The first interface circuit consists of a novel charge-sensitive amplifier (CSA), a pole-zero cancellation (PZC) circuit, and a 2^{nd}-order programmable pulse shaper. The proposed CSA accepts signals of both polarities, exhibits 111 $\bar{e}$-rms noise, and consumes only 37.5 μW. The second interface circuit consists of a CSA, a reset network, a 1^{st}-order shaper, and a PZC circuit. The circuit

consumes about 1 mW and exhibits 66 to 101 $\bar{e}$-rms noise at different peaking times. The third interface circuit is a mixed-signal design and consists of a CSA with leakage compensation, a 5^{th}-order programmable Gaussian shaper, a peak-detect and hold, a discriminator, and a novel Wilkinson-based digitizer. The circuit consumes 1.97 mW and exhibits 58 $\bar{e}$-rms noise. The design performs favourably in terms of power consumption and noise behavior in comparison with similar works in the literature.

Lay Summary

Solid-state radiation detectors measure the dose of radiation and are used in a broad range of applications such as medical imaging, spectroscopy, and astrophysics. The focus of this work is on developing circuit design methodology for readout circuits that measure the amount of deposited charge in such detectors. Based on the presented methodology, an interface circuit for the readout of a specific type of these detectors, namely, Cadmium Zinc Telluride (CZT) detectors, is designed, fabricated and successfully tested. The circuit connects to the individual detector pixels and measures the amount of charge generated by each pixel. Since noise performance of a readout circuit limits the resolution of detection, we have proposed a method to estimate the noise of the circuit analytically. Measurement results of the fabricated integrated readout circuit confirm that the proposed methodology can be used to design a high performance readout system for solid-state radiation detectors.

Preface

I, Mohammad Beikahmadi, am the principle contributor to all the chapters of the thesis. My supervisor, Professor Shahriar Mirabbasi, has provided technical assistance and has also reviewed the thesis. Dr. Krzysztof Iniewski has provided technical assistance and guidance with the design of the chips for CZT radiation detectors. Dr. Roberto Rosales has provided technical assistance with laboratory measurements. He has also provided guidance with printed circuit board (PCB) design, test setup preparation, and performing the measurements.

Some of the chapters in this manuscript have been written based on the following publications. Below is a list of published or submitted conference and journal papers based on this work.

Conference Papers

1. **M. Beikahmadi**, K. Iniewski, and S. Mirabbasi, "A Low-Power Continuous-Reset CMOS Charge-Sensitive Amplifier for the Readout of Solid-State Radiation Detectors," in the proceedings of the IEEE 14^{th} International New Circuits and Systems Conference (NEWCAS), 26-29 June 2016 (Chapters 3 and 4). The authors received ReSMiQ best student paper award, 1^{st} place.

2. **M. Beikahmadi**, and S. Mirabbasi, "A low-power Wilkinson-type ADC for CdZnTe detectors in 0.13-μm CMOS," 21^{st} IEEE International Conference on Electronics, Circuits and Systems (ICECS), pp. 730-733, 7-10 Dec. 2014 (Chapter 6).

3. **M. Beikahmadi**, and S. Mirabbasi, "A low-power low-noise CMOS charge-sensitive amplifier for capacitive detectors," IEEE 9^{th} International New Cir-

cuits and Systems Conference (NEWCAS), pp. 450-453, 26-29 June 2011 (Chapters 3). The authors received the best student paper award, 2^{nd} place.

Journal Papers

1. **M. Beikahmadi**, S. Mirabbasi, and K. Iniewski, "Design and Analysis of a Low-Power Readout Circuit for CdZnTe Detectors in 0.13-μm CMOS", in IEEE Sensors Journal, vol. 16, no. 4, pp. 903-911, Feb. 15, 2016 (Chapter 5).

2. A. Farsaei, Y. Wang, R. Molavi, H. Jayatilleka, **M. Beikahmadi**, A.H. Masnadi Shirazi, M. Caverley, L. Chrostowski, and S. Mirabbasi, "A Review of Wireless-Photonic Systems: Design Methodologies and Topologies, Constraints, Challenges, and Innovations in Electronics and Photonics", Optics Communications journal, 2016 (Other work).

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Glossary

ASIC application-specific integrated circuit

ADC analog to digital converter

CMOS complimentary metal-oxide semiconductor

CSA charge-sensitive amplifier

DAC digital to analog converter

DNL differential non-linearity

ENC equivalent noise charge

INL integral non-linearity

PZC pole-zero cancellation

PCB printed circuit board

PDH peak-detect and hold

SAR successive approximation register

SNR signal-to-noise ratio

SG Semi-Gaussian

SPECT single-photon emission computed tomography

Acknowledgments

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I would also like to acknowledge the National Sciences and Engineering Research Council of Canada (NSERC) and the Institute for Computing, Information and Cognitive Systems (ICICS) at the University of British Columbia. I also appreciate Canadian Microelectronics Corporation for fabrication services and CAD tools support.

I also take this opportunity to express gratitude to all of my colleagues at the System-on-a-Chip research laboratory at the Electrical and Computer Engineering Department for their extensive help and support. Special thanks goes out to Dr. Roberto Rosales for his support, guidance and technical assistance on laboratory measurements. I must also thank Roozbeh Mehrabadi for CAD tools support.

Finally, I would like to take this opportunity to thank my family for their love, support, and attention throughout my life. In particular, I am thankful to my wife and best friend, Kimia, who supported me and encouraged me through this venture.

Chapter 1

Literature Overview

1.1 Introduction to Capacitive Detector Readout Systems

Room-temperature solid-state radiation detectors have broad applications in medical, space, and security systems [16, 17]. These detectors benefit from a better energy resolution and a smaller form factor in comparison with conventional scintillators. Cadmium Zinc Telluride (CdZnTe or CZT) is an example of these detectors which has gained a lot of attention in recent years. High density (≈ 5.9 g/cm^3), high atomic number (Cd: 48, Zn 30, and Te: 52), and tunable wide bandgap ($\approx 1.5-2.2$ eV) make CZT detectors favourable choices for many applications that require room temperature operation [18]. Furthermore, fabrication of CZT detectors with large number of imaging pixels has become economically and technologically viable thanks to recent advancements in their fabrication process. This requires integration of a large number of readout circuits on chip to process the output signal of each pixel. In order to make such an integration feasible, the power consumption, size, and noise of each readout circuit must be kept at acceptable levels. As CZT appears to be widely available for future detector readout systems, the proof of concept integrated circuit that we will design in this research will be optimized for this detector.

Conventional readout circuits had only a small number of electronic channels and were implemented using discrete components while today's imaging systems may have thousands of electronic channels per cm^2 [19, 20]. Implementing a large

number of highly densed electronic channels using discrete components is not a feasible solution due to the high cost and large area. Thus front-end electronics needs to be integrated in a custom-made application-specific integrated circuit (ASIC). Current integrated readout circuits are implemented mainly in complimentary metal-oxide semiconductor (CMOS) technologies. Submicron CMOS technologies offer high integration density, low power consumption as well as the ability to integrate various analog and digital functions on the same chip [21] and therefore minimizing the overall system cost, size, and weight.

1.1.1 The Detector

Radiation detectors generate electron-hole pairs by absorbing the received electromagnetic wave. When enough energy is absorbed by the detector, electron-hole pairs are generated. The pairs drift to corresponding electrodes in the presence of an electric field generated by an applied external voltage. The generated electrons and holes migrate in opposite directions. The motion of electric charges under the influence of the electric field generates a signal that can be modelled by a time-variant current source.

A detector pixel is often modelled by the capacitances to the adjacent neighbours (C_{adj}) and to the backside (C_0). The capacitances are shown in Figure 1.1a. The pixels are held at a constant potential with the help of the amplifiers. The combination of these capacitances form an effective capacitance of C_{det}. This capacitance is shown on the electrical model of the detectors illustrated in Figure 1.1b. To model the detector leakage current, a constant current source is added to the model. The I_{sig} in Figure 1.1b is the signal that is generated by the motion of the pairs under the influence of the electric field. Various factors are involved in determining the shape of the signal such as the applied bias voltage, the position and depth of interaction, and the properties of the detector material [22].

The CZT detectors that we will design the proof-of-concept readout system for, are manufactured by Redlen Technologies, Inc. The detectors typically have 500 fF pixel capacitance and produce a leakage current in the range of 1 fA to 50 nA. When used in single-photon emission computed tomography (SPECT), each pixel generates about 5 fC charge at each event. The events occur typically 1 ms

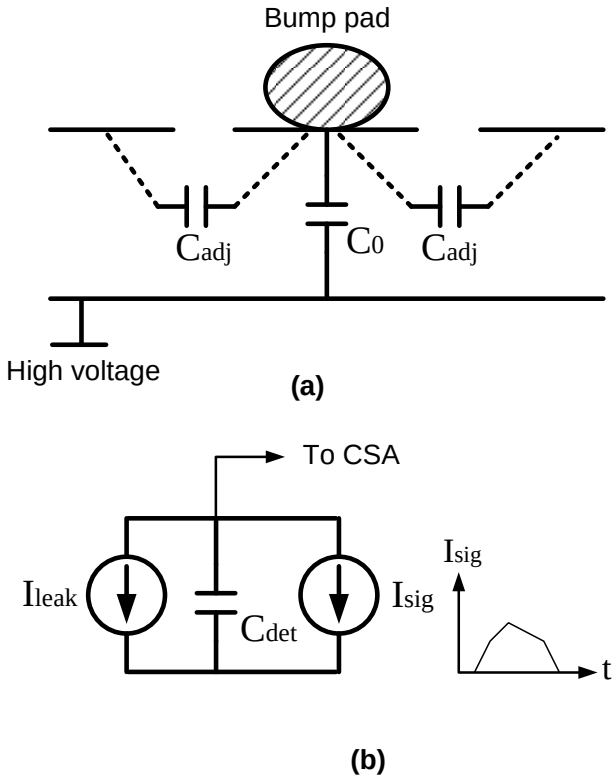


Figure 1.1: (a) Capacitances in a capacitive detector, and (b) electrical model of the detector.

apart.

1.1.2 The Readout System

Figure 1.2 shows a simplified block diagram of a typical readout system. The readout system for capacitive detectors consists of amplification, pulse shaping, and signal processing stages. The stages are briefly reviewed in the following subsections.

Amplification

The sensor generates a small amount of charge which appears as a weak signal at the electrodes. This weak signal is often needed to be amplified by a charge-

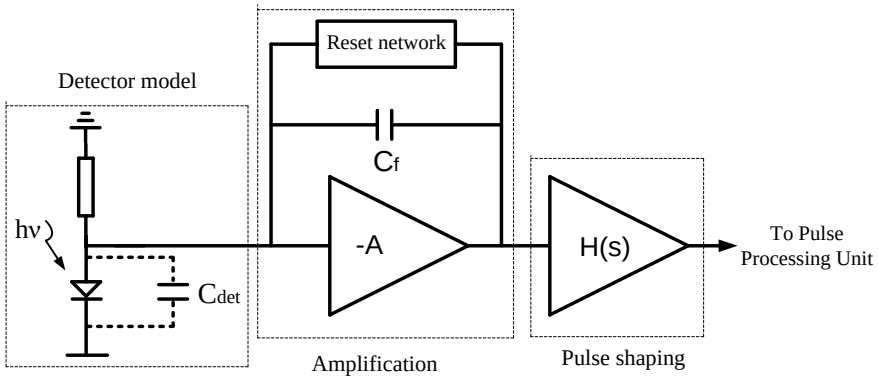


Figure 1.2: Simplified block diagram of a typical readout channel for solid-state radiation detectors.

sensitive amplifier (CSA) before further processing. The core of the CSA consists of an inverting high-gain voltage amplifier and a feedback capacitor. The generated charge by the sensor is integrated on the feedback capacitor. This generates a step-like signal at the output terminal of the CSA. The amplitude of the output signal is approximately equal to Q/C_f where Q is the amount of injected charge and C_f is the feedback capacitance. The charge gain, defined as $A_Q = V_o/Q = 1/C_f$, is thus determined by C_f. Note that C_f is a well-controlled component and therefore, the charge gain of the amplifier becomes (to the first order of approximation) robust to the detector capacitance variations. A reset mechanism, either continuous or discrete, needs to be implemented in order to avoid pulse pile up at the output of the CSA.

Pulse Shaping

The resulting output signal from the CSA is then filtered by a pulse shaper. A pulse shaper is an active or passive filter whose main function is to enhance the signal-to-noise ratio by reducing the bandwidth of the noise. This is achieved by choosing a proper peaking time for the filter which also sets the duration of the pulse. The resulting voltage pulse at the output terminal of the shaper has an amplitude proportional to the amount of the injected charge. This signal can be stored or digitized for further processing.

Digitization and Signal Processing

The signal from the pulse shaper is often digitized before storage or further processing. In order to identify the channels with incidents discriminators are employed. They provide a trigger signal whenever the signal from the pulse shaper rises above a threshold level. The signal from the pulse shaper is passed to a peak-detect and hold (PDH) circuit before digitization. A PDH tracks the signal from the pulse shaper, stores and keeps the peak voltage. This peak voltage is then passed to an analog to digital converter (ADC) for digitization. After the signal is digitized, it can be stored on the chip or transferred to a computer for storage or processing.

1.2 Motivation

The design of readout systems for capacitive solid-state radiation detectors has been discussed extensively in the literature [12, 17, 18, 20–52], however, continuous improvement in readout circuit design is necessary in order to meet the stringent requirements of modern detector systems. The readout system can be realized using either discrete components or integrated circuits. In [53], an experimental comparison between CMOS and discrete charge-sensitive amplifiers for CZT detectors is given. The measured results show that it is possible to reach a high performance using both approaches, however, the integrated circuit approach offers a smaller size and a lower power consumption. As state-of-the-art readout systems may have hundreds or thousands of electronics channels, it would make sense to realize such systems using the integrated circuit approach to save power and lower the cost of the system. Thus for the rest of this work we will mainly focus on readout systems that are realized using the integrated circuit approach. In the following, we review the most recent and popular designs in detail.

RENA-2/3 [41, 42] ASICs are designed in 0.5 μm CMOS technology for readout of CZT detectors. The newest generation of the design contains a charge-sensitive amplifier, leakage compensation, pulse shaper, comparator, Digital to Analog Converter, and Peak-Detect-Hold. It has selectable dual energy range and the peaking time is adjustable from 0.36 to 38 μs. The detector capacitance can vary from 2 to 9 pF. All these features make the chip suitable for a variety of applications. The power consumption of the chip is about 5.8 mW and the equivalent

noise charge (ENC) of the system is 140-150 $\bar{e}$-rms with no detector attached. The design is not suitable for the systems that require lower power consumption and higher resolution.

0.35 μm CMOS process has been a popular choice for the development of integrated circuits for capacitive radiation detectors. A low-noise 64-channel ASIC is proposed in [37] in a 0.35 μm CMOS process for readout of CZT detectors. Each readout channel includes a charge-sensitive amplifier with leakage current compensation, a CR-RC shaper, two filters, an inverse proportional amplifier, a peak-detect-and-hold circuit, a discriminator, a control circuit and a buffer. The input range is from 5 to 190 keV. The measured ENC is 66 $\bar{e}$-rms at a peaking time of 1.5 μs with no detector attached. However, the power consumption of each channel is 8 mW. In [35], a multi-channel readout circuit is proposed for CZT-based spectrum analyzer in a 0.35 μm CMOS process. The front-end circuit includes a charge-sensitive amplifier, a CR-RC shaping amplifier and an analog output buffer. The power consumption of the front-end circuit is 2.8 mW and the measured ENC is 133 $\bar{e}$-rms with no detector attached. However, there is no leakage compensation block on the chip and the detector is assumed to be AC-coupled to the front-end circuit. In [21], another design is proposed for radiation sensor interfaces in 0.35 μm CMOS technology. The design contains a charge-sensitive amplifier and a novel $CR-RC^2$ pulse shaper and a buffer. The power consumption of the front-end circuit is 1 mW per channel but the equivalent noise charge is 382 $\bar{e}$-rms with no detector attached. The peaking time of the pulse shaper is adjustable, however, the peak amplitude of the output signal changes when the peaking time is adjusted. The chip proposed in [43] is called DEDIX and is intended for digital X-ray imaging systems. Each readout channel is built of a charge-sensitive amplifier, a pole-zero cancellation circuit, a shaper, two discriminators and two counters. The detector capacitance can vary from 1 to 3 pF. The measured equivalent noise charge is 110 $\bar{e}$-rms for a detector capacitance of 1 pF at the shaper peaking time of 160 ns. The power consumption per channel is 5 mW. A low-noise ASIC, called KW03, is proposed in [44] which is intended for Silicon and CdTe Sensors in 0.35 μm CMOS technology. Each readout channel includes a charge-sensitive amplifier, bandpass filters and a sample-and-hold circuit. The equivalent noise level of a typical channel is about 89 $\bar{e}$-rms with no detector attached. However, the ENC

increases to 260 $\bar{e}$-rms when the ASIC is housed in a standard QFP package. The power consumption of each readout channel is about 3 mW.

A design in 0.25 μm CMOS process is proposed in [54] for CZT Co-planar grid sensors. The ASIC implements three front-end channels. Two channels are designed for amplification and processing of the collecting and non-collecting electrodes. The third channel provides amplification and processing of the cathode signal. The circuit dissipates 25 mW and achieves an ENC of 500 $\bar{e}$-rms.

A self-triggered pulse amplification and digitization ASIC, called SPADIC, is proposed in [55] in 0.18 μm CMOS technology. Each readout channel includes a charge-sensitive amplifier, a pole-zero cancellation circuit, a second-order pulse shaper, a comparator, a DAC, and a pipeline analog-to-digital converter. The power consumption per channel is 4.5 mW and the equivalent noise charge is above 200 $\bar{e}$-rms with no detector attached.

A family of prototype pixel readout chips operating in single photon counting mode, called Medipix1,2,3, is introduced in [20, 23, 56]. They were implemented in 1, 0.25 and 0.13 μm CMOS technologies, respectively. The latest chip contains a CSA, a first-order shaper with 300 ns shaping time, discriminators, and digital circuits. The chip has two gain settings and each analog channel consumes only 16.2 μW. The ENC of the readout circuit at high gain setting is about 72 $\bar{e}$-rms, however, when the input range is extended by applying a lower gain setting, the ENC increases to 105 $\bar{e}$-rms.

Ultra-deep submicron CMOS processes seems to be appealing to applications that require fast signal processing. A fast prototype chip in 90 nm technology, called PX90, is introduced in [45] for readout of hybrid pixel detectors. Each pixel contains a charge-sensitive amplifier with leakage compensation, a main amplifier, two discriminators, two DACs and two ripple counters. The power consumption of each pixel (excluding the power consumption of other circuits on the chip) is about 47 μW. This chip achieves an ENC of 204 $\bar{e}$-rms with no detector attached. The measured noise spread from pixel to pixel is σ = 22 $\bar{e}$-rms . The ENC rises to 240 $\bar{e}$-rms for a detector capacitance of 50 fF. The offset spread from pixel to pixel is σ = 35 mV. In order to minimize the effect of threshold spread across the chip, the DACs are controlled by an external software. After correction, the effective threshold spread at the discriminator inputs reduces to σ = 1.8 mV which

equals to an input offset of 64 $\bar{e}$-rms. The input dynamic range is limited and the gain and noise performance of the readout circuit vary significantly with the bias condition of the leakage compensation block. More recently, a chip called CHIPIX65 [40, 46] has been under development in a 65 nm process for use in the Large Hadron Collider (LHC) experiments in CERN with collaboration of 35 experts in the field. The experiments demand very high data rates, high integration density, low power, and low noise performance. The analog front-end contains a charge-sensitive amplifier with leakage compensation, a comparator and a time-over-threshold counter. This design achieves a low power consumption of 5 μW and an equivalent noise charge of 110-120 $\bar{e}$-rms per pixel. However, the dynamic range is limited, and a slight change in the detector capacitance affects the rise time and the peak amplitude of the signal noticeably. Table 1.1 summarizes the advantages and drawbacks of the aforementioned readout systems.

As mentioned earlier, state-of-the-art readout systems may integrate thousands of electronic channels on chip. For an example, a pixel detector called ATLAS uses 28000 readout chips and each chip integrates 2880 readout channels [57, 58]. This high level of integration requires low power consumption. The detector pixel size has also shrunk in recent years. The Medipix2 [20] chip, for an example, contains 65536 readout channels for the readout of pixels with dimensions of 50 μm by 50 μm. The pixel size dictates the area available for the integration of each readout channel. Considering such high level of integration and the small area available for heat dissipation, any small improvement in power consumption of each readout circuit can significantly improve the performance of the readout system. As the readout channels are placed as close as possible to the detector pixels, the generated heat by the readout circuits can increase the operating temperature of the integrated circuits and the detector. The increase in temperature deteriorates the performance of the system by

- increasing the noise of the devices in the readout circuits. Thermal noise in both resistors and MOS devices increases with temperature. The thermal noise of the input device of the CSA is the main contributor to the overall noise of the system.

- increasing the leakage current of the detector [59, 60]. The increase in the

Table 1.1: Performance comparison of recent readout systems

Design	Process	Signal processing chain	Advantage(s)	Drawback(s)
RENA-2/3 [41, 42]	0.5 μm CMOS	CSA, leakage compensation, pulse shaper, comparator, DAC, PDH	Selectable dual energy range Widely adjustable peaking time	High power consumption Poor noise performance
[37]	0.35 μm CMOS	CSA, leakage compensation, pulse shaper, filters, amplifier, PDH, discriminator	Good noise performance	High power consumption
[35]	0.35 μm CMOS	CSA, pulse shaper, buffer	Moderate power consumption Moderate noise performance	No leakage compensation
[21]	0.35 μm CMOS	CSA, pulse shaper, buffer	Low power consumption	Poor noise performance
DEDIX [43]	0.35 μm CMOS	CSA, PZC, pulse shaper, two discriminators, two counters	Fast shaping time Moderate noise performance	Very high power consumption
KW03 [44]	0.35 μm CMOS	CSA, filters, sample and hold	Moderate power consumption	Poor noise performance when packaged
[54]	0.25 μm CMOS	CSA, difference amplifier, pulse shaper, baseline holder, bandgap reference, comparator	Processing of both cathode and anode signals	High power consumption Poor noise performance
SPADIC [55]	0.18 μm CMOS	CSA, PZC, pulse shaper, comparator, DAC, pipelined ADC	High speed signal processing chain	High power consumption Poor noise performance
Medipix3 [23]	0.13 μm CMOS	CSA, pulse shaper, discriminators, digital circuits	Low power consumption Good noise performance	Deterioration of noise performance at higher input ranges
PX90 [45]	90 nm CMOS	CSA, leakage compensation, amplifier, two discriminators, two DACs, two ripple counters	Low power consumption Offset correction by DACs	Poor noise performance Limited input dynamic range Offset correction required
CHIPIX65 [40, 46]	65 nm CMOS	CSA, leakage compensation, comparator, time-over-threshold counter	Very low power consumption Fast signal processing	Moderate noise performance Limited dynamic range

leakage current can change the DC bias levels and ultimately saturate the front-end electronics. The shot noise due to the leakage current of the detector can also contribute significantly in the noise of the readout circuits specially at long shaping times [61, 62].

- changing the electrical properties of the detector. For example, electron and hole drift mobilities and electric field uniformity across the detector vary with temperature [63–65]. In general, radiation detectors perform better at lower temperatures. It has been shown in [66] that 1 °C increase in the detector temperature decreases the detected energy by 0.1 keV for events depositing 30 keV. This loss of resolution is problematic for applications that require high spatial resolution.

Designing a low-noise and low-power integrated readout system requires making trade-offs between several key design parameters, including noise performance, gain, linearity, dynamic range, and power consumption. The trade-offs are described in detail below.

- In a readout system it is often desired to improve the resolution of detection which means the noise of the system needs to be reduced. The noise of the readout circuit is mainly dominated by the noise of the CSA and the noise of the CSA can be enhanced at the expense of increasing its power consumption. This is in contrast with the low-power requirement of modern readout circuits. Besides, increasing the power consumption of the circuit generates extra heat which in turn can deteriorate the performance of the detector and the readout circuit and ultimately limit the resolution of detection.

- Linearity is a design parameter that is desired to be increased. Increasing the linearity of design is usually achieved by increasing the power consumption of the readout system which is undesired.

- As the signal produced by the detector is weak, the readout circuit must provide sufficient gain to amplify the signal for further processing. The gain of the readout circuit is often enhanced by increasing the power consumption of the circuit which is undesired. Increasing the gain can limit the dynamic

range of the readout circuit. This is due to the scaling of CMOS technology where there is less and less headroom voltage is available for analog circuits in ultra deep submicron technologies.

As explained earlier, submicron CMOS technology is of great interest for designing front-end electronics for detector applications. Advanced CMOS technologies offer lower supply for both analog and digital circuits which reduces the power dissipation of the readout circuit. Low power dissipation enables high level of integration which is essential in design of multi-channel detector readout systems. Digital circuits also benefit from higher speed with the advancement of CMOS technology. The noise performance of the readout system is also enhanced with the scale of CMOS technology from micron to submicron [67]. In older CMOS technologies the bias conditions and dimensions of the input device of the charge-sensitive amplifier was dictated by the bandwidth requirements of the amplifier. With the advancement of CMOS technology, cut-off frequency of MOS devices has increased significantly. This means that speed is not an issue any more and the input device can be biased in weak inversion region where the transconductance of the input device depends only on the bias current and not on the device dimensions. As a result, the bias conditions and dimensions of the input device can be optimized for noise performance. On the other hand, designing readout systems in deep submicron technologies is becoming more challenging [68]. Reduced supply voltage restricts the output swing (i.e., lower dynamic range) and constrains the circuit topology. Designing precise analog circuits with reduced supply voltage is becoming difficult and requires a good understanding of physical effects and characteristics of devices in deep submicron CMOS processes. Matching of transistors and passive components in analog circuits realized in advanced processes is also difficult. For example, for minimum size MOSFETs in 0.13 μm technologies the standard deviation of threshold voltage mismatch is about 35 mV which increases to about 50 mV for the MOSFETs in 90 nm technologies [67]. Operation of digital circuits using minimum length devices is also affected by mismatch and large timing fluctuations can occur. In addition to increased mismatch between devices and components in each readout channel, the channel to channel mismatch also increases. For example, the measured offset spread from pixel to pixel in a readout

chip in 90 nm technology is σ = 35 mV [45].

When it comes to noise analysis, understanding noise mechanisms that cause performance degradation is essential to design low-noise front-end circuits. With the advancement of CMOS technology into nanometer regime, additional noise sources need to be taken into account in order to accurately model the noise behavior of a readout system. Therefore, it is essential for a designer to clearly understand the trade-offs involved in designing readout systems using deep submicron technologies. Detailed noise analysis of readout systems for solid-state radiation detectors can be found in literature [10, 12, 69–78]. The analysis provided in the literature needs to be reconsidered in order to accurately model the noise behavior of the current state-of-the-art front-end circuits. The reasons include

- The input MOS device of the CSA is often assumed to operate in strong inversion region which is in contrast with low-power operation of the modern readout systems. In state-of-the-art low-power circuit designs the input transistor is biased in weak (or moderate) inversion regions [74]. This change in the region of operation needs to be taken into account when the noise of the system is being modelled and evaluated.

- MOS devices in ultra-deep submicron technologies exhibit additional noise sources that cannot be safely ignored. An example of such noises is the parallel noise contributions from the gate current of the input device of the CSA. The gate leakage current increases significantly with reduction of the gate-oxide thickness in advanced CMOS technologies [79]. This current must be modelled and taken into account when noise behavior of the system is being evaluated and optimized.

- It is often assumed in the literature that the power spectral density of the series flicker noise has a pure $1/f$ distribution. Experimental results in deep submicron technologies show that slope of the $1/f$ noise component of the spectrum α_f is smaller than 1 for N-type and larger than 1 for P-type MOS devices [80, 81]. The $1/f$ noise coefficient (K_f) can also be bias dependent.

Based on the aforementioned reasons, it is necessary to reconsider evaluation of the noise of the modern detector readout system taking into account the new

noise sources, biasing conditions of the devices, and noise models of devices in ultra-deep submicron technologies. In this work we will use the EKV (Enz, Krummenacher, and Vittoz) model [82] of the MOS device to efficiently analyze the noise performance of modern readout systems. EKV is a fully analytical MOS device model which is intended for design, analysis and simulation of low-power and low-voltage analog circuits in advanced CMOS technologies. It offers a better modeling of the weak and moderate inversion regions. It is also a compact model and has a small number of DC parameters compared to other MOS models. BSIM3 (Berkeley Short-channel IGFET) model, for example, is overly empirical and has over 400 DC parameters, but EKV has only 22. The use of this model in simulators can lead to shorter simulation time. EKV version 2.6 is currently supported by many simulators, including Spectre, SpectreRF, Star-Hspice, PSPICE, and others. EKV model is also available in commercial design libraries from foundries such as Toshiba, Atmel, and EM Marin. Examples of commercial integrated circuits designed using the EKV model can be found in [83]. One of the limitations of this model is the assumption of constant doping in the channel which causes inaccurate modeling of capacitances in high voltage MOS devices [84]. Another limitation in EKV version 2.6 is the difficulty of the model to accurately fit I_D-V_G curves for low and high values of V_D simultaneously [85]. This is due to drain-induced barrier lowering (DIBL) effect in short-channel MOS devices and is claimed to be fixed in EKV version 3.0.

The EKV model is based on fundamental physical properties of the MOS structure and takes advantage of the inherent symmetry of the device by referring all the voltages to the local substrate. In this model all the small- and large-signal variables are continuous in all regions of operation. The drain current in this model is defined as a difference between a forward (I_F) and a reverse (I_R) component. The forward and reverse components are a function of $V_P - V_S$ and $V_P - V_D$ through a specific current I_S, respectively. The function is quadratic in strong inversion and exponential in weak inversion. V_P is the pinch-off voltage and is a function of gate voltage for long-channel devices. The pinch-off voltage in short-channel devices becomes a function of gate, source and drain voltage due to the charge-sharing effect. An interpolation function is used to model the current in the moderate inversion region which results in a continuous expression for all regions of operation.

The details of the EKV MOS model equations can be found in [82, 86].

The focus of this research is on developing design methodology for low-power and low-noise integrated readout circuits for capacitive and in particular, for solid-state radiation detectors. We will show how to design an integrated readout circuit for CdZnTe detectors based on the described methodology as a proof of concept. Unique features and recent advances in these detectors will be taken into account and the analog channel will be optimized to achieve high efficiency and performance. As estimation of the noise performance of state-of-the-art readout circuit is an important factor in designing an optimized readout system, we will show how to analytically derive the noise equations of the system taking into account the behaviour of devices in ultra-deep submicron CMOS processes.

1.3 Summary of Contributions

In this thesis, we provide a detailed analysis of capacitive detector readout circuits. We start off by introducing the procedure for designing a readout system for capacitive detectors. We discuss all the important steps of the procedure, including analyzing the specifications, choosing an appropriate technology for the realization of the design, designing the analog and digital blocks, noise evaluation, layout considerations and chip design. We present state-of-the-art designs of each block of the system, compare the designs, and discuss advantages and disadvantages of each design. Furthermore, we present a comprehensive noise analysis of modern capacitive detector readout circuits. We take into account the new noise sources associated with deep submicron technologies. The analysis is based on the EKV model [82] of MOS transistors which is a model valid for all regions of operation.

As a proof of concept, we present the analysis and design of a novel low-power charge-sensitive amplifier and the design and analysis of a readout system for solid-state radiation detectors. The analytical equations for the estimation of the noise of the readout system are derived. The proposed circuits are fabricated in a 0.13 μm CMOS process. We briefly review the contributions in the following subsections.

1.3.1 Analytical Noise Analysis of Front-end Circuits for Solid-State Radiation Detectors

In this work we analyse the noise behavior of state-of-the-art readout systems for solid-state radiation detectors in detail. We will derive the equivalent noise charge (ENC) equations of the system analytically taking into account the additional noise contributions and the requirement of modern readout systems. Unlike other noise analysis methods, the analysis given in this work is based on the EKV model of MOS transistors which is valid for all regions of operation (i.e., from weak to moderate and strong inversion regions). A Semi-Gaussian pulse shaper is used as an example to show the procedure for noise analysis and optimization. The effects of the design parameters of the shaper on the ENC equations of the readout system are discussed.

1.3.2 A Low-Power Charge-Sensitive Amplifier

In this work the design of a novel low-power continuous-reset CMOS CSA is presented. The proposed CSA is intended for capacitive sensor readout circuits, in particular, interface circuits for solid-state detectors used in medical imaging and X-ray spectroscopy. A proof-of-concept interface circuit is designed and fabricated in a 0.13-μm CMOS process and consists of the proposed CSA, a pole-zero cancellation circuit, and a second-order semi-Gaussian programmable pulse shaper. Unlike most of the CSAs in the literature, the proposed CSA can accept signals of both polarities. Measurement results confirm low-power operation of the circuit. The CSA consumes only 37.5 μW from dual supply voltages of 0.9 and 1.2 V. The measured equivalent noise charge of the CSA is about 111 $\bar{e}$-rms.

1.3.3 Design and Analysis of a 4-Channel Readout System for Solid-State Radiation Detectors

In this work we present the design and analysis of a low-power and low-noise 4-channel readout circuit intended for the readout of solid-state radiation detectors (in particular, CZT detectors). The circuit consists of a CSA, a reset network to provide a discharge path for the feedback capacitor, and a first-order pulse shaper with a pole-zero cancellation (PZC) circuit. We have presented a simple method to adjust

the discharge time constant of the CSA in order to accommodate various event rates. Moreover, we have proposed a simple method for the overshoot removal at the output of the pulse shaper when the discharge time constant of the CSA is adjusted. Furthermore, a comprehensive noise analysis of the readout system is presented and the design is optimized in terms of noise performance and power consumption. A proof-of-concept interface circuit is laid out and fabricated in a 0.13-μm CMOS technology. Measurement results of the circuit confirm the low-noise and low-power operation of the readout system. The readout system offers excellent power consumption and superior noise performance in comparison with similar works in the literature.

1.3.4 Design and Analysis of a Complete Readout System for Solid-State Radiation Detectors

In this work we focus on the design and analysis of the pulse shaper and the signal processing blocks of a readout system. As a proof of concept, we will design and integrate a complete mixed-signal readout system. The integrated readout system consists of a CSA with leakage compensation, a Gaussian pulse shaper, a PDH, a discriminator, and a Wilkinson-based ADC. In addition to conventional blocks of a Wilkinson-type digitizer, the ADC contains additional circuitry that prevents a voltage drop at the moment when conversion commences. The test chip is laid out and fabricated in a 0.13 μm CMOS technology. Measurement results of the readout circuit confirm the feasibility of the design. The readout system performs favourably in terms of power consumption and noise behavior in comparison with similar works in the literature.

1.4 Thesis Outline

So far, we have introduced the readout system for solid-state radiation detector and discussed the challenges involved in designing low-power and low-noise readout circuits. The rest of the thesis is organized as follows.

In chapter 2, we present the methodology for designing a low-power and low-noise readout system for capacitive radiation detectors. The methodology includes analyzing the specifications of the detector and the system, choosing an appropri-

ate technology for the realization of the system, designing the analog and digital blocks, noise evaluation, layout considerations, and chip design. In Chapter 3, we provide a detailed noise analysis of modern readout systems for capacitive and in particular, solid-state radiation detectors in detail. We will derive the equivalent noise charge equations of the readout system analytically taking into account the additional noise contributions and the requirement of the readout system. In Chapter 4, the design of a novel low-power continuous-reset CMOS charge-sensitive amplifier is presented. The proposed CSA is intended for capacitive sensor readout circuits, in particular, interface circuits for solid-state detectors used in medical imaging and X-ray spectroscopy. A proof-of-concept interface circuit is designed and fabricated employing the proposed amplifier. Measurement results of the readout system are presented. In Chapter 5, we focus on the design and noise analysis of a low-power and low-noise four-channel readout circuit consisting of a CSA and a first-order pulse shaper. We present a comprehensive noise analysis of the readout system. Measurement results of the readout system are also presented and the design is compared with similar works in the literature. In Chapter 6 we discuss the design and analysis of a complete mixed-signal readout system. The focus of the design is on the pulse shaper and signal processing circuits. We present detailed design and analysis of the blocks. The measurement results of the fabricated chip are presented and discussed. Finally, Chapter 7 summarizes the research results and future work.

Chapter 2

Readout System Design for Capacitive Radiation Detectors

In this chapter the procedure for designing a readout system for capacitive solid-state radiation detectors is described. A readout system consists of the radiation detector, readout circuit, supporting structures, and cooling (if any). To properly design an efficient readout system, both system- and circuit-level requirements must be taken into account. A successful design requires making trade-offs on several design aspects which cannot be optimized simultaneously.

2.1 System Specifications

From a system point of view, a designer must consider several specifications. The main system-level specifications are summarized in Table 2.1 [87]. It is worth mentioning that these specifications cannot be optimized simultaneously and the designer must make trade-offs carefully.

2.2 Circuit Design Specifications

In analog circuit design the designer is given a set of specifications and is asked to transform the specifications into circuits. The designer has to find an optimal solution to the given problem such that the design requirements are met. This involves finding the right technology, creating schematics and layouts, and then

Table 2.1: System-level specifications for capacitive detector readout systems

Specification	Description
Detector geometry	How to arrange the detector modules? How many modules are needed? What is the coverage of the modules? Are there any dead regions?
Efficiency	How much charge must be collected for efficient detection? what are the properties of the detector that affect the noise of the system?
Event rate	What is the event rate of the system? Would the readout circuit be able to deal with the event rate? Is segmentation required?
Readout	What is the architecture of the readout circuit? What are the burdens on the readout circuit?
Cooling, support structures and cables	What are the required mechanical supports? Is cooling required? How the data are readout?
Cost	What is the overall cost of the system? How does the cost of the system affect the design considerations? Does the cost of the system affect its robustness?

simulating the design using available tools. The designer has to change and optimize the design numerous times until simulations confirm that the design meets all the specifications.

When the circuit to be designed is intended for the readout of radiation detectors, the design must satisfy the characteristics of the sensor as well as the requirements of the readout system. The main circuit design specifications of capacitive detector readout systems are summarized and described in Table 2.2.

Table 2.2: Main circuit design specifications for capacitive detector readout systems

Specification	Description
Detector capacitance	The capacitance of each pixel that loads the charge amplifier.
Detector leakage current	The leakage current of each pixel that must be compensated.
Energy range	The range of absorbed energy by the detector.
Energy resolution	The smallest amount of deposited energy (or equivalently charge) that the system must be able to process.
Input dynamic range	The maximum amount of charge that the system must handle linearly.
Signal-to-noise ratio (SNR)	SNR determines the gain and noise level of the system.
Counting rate	Counting rate determines how fast the readout system must process the signals.
Radiation hardening tolerant	Determines if the readout system must use processes that are tolerant to radiation
Power consumption	The maximum possible power consumption of the readout system
Size	The size of the module or the integrated circuit

2.3 Technology Selection

After analyzing the design requirements, the designer must decide on the technology to use for the integration of the design. A number of technologies exist for the realization of circuits including Bipolar, SOI, CMOS, and BiCMOS to name a few.

Bipolar devices are often used for amplification. They can switch signals at very high speeds and can provide large currents to the loads. So they are used in high frequency, high slewing, or high bandwidth applications. They are not suitable candidates for applications that require high input impedance.

SOI technology is based on the use of a layered silicon-insulator-silicon substrate. In comparison with Bulk CMOS technology, it offers a lower parasitic capacitance, lower leakage current, less antenna issues, resistance to latchup, and a higher performance. However, it is not well adapted for the development of typical analog circuits. This technology is mostly used in silicon photonics, microprocessors, and high performance radio-frequency applications.

Bulk CMOS has been a popular choice for the integration of circuits. The process is well-adapted for analog, digital, and mixed-signal applications. When it comes to small scale fabrication, it is very economical to use CMOS processes thanks to foundries that offer multi-project runs. The disadvantages of using bulk CMOS technology are high flicker noise, rapid scaling of technology which results in reduction of dynamic range and worsening of noise. When compared to Bipolar technology, CMOS devices have worse matching. They also need to burn more power for a given transconductance. In short, Bipolar technology offers better performance for the design of amplifiers, while CMOS technology has better noise performance, and offers many advantages for the integration of digital circuits.

A BiCMOS process, as the name suggests, is designed to offer the advantages of both Bipolar and CMOS technologies. The disadvantage of this technology is that many advantages of CMOS and Bipolar technologies are not directly offered by this technology without extra fabrication steps which adds to the cost. So the complexity of process and cost have been major factors in preventing this technology from widespread use.

2.4 Readout Circuit Design

As described in the previous chapter, a readout system usually contains various stages for signal amplification, pulse shaping, digitization and further signal processing. Depending on the available silicon area and power consumption budget, the pulse shaping, digitization and signal processing may be performed outside of the integrated device using available commercial ICs. Figure 2.1 shows a detailed block diagram of a complete readout system. A readout channel may contain one or more of the following building blocks.

- Charge-Sensitive Amplifier (CSA)

- Reset Network
- Pole-Zero Cancellation (PZC)
- Pulse Shaper
- Peak-Detect and Hold (PDH)
- Discriminator
- Analog-to-Digital Converter (ADC)

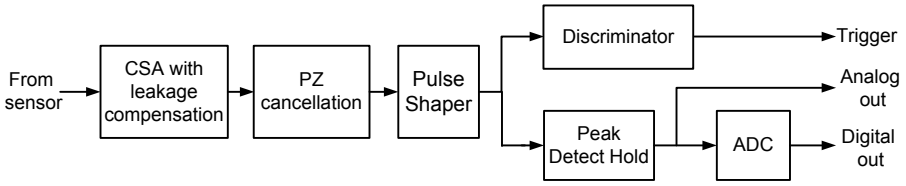


Figure 2.1: The block diagram of a complete readout channel.

The signal at the output of the shaper (or sometimes CSA) must be digitized for storage or further processing. Analog-to-Digital Converters (ADCs) are used for this purpose. The waveform at the output of the pulse shaper must be tracked and then its peak value stored before passing the signal to the ADC. A Peak-Detect and Hold (PDH) circuit performs this task. For systems with a large number of channels, it is impractical to allocate an ADC per channel due to high cost in terms of area and power. Thus it is essential for such systems to multiplex the outputs of channels into a fewer number of ADCs. This way, only the events that need to be digitized are processed by the ADCs. Obviously, a trigger signal must be generated to identify the events. A discriminator is used for generating a trigger signal. A trigger signal is generated whenever the signal level at the output of the shaper is higher than a threshold level. In the following sections, we describe the operation and design of each block in detail.

2.4.1 Charge-Sensitive Amplifier

Charge-sensitive amplifiers are widely used in the design of readout circuits for various capacitive sensors, in particular, for solid-state radiation detectors. Other applications of CSAs include amplification of signals from piezoelectric sensors [88], photodiodes [89], and charge-coupled device (CCD) imagers [90]. Insensitivity of the gain to detector capacitance variations is the main motivation of using CSAs in the front-end circuit of readout systems [22]. To maximize the achievable resolution, the noise of the readout circuit must be minimized. Since the noise of the system is mainly dominated by the noise of the CSA input device, designing a low-noise low-power CSA is of paramount importance in such readout circuits.

Several design architectures exist for CSAs in the literature. Single-ended configuration is commonly used in design of CSAs to save power. In CSA design it is desired to increase the transconductance of the input device in order to improve both speed and noise performance which ultimately results in increased device width and capacitance. Use of cascode circuitry allows the designers to couple a wide input device with narrow cascode devices. This unique feature of a cascode topology helps provide a high gain as well as a high GBW. However, there is a conflicting trade-off associated with the cascode topology. From a noise point of view, the input device must operate at a high current level in order to achieve a good noise performance. In contrast, in order to have a high output resistance (and consequently a high gain), low cascode current level is desired. To overcome this problem, folded-cascode-based designs have been introduced by the designers. In folded-cascode topology the DC and signal paths are separated. Therefore, the input device and the cascode branch can operate at their optimum current levels to achieve both a low-noise performance and a high gain. Early designs used the cascode topology [89, 91–93], however, most of the current designs are based on the use of folded cascode topology [8, 44, 71, 94–102]. In addition to cascode and folded-cascode designs a few different architectures exist in the literature. For example, in [103] an all NMOSFET CSA is proposed that has a power consumption of only 1.2 μW but uses zero threshold voltage devices. In [96] split-leg straight cascode is chosen for implementation of the CSA which maximizes the current in the input device. However, the output voltage swing is reduced compared to a

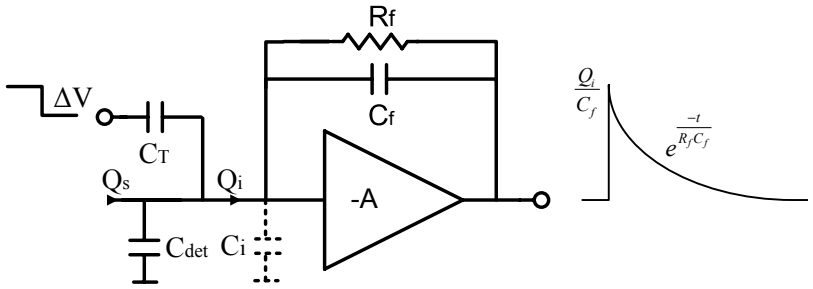


Figure 2.2: Principle operation of a typical CSA. C_{det} and C_T are the detector and test capacitances respectively. The input dynamic capacitance is represented as $C_i = (A+1)C_f$.

split-leg folded cascode topology. In addition to standard CMOS designs, other topologies exist for CSAs in the literature that use either bipolar or JFET devices [104–110].

Figure 2.2 shows the principle of operation of a typical CSA. A CSA consists of an inverting voltage amplifier with a high input resistance, a feedback capacitance and a reset network (R_f here). We assume that an input signal produces a signal charge of $Q_s = Q_i + Q_{det}$ where Q_{det} is the deposited charge on the detector capacitance and Q_i is the delivered charge to the input node of the CSA. Since the amplifier ideally has an infinite input resistance, no current can flow into the amplifier and thus all the delivered charge must be integrated on the feedback capacitance.

$$Q_i = C_f v_f = C_f[v_i - (-A)v_i] = (1+A)C_f v_i. \tag{2.1}$$

Therefore, C_f appears as a dynamic input capacitance with an enhanced value of

$$C_i = \frac{Q_i}{v_i} = \frac{(1+A)C_f v_i}{v_i} = (1+A)C_f. \tag{2.2}$$

The ratio of the integrated charge to signal charge then equals to

$$\frac{Q_i}{Q_s} = \frac{C_i}{C_i + C_{det}} = \frac{1}{1+\frac{C_{det}}{C_i}}, \tag{2.3}$$

which suggests that maximum charge transfer occurs when the dynamic input capacitance is considerably larger than the detector capacitance (i.e., $C_i \gg C_{det}$). One advantage of CSAs compared to voltage amplifiers is that the charge gain is well-defined.

$$A_Q = \frac{v_o}{Q_i} = \frac{Av_i}{C_i v_i} = \frac{A}{(1+A)C_f} \approx \frac{1}{C_f}. \tag{2.4}$$

Another advantage is ease of charge calibration. A test capacitor can be integrated on chip which can be used to inject a well-defined charge into the input node of the CSA (see Figure 2.2). If a voltage step of $\triangle V$ is applied to a test capacitance of C_T, the injected charge will be equal to

$$Q_{inj} = \frac{C_T}{1+\frac{C_T}{C_i+C_{det}}} \triangle V \approx C_T(1-\frac{C_T}{C_i+C_{det}}) \triangle V. \tag{2.5}$$

We will now calculate the input time constant of a CSA. This is particularly important in order to understand how quickly charge is transferred from the detector and also to estimate the required Gain-Bandwidth Product (GBW) for the CSA. At frequencies much larger than the corner frequency (f_c) of the amplifier and much smaller than the unity gain frequency (f_0), the input impedance of the amplifier can be approximated as

$$Z_i = \frac{Z_f}{1-A_v} \approx \frac{Z_f}{-A_v} = \frac{\frac{1}{j\omega C_f}}{\frac{-1}{j(\frac{\omega}{\omega_0})}} = \frac{1}{\omega_0 C_f}, f_c \ll f \ll f_0. \tag{2.6}$$

which appears as a resistance (R_i). Therefore, the detector capacitance is discharged by a time constant of

$$\tau_i = R_i C_{det} = \frac{1}{\omega_0 C_f} C_{det} = \frac{1}{\omega_0(\frac{C_f}{C_{det}})}. \tag{2.7}$$

The required GBW of the amplifier can be calculated using (2.7). By combining (2.3) and (2.7), the charge transferred to the amplifier can be approximated as

$$Q(t) \approx \frac{Q_s}{1+\frac{C_{det}}{C_i}}(1-e^{\frac{-t}{\tau_i}}). \tag{2.8}$$

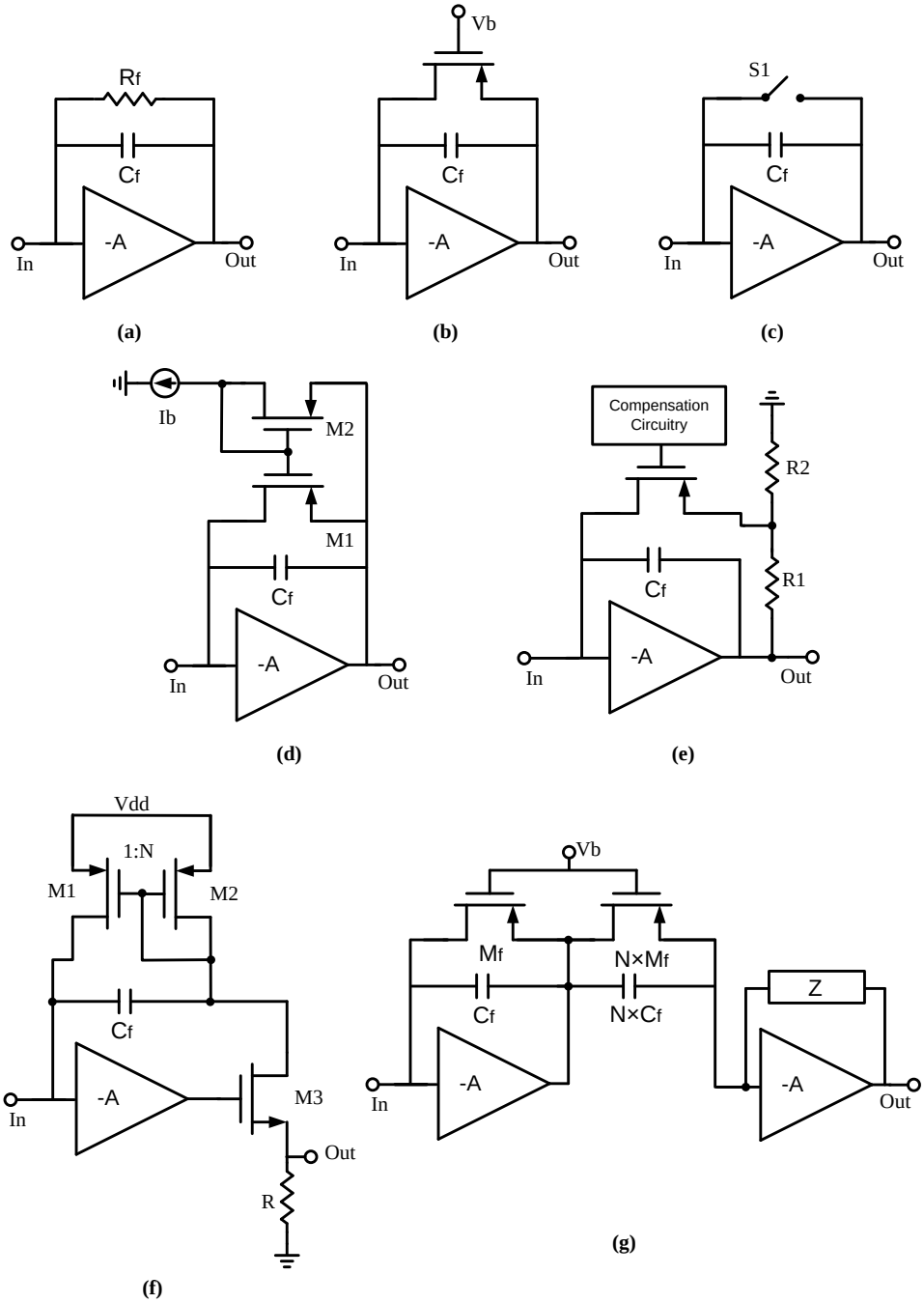
In this equation C_i determines what fraction of the signal charge from detector is transferred to the amplifier and the time constant, τ_i, determines how quickly the charge is transferred.

2.4.2 Reset Network

As explained earlier, the generated charge from the detector is integrated on the feedback capacitor. After integration, the voltage across the capacitor must be discharged in order to prepare the system for another event. The role of a reset network is to provide a path for discharging the capacitor either continuously or discretely. The reset network must be carefully designed as it directly contributes to the noise of the system. The discharge time of the CSA must be significantly larger than the shaping time and also short enough to prevent pulse pile-ups at high event rates. Implementing a large discharge time has the challenge of integrating a high value feedback resistor in the reset network. In our work, we need a circuit that can accommodate leakage current of CZT detectors in the range of 1 fA to 50 nA.

A number of reset mechanisms can be found in the literature based on the target application. The reset circuit are typically based on the use of a resistor [1], MOS device [2, 3], MOS switch [4, 5], current mirrors [6], self-adaptive biasing scheme [7, 8], current conveyor feedback [9], MOS device and N times replica of it [10, 11], low-frequency feedback loop [12–14], or cold resistor [15] (see Figure 2.3). Reset circuits that use resistors (see Figure 2.3a) are simple to design, however, it is often desired to increase the time constant of the reset network by increasing the value of the resistor. Integrating a large-value resistor is difficult and area consuming. Besides, the leakage current of the detector can saturate the charge amplifier if the value of the resistor or the leakage current is high enough. The resistor is usually used in applications where charge integration and pulse shaping is fast.

In the single MOS device configuration shown in Figure 2.3b the reset device is biased with a constant voltage source which provides the desired resistance. The device is usually biased in weak inversion (or subthreshold) region to provide a high-value feedback resistance. This is essential in order to increase the discharge


Rf
Cf
-A
In
Out
(a)
Vb
Cf
-A
In
Out
(b)
S1
Cf
-A
In
Out
(c)
Ib
M2
M1
Cf
-A
In
Out
(d)
Compensation Circuitry
R2
R1
Cf
-A
In
Out
(e)
Vdd
1:N
M1
M2
Cf
-A
In
M3
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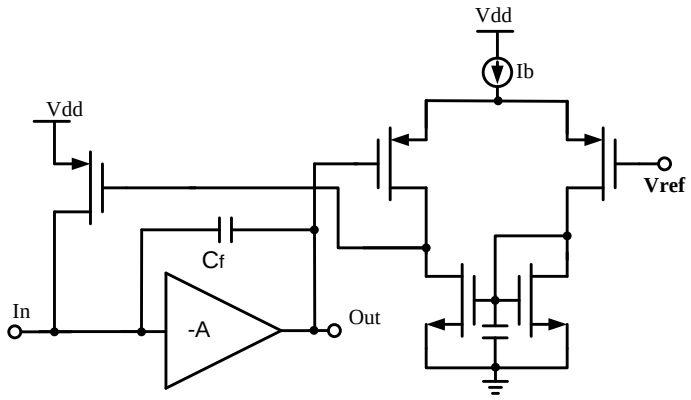
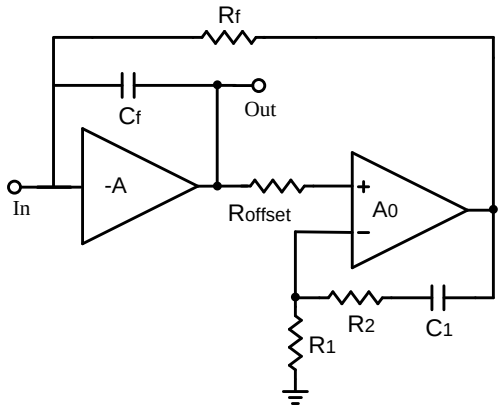


(h)



(i)

Figure 2.3: Common reset circuits using a (a) resistor [1], (b) MOS device [2, 3], (c) MOS switch [4, 5], (d) current mirror [6], (e) self-adaptive biasing scheme [7, 8], (f) current conveyor feedback [9], (g) a MOS device and N times replica of it [10, 11], (h) low-frequency feedback loop [12–14], and (i) cold resistor [15].

time-constant of the CSA and to lower the noise contribution of the resistor. This configuration is advantageous over a single resistor from an area point of view, however, the MOS device may exhibit non-linearities that need to be compensated in the next stages.

The MOS switch configuration (see Figure 2.3c) operates with a periodic reset signal and discretely discharges the capacitor. This configuration suffers from charge injection and does not provide a discharge path for the leakage current of the detector.

In the current mirror configuration shown in Figure 2.3d device M_2 is biased in the linear region. If a signal appears at the output of the CSA, the device enters the saturation region and the bias current is copied to M_1. Device M_1 then discharges the capacitor with a constant current equal to $I_b + I_{leak}$ where I_{leak} is the leakage current of the detector. The bias current of the MOS devices must be small in order to reduce the noise contributions of the reset network. This configuration may introduce additional non-linearities that need to be compensated. The leakage current of the detector can cause a DC shift at the output of the charge amplifier.

In the self-adaptive biasing scheme shown in Figure 2.3e the output voltage is attenuated and applied to the source terminal of a PMOS device which is biased in weak inversion region. Since the effective drain-source resistance of the MOS device is extremely dependent on the biasing condition, an adaptive compensation circuitry is designed which compensates for the variations in the temperature, threshold voltage of the device, and the node voltages. This reset configuration can accommodate a large leakage current because when the leakage current increases, the effective resistance of the device reduces and prevents the CSA from saturation. However, accommodation of the leakage current is achieved at the expense of introducing additional non-linearities like the change in the associated pole.

The current conveyor feedback (see Figure 2.3f) consists of a source follower, a small resistor, and a current mirror. The drain current of M_3 is proportional to the output voltage (i.e., $V_{out} = R.I_{D3}$). This current is scaled down by the current mirror and then injected back to the input. Thus the configuration provides an equivalent feedback resistance equal to $N.R$ where N is the current gain of the current mirror. A Bipolar Junction Transistor (BJT) is used as the input device of the CSA in order to sink the leakage current of the detector. This scheme offers a good linearity by

using a resistor. The noise from the resistor and the scaling down network must be minimized.

The configuration shown in Figure 2.3g uses a MOS device and a feedback capacitor connected to the next stage through N times replica of the MOS and the feedback capacitor. The MOS devices are biased above threshold and in the saturation region. They share the same gate-to-source voltage. An N times leakage current of the detector appears at the input terminal of the following stage which must be absorbed without saturating the stage. This configuration completely compensates the leakage current of the detector and also provides a good linearity, however, implementing and matching of N times replica of the MOS and the feedback capacitor is challenging (e.g., N can be as high as 144).

The low-frequency feedback loop shown in Figure 2.3h uses a differential pair and a current mirror. Each transistor of the differential pair is biased at $I_b/2$ in the steady state mode. After each integration the output of the CSA recovers back to its DC level (i.e., V_{ref}) thanks to the low-frequency feedback loop. This configuration offers a good linearity and complete leakage compensation.

The cold resistor configuration shown in Figure 2.3i uses an amplifier and passive components to automatically zero the DC voltage at the output of the CSA. This configuration can provide full leakage compensation. The reset mechanism used in the configuration reduces the effective value of the feedback resistor (i.e., makes it a cold resistor). As a result, the resetting process becomes faster with no additional noise and no loss of sensitivity. However, the offset voltage of the amplifier needs to be compensated or will affect the final offset of the circuit.

Amongst the mentioned reset configurations, the Krummenacher's low frequency feedback loop is the most popular one [23, 44, 111]. In this circuit the output of the CSA is compared with a reference voltage and then drain current of a MOS transistor is adjusted to compensate the leakage current. This configuration provides full leakage compensation but may introduce a pole and a zero and some non-idealities that need to be compensated.

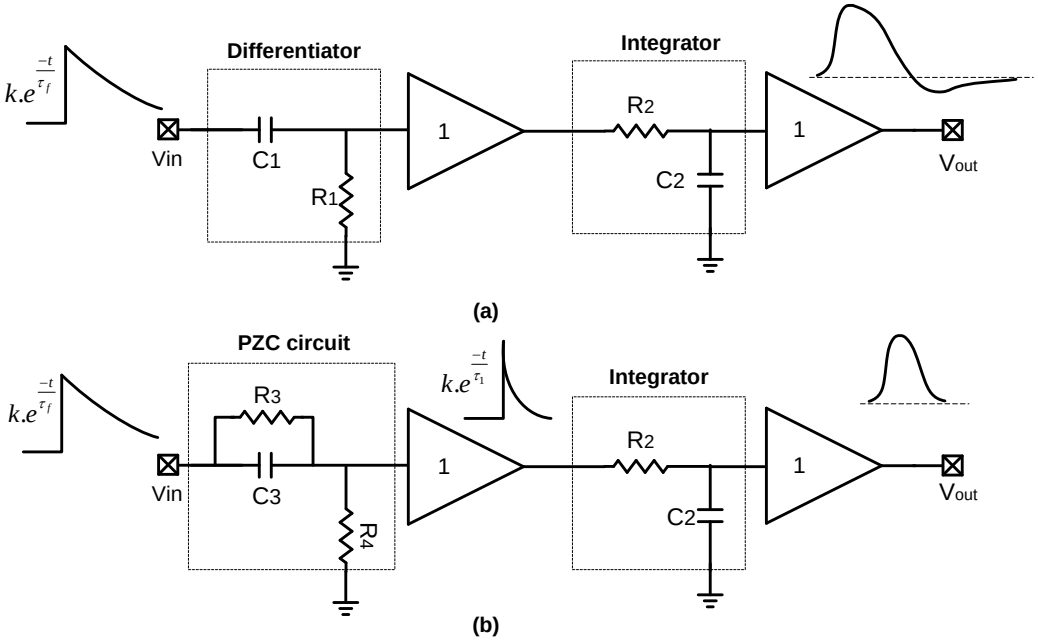


Figure 2.4: (a) Circuit schematic of a first-order CR-RC pulse shaper, and (b) use of a PZC network in the CR-RC pulse shaper circuit to cancel the long decay time of the input signal.

2.4.3 Pole-Zero Cancellation (PZC) Circuit

The signal from the charge-sensitive amplifier is not an ideal step function and has a finite decay time. If this signal is passed through a shaping network, the finite decay time of the amplifier causes a long undershoot at the output which is undesired. The amplitude of the undershoot is higher when the amplifier passes a large pulse to the pulse shaper. This will temporarily shift the baseline which is also undesired. In order to suppress the undershoot at the output of the pulser shaper, the associated pole with the preamplifier must be cancelled. This is achieved using a pole-zero cancellation (PZC) network. To see how the PZC circuit functions, let's consider a first-order pulse shaper and analyze the equations.

Figure 2.4a shows a first-order CR-RC pulse shaper. The transfer function of

the pulse shaper is given by

$$\frac{Vout(s)}{Vin(s)} = \frac{s\tau_1}{(1+s\tau_1)(1+s\tau_2)}, \tag{2.9}$$

where τ_1 and τ_2 are the time constants of the differentiator and integrator in the pulse shaper's network respectively. The signal from the preamplifer has a form of $k.\exp(\frac{-t}{\tau_f})$ and is passed to the pulse shaper. The resulting output signal in frequency domain is

$$Vout(s) = \frac{k\tau_f}{1+s\tau_f}\frac{s\tau_1}{(1+s\tau_1)(1+s\tau_2)}. \tag{2.10}$$

As can be seen in (2.10), the associated pole with the preamplifier appears at the output of the pulse shaper. It is possible to cancel this pole by introducing a zero in the transfer function of the pulse shaper. The modified circuit of the pulse shaper is shown in Figure 2.4b. In this figure, the differentiator is replaced with a circuit that produces a zero and a pole in the transfer function of the pulse shaper. The output signal in Figure 2.4b is given by

$$Vout(s) = \frac{k}{s+\frac{1}{\tau_f}}\frac{s+\frac{1}{R_3C_3}}{s+\frac{1}{C_3}(\frac{1}{R_3}+\frac{1}{R_4})}\frac{1}{s+\tau_2}. \tag{2.11}$$

In (2.11), if we set $\frac{1}{\tau_f} = \frac{1}{R_3C_3}$ and $\frac{1}{C_3}(\frac{1}{R_3}+\frac{1}{R_4}) = \frac{1}{\tau_1}$, then the equation for the output signal in frequency is reduced to

$$Vout(s) = \frac{k}{s+\tau_1}\frac{1}{s+\tau_2}. \tag{2.12}$$

The above equation shows that the associated pole with the preamplifier is cancelled by the zero of the PZC network.

2.4.4 Pulse Shaper

In detector readout circuits, the signal from the CSA is often passed through a filter before performing amplitude or time measurements. As the filtering process affects the amplitude or timing of the pulse signal, this type of signal processing

is called pulse shaping. The most common pulse shaping method is to produce a pulse whose peak amplitude is proportional to the detected charge in the detector.

Several pulse shaping methods can be found in the literature including CR-RC [23, 44], trapezoidal/ triangular [112, 113], delay-line [114, 115], and Semi-Gaussian (SG) pulse shaping [10, 21, 95]. Passive CR-RC pulse shapers are realized by cascading a differentiator by an integrator. They can also be realized using active elements. The simplicity of design and ease of controlling the shaping time makes these pulse shapers very attractive. However, the signal-to-noise ratio (SNR) in this pulse shaping method is not very good and large pulse pile-up errors will occur at high event rates because of the long tail of the output pulse. The problem of slow return to zero can be solved by adding another differentiation stage. The resulting pulse shaping filter is called double differentiation shaper. This pulse shaper produces bipolar shaped pulses which are useful for high event rate applications. In practice, double differentiation shaping introduce a small baseline shift as the two lobes of the shaped signal are not of exactly equal area. At low event rates, the noise performance of these pulse shapers is worse than that of CR-RC shapers.

Theoretically, triangular pulse shaping results in a higher SNR compared to CR-RC or Gaussian shaping. In practice, true triangular shaping can not be realized using passive components. However, it is possible to achieve a semi-triangular pulse shaping by using active elements but the design is usually difficult and cost-ineffective. Trapezoidal pulse shapers are mostly used for detectors in which the charge collection time is dependent on the position of radiation interaction. The flat top of these pulse shapers results in pulses with the same peak amplitudes whereas use of others pulse shapers without a flat top will produce pulses with slightly different amplitudes. Delay-line shapers (single or double) are not popular choices for high resolution solid-state detectors due to their poor noise performance. They usually introduce undesirable artifacts into the signal and to alter the width of the pulse it is necessary to change the length of the delay line [22].

SG filters are the most popular pulse shapers for solid-state radiation detectors. They can be realized using either active or passive elements. The peaking time in these shapers is longer than CR-RC pulse shapers and the shape of the signal is more symmetrical. This results in a faster return to the baseline and thus pulse pile-up errors at high event rates are reduced. A 4^{th}-order SG shaper produces shaped

pulses which are quite close to true Gaussian ones.

2.4.5 Peak-Detect and Hold (PDH)

The analog voltage at the input of the ADC must stay constant during conversion. To fulfil this requirement, the output of the pulse shaper must be passed to a PDH circuit (also called a pulse stretcher). The PDH generates a signal with an amplitude equal to the height of the input signal but for a longer duration. The most simple PDH consists of a diode and a capacitor which is shown in Figure 2.5a. Figure 2.5b shows a modified version of this architecture which effectively decreases the impedance of the diode by a factor of (A+1). The main drawback of this circuit is the reverse dark current of the diode which causes progressive lowering of the hold voltage. Figure 2.5c shows a popular CMOS PDH [39, 116–119]. The rectifying elements in this architecture are realized using current mirrors instead of diodes. The circuit in Figure 2.5c suffers from offset. An offset-free two-phase PDH is proposed in [120]. Another design for high speed and high event rate applications is introduced in [121] which is based on the offset-free two-phase circuit described in [120]. The proposed design uses a leakage compensation scheme to lower the output DC error. Another design is introduced in [122] which uses two ramps with different slopes to sample the input voltage. The simulated error of the peak value is less than 1% for this design and the droop voltage is less than 20 $\mu V/\mu s$. The drawback of this approach is its high power consumption.

2.4.6 Discriminator

Pulse height discriminators are used to generate trigger signals for the channels with incidents. Ideally, a discriminator must deliver a signal when the input pulse height is higher than a threshold level regardless of the input pulse shape. The discriminator must also recover fast enough and completely in order to process two close signals. In addition, the dead-time must be constant with respect to the pulse height of the signal at the input of the discriminator.

A common method to realize a discriminator is by using a fast comparator. The general design techniques for high-speed comparators is described in [123]. A fully differential realization of a discriminator is presented in [124]. In [125], the

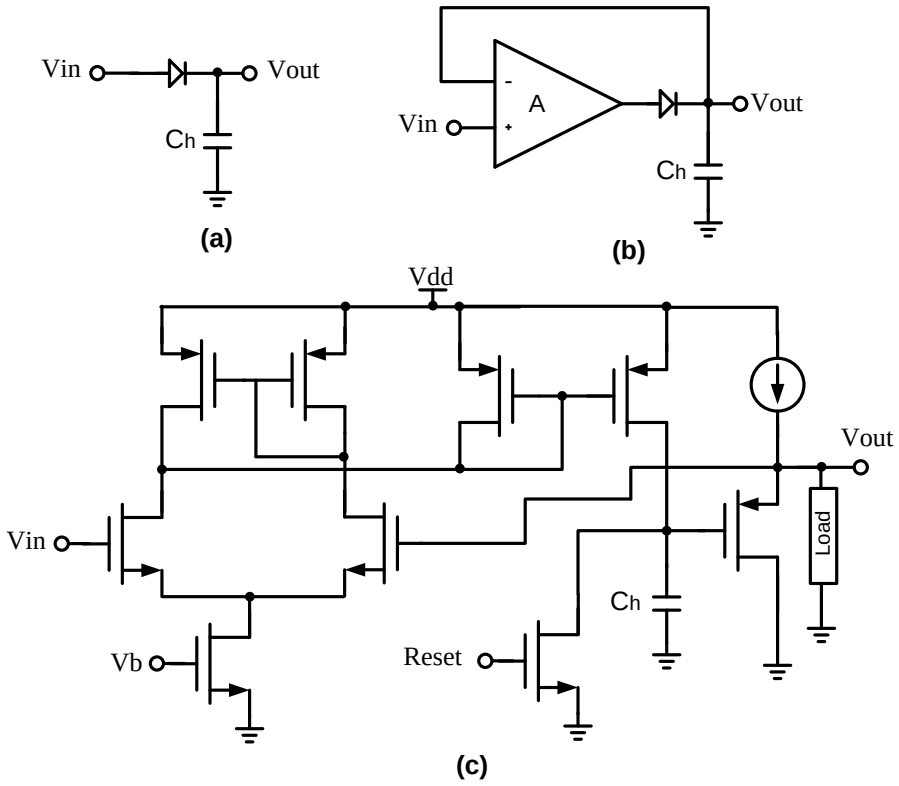


Figure 2.5: PDH employing (a) a diode, (b) an amplified diode, and (c) current mirrors and an OTA.

design of high-speed and high-resolution multi-stage comparators is described in detail. The design is optimized in terms of number of stages as well as the offset of the circuit. A low-power autozeroed high-speed comparator is introduced in [126]. The achieved resolution is better than 1 mV at operating speeds more than 10 MHz.

2.4.7 Analog-to-Digital Converter (ADC)

The ADCs used in detector readout circuits must satisfy several design specifications:

- Resolution

  The resolution of an ADC is a measure of granularity of the digitized output. In order to accurately digitize the analog input, the resolution of the ADC must be considerably better than the noise level of the input. This means that the digitization error must be small compared to the noise level of the input signal.

- Integral nonlinearity

  This parameter shows how much the relationship of the digitized output to the analog input deviates from absolute linearity. The linearity of the ADC varies by the pulse shape and duration of the input signal. Increasing the duration of the input signal can improve the integral nonlinearity of the ADC.

- Stability

  Stability shows whether conversion gain and baseline change over time. In precise measurements it is necessary to monitor changes in conversion parameters of the ADC.

- Differential nonlinearity

  Differential nonlinearity is used to express how uniform the digitization increments are. Special attention must be given to the differential nonlinearity as a differential nonlinearity of higher than $\pm$ 0.5 LSB can result in a nonmonotonic conversion. This means for some analog inputs an increase in signal will generate decreased digital outputs. In poor ADC designs the width of bins may differ systematically.

- The count-rate performance

  The count-rate performance of the ADC must be examined carefully as detectors often generate signals randomly which is in contrast with most systems where inputs are sampled at regular intervals.

- Conversion time

  This parameter shows how long it takes for the ADC to complete the digitization. Obviously, the system cannot accept a new input during this dead

time. Signal acquisition time, conversion time, and readout time contribute in the dead time of the system. In continuous-event systems, the dead time can be ignored if the event rate is smaller than the conversion time.

Different conversion techniques exist in the literature which are suitable for use in detector readout circuits. Flash [127, 128], successive approximation [129, 130], Wilkinson [131–134], and pipelined [135, 136] ADCs are relevant architectures which are usually used for digitization of the output signal of the pulse shapers. A combination of these architectures may also be used in order to obtain high resolution and fast conversion time. The principle of operation and pros and cons of relevant digitization techniques are reviewed.

- Flash ADC

  Flash conversion is the simplest technique which enables fast conversion but with the expense of area and high power consumption. In this technique the analog input is fed to a bank of comparators. An n-bit converter requires 2^n comparators. The threshold voltage of comparators are set by a resistive divider which provides a constant relative resolution over the entire conversion range.

- Successive Approximation Register ADC

  successive approximation register (SAR) ADC is commonly used in various readout circuits which require medium to high resolution of digitization. This technique makes efficient use of circuitry but with a drawback of poor differential nonlinearity. In this technique the analog input is fed to a pulse stretcher and a binary search algorithm is used to determine the digitized output. In the first step the Most Significant Bit (MSB) of the output code is set to 1 and the code is passed to a digital to analog converter (DAC). This forces the output of the DAC to be Vref/2 where Vref is the reference voltage supplied to the DAC. The output voltage of the DAC is then compared with the output voltage of the pulse stretcher. If the output voltage of the DAC is greater than the output voltage of the pulse stretcher, the MSB is set to 0, otherwise remains at 1. In the next step the second MSB is set to 1 and a comparison is made. Again, depending on the result of comparison, this bit

is cleared or remains at 1. The sequence continues until the last bit is determined. Thus, an n-bit successive approximation converter requires n steps. The major concern in this technique is the accuracy of the resistors that set the DAC levels. It is very difficult to implement extremely accurate resistors on chip and this leads to poor differential nonlinearity.

- Pipelined ADC

  Pipelined ADC is one of popular techniques which is used in applications that require fast conversion time. Unlike other techniques, the throughput is determined by the maximum time per stage and not the total conversion time. In one implementation of a 12-bit pipelined ADC the input signal is fed to a sample and hold (S&H) and a 3-bit Flash ADC. The output of the Flash ADC is fed to a DAC with 12-bit resolution. The resulting signal is then subtracted from the original signal which has been maintained by the S&H. The output signal from this stage is then passed to three similar stages sequentially for further quantization. Each stage provides 2 bits of resolution and one bit for error correction. The last 4 bits are resolved using a 4-bit Flash ADC. The drawback of this architecture is high number of components.

- Wilkinson ADC

  Wilkinson ADC was first introduced in 1950 and since then has been widely employed in precision pulse digitization systems. This technique is based on comparison of the voltage across a discharging capacitor with a baseline voltage. The input analog input is first fed to a pulse stretcher/peak detector and its peak amplitude voltage is stored on a capacitor. Then the capacitor is disconnected from the input and a current source is turned on which discharges the capacitor with a constant current. As the discharge commences, a counter is enabled to count the number of clock pulses until the voltage across the capacitor reaches the baseline level. The discharge time of the capacitor and consequently the conversion time is a linear function of the input peak amplitude. This technique basically offers excellent differential linearity as the clock pulses are precise and uniform. Other advantages include efficient use of circuitry and low power consumption. The only drawback is

the relative long conversion time.

In summary, flash ADCs enable fast conversion rates but at the expense of larger area and higher power consumption. SAR ADCs are commonly used in readout circuits which require medium to high resolution digitization. This technique makes efficient use of hardware; however, its relatively poor differential linearity is usually problematic. Pipelined ADCs are also popular candidates which are used in applications that require fast conversion time. Unlike other techniques, the throughput is determined by the conversion time of one stage. The power consumption of these types of ADCs is moderate but they typically have a higher complexity in comparison with SAR structures. The pros and cons of the common techniques for digitization of the output signal of the pulse shaper are summarized in Table 2.3.

Table 2.3: Performance comparison of various digitization techniques for detector readout circuits

Digitization technique	Advantages	Drawbacks
Flash ADC	fast conversion	high number of components
	monotonic conversion	high power consumption
Successive approximation ADC	moderate power consumption	poor differential nonlinearity
	efficient use of circuitry	
Wilkinson ADC	excellent differential nonlinearity	relatively long conversion time
	efficient use of circuitry	
	low power consumption	
Pipelined ADC*	moderate power consumption	high number of components
	fast conversion	

*Assuming Flash ADCs are used in implementation of the pipeline stages

2.5 Noise Evaluation

The minimum detectable signal from the detector is limited by the electronic noise of the readout system. This is often referred to as the detection resolution of the

system. The noise of the readout system must be minimized to improve the resolution of detection. Measurement of energy, timing or position are affected by random noise. For an example, if a timing signal is measured by a comparator, the fluctuations in the leading edge of the signal due to noise is translated into time shifts.

Electronics noise can be divided into random and non-random categories. Random noise in electronic elements has a Gaussian distribution. Three common sources of noise exist in electronic elements which include thermal (or Johnson), flicker (or 1/f), and shot noise.

Thermal noise

This noise is due to thermal fluctuations of the electron distribution in a conductor. The spectral voltage and current densities in a resistance R are [137]

$$\frac{d\overline{e_n^2}}{df} = 4kTR, \tag{2.13}$$

and

$$\frac{d\overline{i_n^2}}{df} = \frac{4kT}{R} \tag{2.14}$$

where k is Boltzman constant and T is the temperature. As the thermal spectral voltage and current densities are independent of frequency, the thermal noise is often referred to as white noise. The total noise is obtained by integrating over the bandwidth of the system. Increasing the bandwidth of the system increases the total noise. Increasing the speed of a pulse measurement system will increase the noise since bandwidth is inversely proportional to rise time.

Flicker noise

This type of noise exists in many electronic devices such as FETs. The source of flicker noise is not unique meaning that different devices can exhibit flicker noise due to different mechanisms. The noise power spectrum has a 1/f dependence and is shown by [138]

$$\frac{d\overline{e_n^2}}{df} = \frac{A_f}{f^{\alpha_f}}, \tag{2.15}$$

where A_f and α_f depend on the device and fabrication process.

Shot noise

Shot noise is due to the statistical fluctuation in the number of charge carriers. Shot noise requires the presence of a current flow with the condition that the carriers are injected independent of each other. This is the case in semiconductor diodes. The frequency spectrum of the noise current is given by [138]

$$\frac{d\overline{i_n^2}}{df} = 2qI, \tag{2.16}$$

where q is the charge of one electron, and I is the current.

To evaluate the noise of a detector readout system simulations and analytical methods are often used. We will discuss analytical noise analysis of modern detector readout circuits in Chapter 3. Noise simulations can be done using commercial circuit simulators (e.g., Cadence Analog Design Environment or HSPICE). The designer specifies the input and output ports of the circuit as well as the frequency range for which the output noise will be calculated. The tool calculates the DC operating points, and computes the transfer function between the specified input and output ports. The simulator linearizes the circuit about the DC operating point and calculates the total noise spectral density at the output port.

2.6 Layout Considerations and Chip Design

After the circuit is simulated a layout must be generated to enable the fabrication of the chip. The layouts are used by the foundries to extract the masks used for fabrication. The geometries of transistors, resistors, capacitors and other components are entered in a computer aided design (CAD) tool (e.g., Cadence Virtuoso®). A number of design rules must be obeyed during the layout. The rules are intended for the manufacturability, robustness, and maximizing the yield of the technology. They prevent failure mechanisms such as electrostatic discharge (ESD), electromigration, antenna effects, and metal fracturing [139]. ESD can be prevented by using ESD structures such as diodes at the input and output pads. To prevent electromigration, metal widths can be made wider. Antenna effects can be avoided

by changing the order of the routing layers, adding vias near the gates, or adding diodes to the nets. Metal fracturing is caused by sharp steps since the required current cannot be passed. To avoid this phenomenon sharp steps must be replaced by several smaller steps.

After the layout is done and the design passed the rule checks, layout versus schematic (LVS) must be called. This is to ensure that the generated layout represents the designed schematic. After this process the parasitics must be extracted. The parasitics mainly include bulk resistances, capacitances between conductors, and capacitances from conductors to ground. The integrated circuit must be simulated again with the parasitics included. This ensures that the parasitics do not cause failure or undesired behaviour.

Once the layout of the chip is done and post-layout simulations are carried out, the chip can be sent to foundries for fabrication. After the device is fabricated, it is usually housed in a packaged. A package protects the die, powers up the circuit, and provides the electrical connection between the circuit and other components of the system.

The integrated circuits used in detector readout systems are exposed to irradiation. Irradiation can cause latch up, shift the threshold voltage of devices, and increase the leakage current. It can ultimately fail the readout circuit. Dedicated radiation hard technologies exist for the systems that require high radiation tolerance. For other systems it is possible to use standard CMOS technologies under conditions.

Irradiation measurements on transistors in different CMOS technologies show that the threshold shift due to irradiation reduces significantly for oxides thinner than about 10 nm [140, 141]. Current sub-micron CMOS technologies offer devices with an oxide thickness in that range. So it is expected that the threshold voltage shift due to irradiation in deep sub-micron technologies would be negligible. However, irradiation can be ionizing which causes leakage in NMOS devices [140]. The leakage current in these devices can be reduced significantly by proper layout techniques. It has been shown in [142] that use of enclosed geometry for NMOS devices and guard rings prevents radiation-induced leakage current in a standard CMOS process. The approach described in [142] is appealing for deep-micron technologies where overhead area is to some extent compensated by the

increased integration density.

Chapter 3

Analytical Noise Analysis of Front-end Circuits for Solid-State Radiation Detectors

3.1 Introduction

In this chapter, we analyse the noise behavior of state-of-the-art readout systems for solid-state radiation detectors in detail. We will derive the ENC equations of the system analytically taking into account the additional noise contributions and the requirement of modern readout systems. The equations are valid for all regions of operation of the input MOS device of the CSA. We will use a Semi-Gaussian (SG) pulse shaper as an example to show the procedure for noise analysis and optimization. We will also discuss the effects of the design parameters of the shaper on the ENC equations of the readout system.

A readout circuit may have one or more amplification stages. Assuming that the circuit is well-designed, the noise of the amplifier chain is dominated by the noise of the first amplifier stage (i.e., the CSA). A CSA must be designed such that its noise is dominated by the noise of its input amplifying device [87]. Since CSAs often employ MOS devices as their input amplifying element, it is essential to understand the noise sources in these devices. In the following subsection we

review the main noise sources in MOS devices.

3.1.1 Noise Sources in MOS Devices

Thermal and flicker noise are the two primary noise sources in MOS devices. Other noise sources that are often neglected include thermal noise associated with the resistive poly-gate, thermal noise associated with the resistive substrate, and shot noise due to the gate leakage current. We hereby review the primary noise sources in these devices. The contribution of other noise sources becomes significant when the devices are realized in ultra-deep submicron technologies. We will deal with such noise sources in the rest of this chapter.

Thermal noise

The thermal noise is due to the thermal velocity fluctuations of the charge carriers in the channel [87]. The behavior of the thermal noise can be modelled by a voltage noise source in the gate of the device. This noise is frequency independent and its spectral power density is given by [82, 138]

$$S_{w,ser} = \Gamma \frac{4k_B T}{g_m}, \tag{3.1}$$

where Γ is the coefficient of the channel thermal noise, T is the absolute temperature, k_B is the Boltzmann's constant, and g_m is the transconductance of the input device of the CSA.

Flicker noise

The origin of flicker noise in MOS devices is the number fluctuation due to charge trapping [138]. This noise can be modelled by a frequency-dependent voltage noise in the gate of the device. The spectral power density of flicker noise is given by [82, 138, 143]

$$S_{f,ser} = \frac{K_{fs}}{f^{\alpha_{fs}} C_{ox} W L}, \tag{3.2}$$

where K_{fs} is the intrinsic process parameter, W is the device width, L is the device length, and C_{ox} is the gate oxide capacitance per unit area. The value of α_{fs} is technology and device dependent. In conventional noise analysis it is often assumed

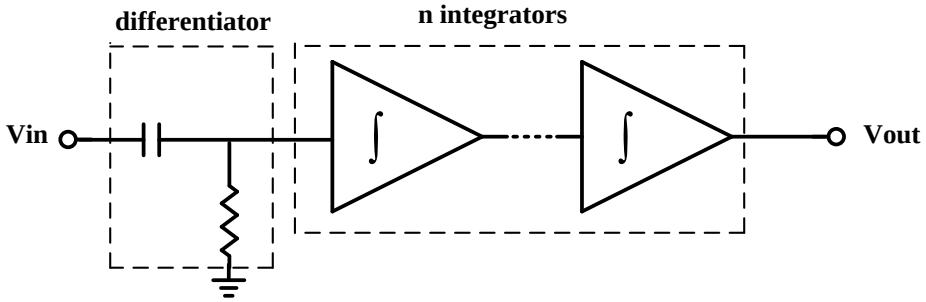


Figure 3.1: The block diagram of a Semi-Gaussian pulse shaper.

that the flicker noise is independent of the device bias current and the noise spectral power density is inversely proportional to the frequency (i.e., $\alpha_{fs} = 1$). Contrary, recent studies show that the value of K_{fs} can be bias dependent [143] and the value of α_{fs} is not exactly equal to 1.

3.1.2 Pulse Shaper Analysis

Pulse shapers play an important role in the overall noise performance of the readout system. Understanding the behaviour of pulse shapers is essential when designing a low-noise readout system is concerned. Let's first consider a simple $CR-RC$ filter. This pulse shaper is basically a CR high-pass filter (a differentiator) followed by an RC low-pass one (an integrator). The integrator limits the bandwidth of the signal and the differentiator sets the desired decay time. The readout systems that use $CR-RC$ pulse shapers cannot operate at high counting rates. This is due to the fact that the output of the filter returns to the baseline slowly preventing high counting rates. The problem can be avoided by passing the signal through additional integrators which makes the output pulses more symmetrical. The resulting filter is called a Semi-Gaussian $CR-(RC)^n$ pulse shaper. Its block diagram is shown in Figure 3.1. Better signal-to-noise characteristic is another advantage of SG over $CR-RC$ pulse shapers [22].

The transfer function of an SG pulse shaper consisting of one differentiator followed by n integrators is

$$H(s) = \frac{s\,\tau_d}{1+s\,\tau_d} \times \left(\frac{A_{SH}}{1+s\,\tau_i}\right)^n, \tag{3.3}$$

where τ_d and τ_i are the time constants of the differentiator and integrators respectively. A_{SH} is the DC gain of the integrators and n is the order of the shaper. The peaking time defined by $\tau_s = n\,\tau_i$ is the time that the output of the shaper reaches the peak amplitude. τ_s is an important design parameter as it affects the noise bandwidth. It is very common to choose $\tau_d = \tau_i = \tau$ in SG pulse shapers which reduces the transfer function to

$$H(s) = \frac{(A_{SH})^n\, s\,\tau}{(1+s\,\tau)^{n+1}}. \tag{3.4}$$

In time domain, the output signal due to one electron charge delivered by the detector can be simply calculated as [71]

$$V_o(t) = L^{-1}\left\{\frac{q}{sC_f}H(s)\right\} = \frac{qA^n n^n}{C_f\, n!}(\frac{t}{t_s})^n e^{(-\frac{nt}{\tau_s})}, \tag{3.5}$$

where q corresponds to one electron charge (i.e., $q = 1.6\times10^{-19}$ C). The peak amplitude of the signal equals to

$$V_{o,max} = V_o(t=\tau_s) = \frac{qA^n n^n}{C_f\, n!\, e^n}. \tag{3.6}$$

3.2 Derivation of Equivalent Noise Charge (ENC) Equations

The noise of a detector readout system is usually expressed as the equivalent noise charge or ENC. The ENC is defined by the ratio of rms noise at the output of the pulse shaper to the signal amplitude due to one electron charge [71]. In other words, ENC is the number of input charges for which the signal-to-noise ratio at the output of the pulse shaper equals one. Although ENC is a convenient measure of system noise, it is not a primary quantity. In fact ENC is derived from contributions of the voltage and current noise sources of the system. ENC is often expressed in terms of units of electric charge (i.e., $q = 1.6\times10^{-19}$ C) or in fC. Mathematically, ENC can be expressed as

$$ENC = \sqrt{\frac{V^2_{no,tot}}{V^2_{o,max}}}, \tag{3.7}$$

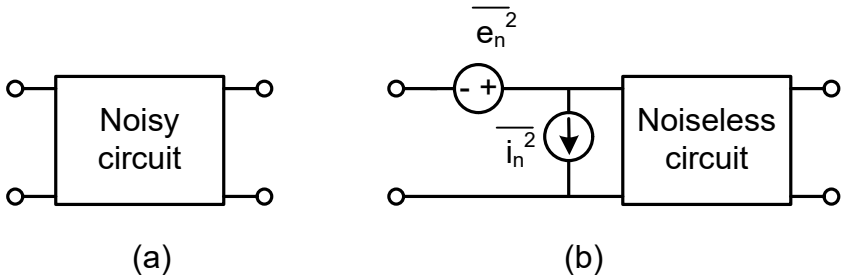


Figure 3.2: (a) Model of a noisy two-port network, and (b) model of the network with the noise sources referred to the input.

where $V_{no,tot}^2$ is the total integrated noise power at the output of the pulse shaper, and $V_{o,max}$ is the peak amplitude of the output signal due to one-electron charge. The ENC depends on the characteristics of both the CSA and the pulse shaper.

For the purpose of noise analysis, we first need to model the noise of the readout system. The noise of any two-port network can be modelled by equivalent voltage (series) and current (parallel) noise sources, typically referred to the input ports of the network [144]. These noise sources are illustrated in Figure 3.2. In a well-designed front-end circuit, the noise of the system is dominated by the noise of the input MOS device of the CSA. The series and parallel noise power spectral densities are uncorrelated [71] and therefore, the total equivalent noise charge of the readout circuit can be calculated by the sum of the individual ENC contributions.

The power spectral densities of the readout circuit can be expressed by the following equations

$$\frac{d\overline{e_n^2}}{df} = S_{w,ser} + S_{f,ser}, \tag{3.8}$$

$$\frac{d\overline{i_n^2}}{df} = S_{w,par} + S_{f,par}. \tag{3.9}$$

where the first term in each equation contains frequency independent (white-like) and the second term frequency dependent portion of the noise power spectral densities. The series and parallel power spectral densities are uncorrelated and therefore

the total noise power spectrum at the output of the CSA can be expressed as

$$V_{no,CSA}^2 = \left|\frac{C_{det}+C_f+C_{in}}{C_f}\right|^2 e_n^2 + \left|\frac{1}{sC_f}\right|^2 i_n^2$$
$$= \left|\frac{C_{tot}}{C_f}\right|^2 e_n^2 + \left|\frac{1}{sC_f}\right|^2 i_n^2, \tag{3.10}$$

where C_{det} is the detector capacitance, and C_{in} is the input capacitance of the input device of the CSA. C_{in} can be extracted from SPICE simulations.

The total integrated rms noise at the output of the pulse shaper can be calculated using the following equation

$$V_{no,tot}^2 = \int_0^\infty |V_{no,CSA}|^2 \times |H(j2\pi f)|^2 df. \tag{3.11}$$

The ENCs of the readout system can now be calculated by substituting (3.6) and (3.11) into (3.7). Since the power spectral densities in equations (3.8) and (3.9) are totally uncorrelated, it is more convenient to deal with them separately.

3.2.1 Power Spectral Density of the Equivalent Voltage Noise Source

The series white noise voltage spectrum can be expressed by the following equation

$$S_{w,ser} = \Gamma \frac{4k_B T}{g_m}, \tag{3.12}$$

where Γ is the coefficient of the channel thermal noise, T is the absolute temperature, k_B is the Boltzmann's constant, and g_m is the transconductance of the input device of the CSA. The value of Γ depends on the region of operation of the device and can be described by the following equation which is valid for all inversion regions of MOS devices [82]

$$\Gamma = \alpha_w n_{sub} \gamma. \tag{3.13}$$

In this equation α_w is the thermal noise excess factor, n_{sub} is the sub-threshold slope factor, and γ the thermal noise coefficient. The value of the coefficient γ varies from $1/2$ in weak inversion to $2/3$ in strong inversion [82]. By substituting (3.12) into (3.10) and (3.11) and taking the integral, the total integrated rms thermal

noise at the output of the shaper can be obtained as

$$V_{n,w,ser}^2 = \alpha_w n_{sub} \gamma \frac{4k_B T}{g_m} \left(\frac{C_{tot}}{C_f}\right)^2 \times \left(\frac{(A_{SH})^{2n} B(3/2, n-1/2)\, n}{4\pi\, \tau_s}\right), \tag{3.14}$$

where n is the order of the pulse shaper. $B(x,y)$ represents the Beta function and is defined by

$$B(x,y) = \int_0^1 \frac{t^{x-1}}{(1-t)^{1-y}} dt = \int_0^\infty \frac{t^{x-1}}{(1+t)^{x+y}} dt. \tag{3.15}$$

The value of $B(x,y)$ can be obtained using the *beta* function in MATLAB®.

The ENC of the system due to thermal noise can be calculated by substituting (3.14) and (3.6) into (3.7) and is given by

$$ENC_{w,ser}^2 = \alpha_w n_{sub} \frac{4K_B T}{g_m} \times \left(\frac{(n!)^2 e^{2n}}{n^{2n}}\right) \times \left(\frac{C_{tot}^2 (A_{SH})^{2n} B(3/2, n-1/2)\, n}{q^2\, \tau_s}\right). \tag{3.16}$$

This general expression for the series white noise is valid for all regions of operation of the CSA input device.

The series flicker noise voltage spectrum can be expressed by the following equation [143]

$$S_{f,ser} = \frac{K_{fs}}{f^{\alpha_{fs}} C_{ox} W L}, \tag{3.17}$$

where K_{fs} is the intrinsic process parameter. Experimental data for MOS devices in submicron technologies shows that the parameter K_{fs} can be bias dependent [143]. The corresponding $ENC_{f,ser}$ due to series flicker noise is given by the following equation

$$ENC_{f,ser}^2 = \frac{K_{fs} C_{tot}^2}{2 q^2 C_{ox} W L} \times \left(\frac{(n!)^2 e^{2n}}{n^{2n}}\right) \times (2\pi\tau_0)^{\alpha_{fs}-1} \times B\left(\frac{3-\alpha_{fs}}{2}, n + \frac{\alpha_{fs}-1}{2}\right). \tag{3.18}$$

3.2.2 Power Spectral Density of the Equivalent Current Noise Source

The reduction of the oxide thickness with the scaling of CMOS technology has increased contributions of a few noise sources that otherwise could have been neglected without significantly affecting the overall noise performance of the system. When implemented in advanced CMOS processes, a major noise source that needs to be taken into account is the gate leakage current of the input device of the CSA. This leakage current is mainly due to the tunnelling phenomena. Gate-to-inverted channel current (I_{GC}) and the parasitic current through gate-to-source or gate-to-drain extension overlap region (I_{GS} or I_{GD}) are the main components contributing to the gate leakage current [143]. A combination of white-type and quasi $1/f$ noise behaviour is generally used to model the noise associated with the gate leakage current.

The frequency independent (white-like) noise contributions in the device gate leakage current can be modelled by the following equation [79]

$$S_{w,par} = 2q(|I_{GC}| + |I_{GS}| + |I_{GD}|) = 2qI_0, \tag{3.19}$$

where I_0 is the total gate leakage current. The $ENC_{w,par}$ is obtained by evaluating (3.7) using (3.19) and (3.6) and is given by

$$ENC^2_{w,par} = 2qI_0 \frac{\tau_s}{q^2 4\pi n} \left(\frac{(n!)^2 e^{2n}}{n^{2n}} \right) \times \quad B(\frac{1}{2}, n+\frac{1}{2}). \tag{3.20}$$

Please note that (3.20) can also be used to calculate the ENC of the system due to the leakage current of the detector.

The frequency dependent noise contribution in the gate leakage current is modelled by the following equation [79]

$$S_{f,par} = \frac{K_{fp}}{f^{\alpha_{fp}}} \times \left[\frac{I^2_{GC}}{W(L-2\Delta L)} + \frac{I^2_{GS} + I^2_{GD}}{W\Delta L} \right] = \frac{K'}{f^{\alpha_{fp}}}, \tag{3.21}$$

where K_{fp} is the intrinsic parallel flicker noise coefficient, W is the device width, L is the channel length, and ΔL is the gate-to-source/drain overlap length. The $ENC_{f,par}$ of the system due to parallel flicker noise is given by the following equa-

tion

$$ENC_{f,par}^2 = \left(\frac{K'(\tau_0)^2}{2q^2(2\pi\tau_0)^{1-\alpha_{fp}}}\right)\left(\frac{(n!)^2 e^{2n}}{n^{2n}}\right) \times B(\frac{1-\alpha_{fp}}{2}, n+\frac{1+\alpha_{fp}}{2}). \quad (3.22)$$

The total equivalent noise charge of the readout circuit is given by the sum of the individual ENC contributions

$$ENC_{tot}^2 = ENC_{w,ser}^2 + ENC_{f,ser}^2 + ENC_{w,par}^2 + ENC_{f,par}^2. \quad (3.23)$$

Optimal design of the readout system is achieved by minimizing (3.23) with respect to the design parameters of the CSA and pulse shaper simultaneously. In the following section we discuss the effects of the parameters of the shaper on the overall noise of the system.

3.2.3 Pulse Shaper's Parameters

The transfer function of a SG pulse shaper is characterized by three parameters but only two of them appear in the ENC equations: the shaping time (τ_s) and the number of integrators (n). In order to obtain insight into the effects of shaper's parameters on the overall noise of the readout system, we evaluate noise of a typical detector readout circuit in a 0.13 μm CMOS process. Let us assume that a detector with 0.5 pF capacitance is read out by a CSA and a SG pulse shaper. The input transistor of the CSA is an NMOS device with $W/L = 41\mu m/0.2\mu$m and draws I_{DS} =10 μA. The feedback capacitance is assumed to be 20 fF. Figure 3.3 shows the ENC_{tot} of the readout circuit in a 0.13 μm CMOS process as a function of peaking time and order of the pulse shaper. Gate current noise data are taken from [79]. As expected, for a fixed order n and for short peaking times, the ENC_{tot} gradually decreases when shaping time increases. However, at large peaking times the gate leakage current slightly increases the noise of the readout circuit. So the noise due to gate leakage current can be safely neglected in this technology without significantly affecting the overall noise performance of the system. Similarly, for a fixed peaking time, the ENC_{tot} decreases when the number of integrators (n)

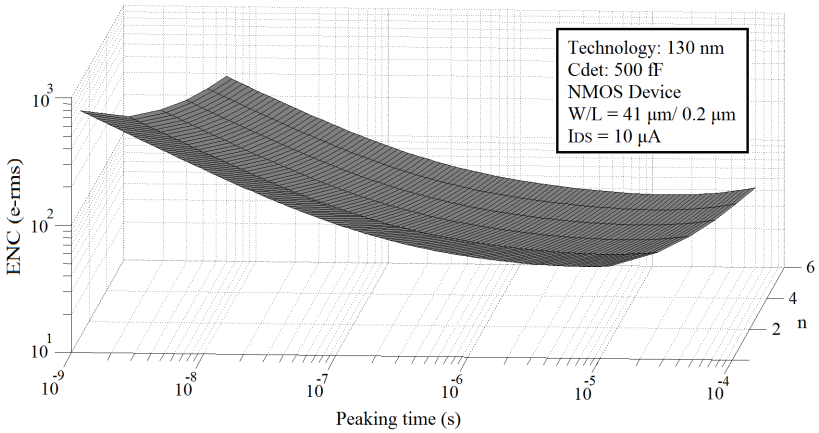


Figure 3.3: Effect of shaping time and order of the shaper on the ENCs of a detector readout system in a 0.13 μm CMOS process.

increases. Please note that the shot noise due to the dark current of the detector is not taken into account in this analysis. This noise source, modelled with a parallel noise current, gradually gives rise to the ENC_{tot} after a range of peaking times.

3.2.4 Process Scaling

In order to see the effects of process scaling, ENC_{tot} of the same readout circuit is calculated in a 90 nm CMOS process. The result is shown in Figure 3.4. Comparing the ENCs plotted in Figure 3.3 and Figure 3.4 shows that in deep submicron technologies the noise due to the gate leakage current cannot be neglected especially at large peaking times. The gate leakage current in a 90 nm process is about 2-3 orders of magnitude larger than in a 0.13 μm process [79]. Moreover, in deep submicron processes the gate leakage current is strongly dependent on the drain-to-source voltage of the input MOS device when the device is biased in weak or moderate inversion regions [79, 145]. This noise analysis confirms that the parallel noise sources must be accurately modelled when improving the resolution of readout system implemented in an advanced CMOS process is concerned.

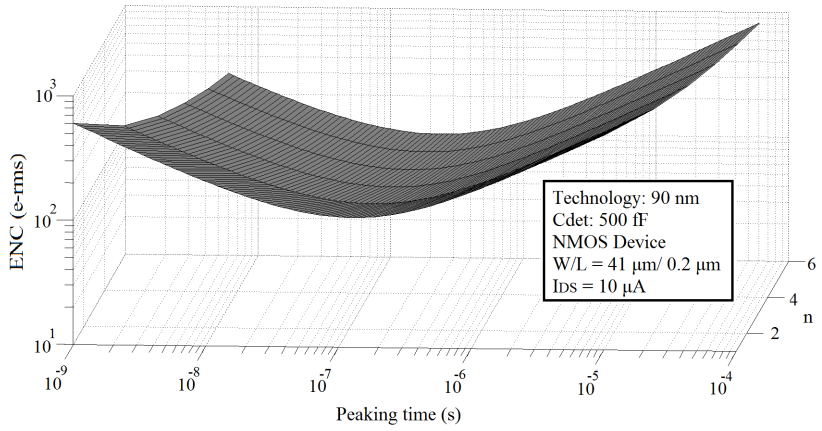


Figure 3.4: Effect of shaping time and order of the shaper on ENCs of a detector readout system in a 90 nm CMOS process.

3.3 Measurement of Noise of the Readout System

As explained earlier in Section 3.2, the ENC is defined by the ratio of rms noise at the output of the pulse shaper to the output signal amplitude due to one electron charge [71]. In practice, it is not possible to inject one electron charge into the circuit and measure the corresponding output peak amplitude. This means that it is essential to inject a practical amount of charge to be able to determine the ENC of the system. To account for this practical limitation, equation (3.7) can be rewritten as

$$ENC = Q_{sig}/(S/N) = (V_{no}/V_{sig})Q_{sig}, \tag{3.24}$$

where Q_{sig} is the input signal charge, and V_{sig} and V_{no} are the output signal pulse height and output noise respectively. These three parameters must be carefully measured in order to calculate the noise of the system. To do this, a known step-like signal (V_{Test}) is applied to an integrated test capacitance (C_{Test}) and the relevant output parameters of the pulse shaper are measured. In this situation, the input charge is known (i.e., $Q_{sig} = V_{Test}C_{Test}$) and the other two parameters need to be measured by a proper instrument.

The easiest method to calculate the ENC of the readout system is to use a mul-

tichannel pulse height analyzer. A multichannel analyzer (MCA) is an instrument that measures the pulse height spectrum. The output of the MCA is usually sent to a computer for analysis, display, or storage. An MCA usually consists of a discriminator, an analog-to-digital converter (ADC), a memory, and a display. When the amplitude of the incoming pulses is higher than a threshold, the pulse is captured for further processing. The ADC only digitizes the maximum height of the pulse and the digitized value is stored in a memory. The MCA only accepts another pulse once the processing of the current pulse is finished. By counting the number of pulses of each height over a period of time we can plot the energy spectrum of the electromagnetic wave. The peak centroid shows the magnitude of the signal and the width of the peak represents the noise. The equivalent noise charge of the readout system can be calculated using

$$FWHM = 2.35 \times Q_n, \tag{3.25}$$

where FWHM is the full width of the peak at half its maximum height and Q_n is the equivalent rms noise charge.

Since multichannel analyzers are highly specialized instruments, they may not be available for use at every research laboratory. Another method exists to calculate the ENC of the readout system and it uses a spectrum anlayzer [146] or a voltmeter and an oscilloscope. The signal pulse height can be easily measured using an oscilloscope. The noise level can be determined from a spectrum analyzer or a voltmeter. The measured values can then be substituted into (3.24) to calculate the equivalent noise charge of the system.

If a voltmeter is used to measure the noise, it must have enough bandwidth and adequate sensitivity. Most of the voltmeters in the market measure the peak amplitude of the signal and display it in rms. This conversion is valid for only sinusoidal signals. A voltmeter that measures true rms of the signal must be used for the purpose of measuring the noise of the system. Such a voltmeter uses a thermal sensor or alternatively squares the signal and calculates the square root. The bandwidth of the voltmeter must also be sufficiently higher than that of the readout system.

If a spectrum analyzer is used to measure the noise of the system, it must also be

able to measure the true rms value of the signal. The spectrum analyzer measures the magnitude of the signal versus frequency. It is important to choose a proper value for the resolution bandwidth of the instrument as the measured noise level strongly depends on it. It is possible to find instruments in the market that measure spectrum of the signal in terms of $V/\sqrt{Hz}$. The total noise of the system is then calculated using [87]

$$V_{no} = \sqrt{\sum_{k=0}^{N} [v_{no}^2(k).\triangle f]}, \tag{3.26}$$

where N is the number of frequency bins, and $\triangle f$ is the size of the frequency bin. The measurement can be repeated with the chip turned off, to get the background noise generated by the measurement system. The background noise is then subtracted in quadrature to get the noise of the readout system [147].

Chapter 4

Analysis and Design of a Novel Low-Power Charge-Sensitive Amplifier

4.1 Introduction

Solid-state radiation detectors produce a small amount of charge that needs to be amplified by charge-sensitive amplifiers (CSAs). An important feature of CSAs is the robustness of their charge gain to detector capacitance variations [22]. Noise performance, gain (and linearity), and power consumption are the key parameters that pose several trade-offs in the design of CSAs. In order to improve the resolution of detection, the noise of the system needs to be reduced. The noise of the readout circuit is mostly due to the noise of the CSA and thus designing a low-noise CSA is of paramount importance [148]. The noise performance of the CSA can be enhanced at the expense of increasing its power consumption which is in contrast with the low-power requirement of modern readout circuits. Besides, increasing the power consumption of the circuit generates extra heat which in turn may deteriorate the performance of the detector and ultimately limit the resolution of detection. Furthermore, charge amplifiers are usually implemented using single-ended configurations to save power. Thus their gain is usually low, and is

improved at the expense of increasing the power consumption which is undesirable. Also, they do not usually process signals of both polarities. We address these issues by introducing an improved CSA. The proposed CSA is then used in a readout circuit. Measurement results of the front-end circuit confirm the operation of the circuit. In the following section, we present the design of the proposed low-power continuous-reset CMOS CSA.

4.2 The Proposed Charge-Sensitive Amplifier

The discussion on the gain of the CSA in Chapter 1 is based on the assumption that the gain of the inverting amplifier is sufficiently large. The large gain of the amplifier significantly increases the value of the reflected capacitance at the input terminal of the amplifier (due to the Miller effect on the feedback capacitor). This in part facilitate the desired property that the charge gain of the CSA would become robust to the detector capacitance variations. The increase in the gain of the amplifier is often achieved by both employing a folded-cascode architecture in the design of the CSA and by increasing the transconductance of the input transistor of the CSA. The latter results in an increase in the overall power consumption of the CSA.

The proposed low-power continuous-reset CMOS CSA is shown in Figure 4.1. A regulated folded-cascode stage and a source follower buffer are used in the design of the CSA. A gain-boosting technique [144] is employed in both upper and lower branches of the cascode stage in order to enhance the overall gain of the amplifier with negligible overhead power consumption. In the schematic shown in Figure 4.1, device MN4 (MP4) helps to increase the output impedance of the lower (upper) cascode branch by regulating the voltage across the device MN3 (MP3). The cascode current source consisting of MP5 and MP6 (MN5 and MN6) provides a 0.5 μA bias current to transistor MN4 (MP4). A 97 fF compensation capacitor (C_c) is placed between the source terminal of MP7 and the drain terminals of MN2 and MP2 for stability purposes.

The input device of the CSA is chosen to be a PMOS device since it generates a lower flicker noise as compared to an n-type MOS device [149]. It is biased in the middle of the moderate inversion region with an inversion coefficient approxi-

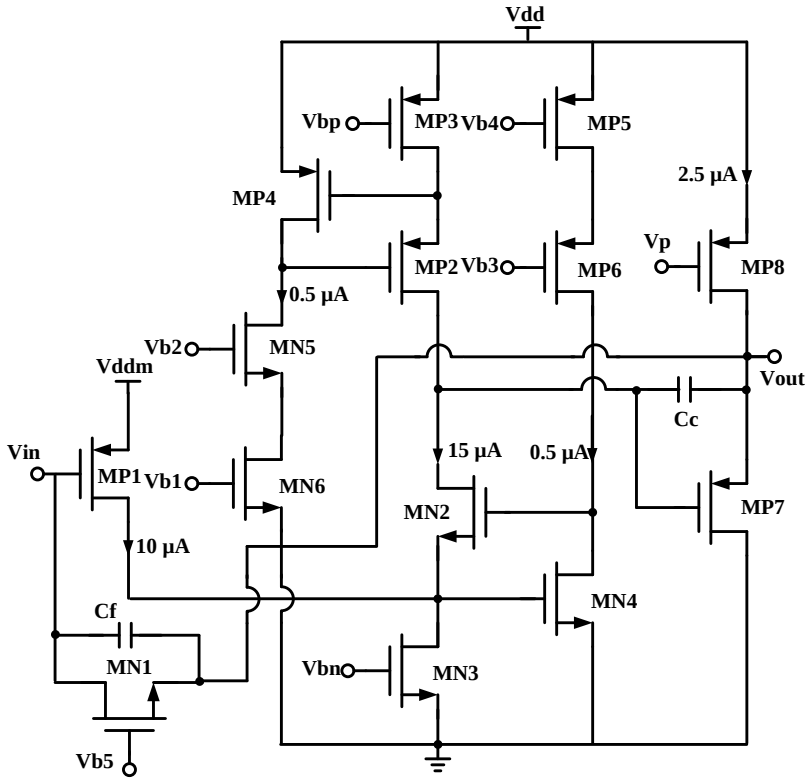


Figure 4.1: The proposed low-power continuous-reset CMOS charge-sensitive amplifier.

mately equal to 1 [82]. This is to achieve a satisfactory trade-off between linearity, dynamic range, and speed while keeping the power consumption at a reasonably low level. The gate length of the input transistor is chosen to be 0.25 μm which is $\sim 2\times$ larger than the minimum feature size in the process used. As the input device is biased at relatively high current levels, to further decrease the power consumption of the amplifier, the source terminal of the input device is connected to *Vddm*, a supply voltage lower than *Vdd*.

The value of the feedback capacitor of the CSA is chosen to be 100 fF which results in a theoretical gain of 10 mV/fC. An integrated high-value DC feedback resistor discharges the capacitor continuously. The resistor is implemented by an n-type MOS device (MN1) biased in weak inversion region and provides a DC

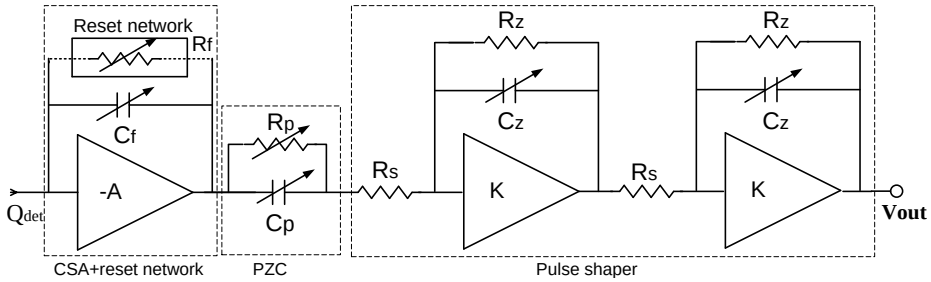


Figure 4.2: Block diagram of the readout circuit employing the proposed CSA, a PZC, and a 2^{nd}-order Semi-Gaussian programmable pulse shaper.

path for the leakage current of the detector. Other reset mechanisms may be used depending on the desired linearity and the amount of leakage current that needs to be compensated. Please refer to Section 2.4.2 for the pros and cons of the most frequently used reset networks.

In order to validate the operation of the proposed CSA, it is employed in a front-end circuit that is optimized for the readout of CZT detectors. The circuit consists of the proposed CSA, a pole-zero cancellation circuit, and a second-order semi-Gaussian programmable pulse shaper. Its block diagram is shown in Figure 4.2. The required bias voltages/currents are generated on chip using an external reference current. Analytical noise analysis of the readout circuit is given in the following section.

4.3 Noise Analysis of the Readout Circuit

It can be shown that if $R_z \times C_z = R_s \times C_p$ and $R_s \ll R_p$ are met, then the transfer function of the cascade of the pulse shaper and the PZC circuit can be written as

$$H(s) = \frac{V_{out}(s)}{V_{out,CSA}(s)} = \frac{R_z}{R_p}\frac{R_z}{R_s}\frac{1+R_pC_ps}{(1+st_p)^3}, \tag{4.1}$$

where, $t_p = R_z C_z$. If $R_f C_f = R_p C_p$, then pole-cancellation occurs and the output voltage due to one electron charge (q) can be written as

$$V_{out}(t) = \frac{q}{2C_f}\left(\frac{C_p}{C_z}\right)^2\left(\frac{t}{t_p}\right)^2 e^{-\frac{t}{t_p}}. \tag{4.2}$$

The peak amplitude of the signal occurs at $t = 2t_p$ and equals to

$$V_{o,max} = |V_{out}(t = 2t_p)| = \frac{2q}{C_f}\left(\frac{C_p}{C_z}\right)^2 e^{-2}. \tag{4.3}$$

Note that the peak amplitude due to one electron charge depends only on the value and/or ratio of capacitors which are well-controlled values. Following the procedure described in Chapter 3, the noise equations of the readout circuit can be derived analytically. The ENC contribution due to the series white noise equals to

$$ENC_{w,ser}^2 = \Gamma\frac{4k_B T}{g_m}\frac{C_{tot}^2}{16\pi q^2 e^{-4} t_p}\left|B\left(\frac{3}{2},\frac{3}{2}\right)\right|, \tag{4.4}$$

where Γ is the coefficient of the channel thermal noise, C_{tot} is the total capacitance that shunts the amplifier input, T is the absolute temperature, k_B is the Boltzmann's constant, g_m is the transconductance of the input devices of the CSA, and B is the Beta function [71]. The ENC contribution due to series frequency-dependent noise can be written as

$$ENC_{f,ser}^2 = \frac{K_{fs}}{WLC_{ox}}\frac{C_{tot}^2}{8q^2 e^{-4}(2\pi t_p)^{1-\alpha_{fs}}}\times \left|B\left(\frac{3-\alpha_{fs}}{2},\frac{3+\alpha_{fs}}{2}\right)\right|, \tag{4.5}$$

where, K_{fs} is an intrinsic process parameter, C_{ox} is the gate oxide capacitance per unit area, and α_{fs} is the fitting exponent of f for the flicker noise equation, and W and L are the width and length of the input device of the CSA, respectively. The ENC contribution due to the parallel white noise equals to

$$ENC_{w,par}^2 = 2qI_0\frac{t_p}{16\pi q^2 e^{-4}}\left|B\left(\frac{1}{2},\frac{5}{2}\right)\right|, \tag{4.6}$$

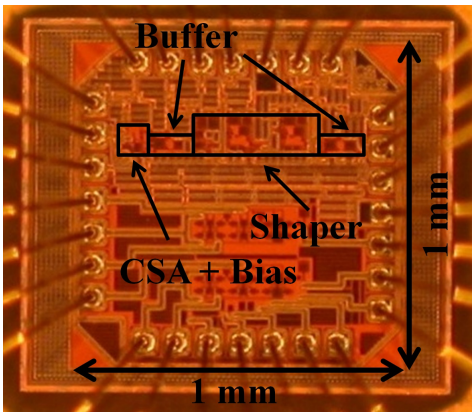


Figure 4.3: Chip micrograph. The chip is packaged in a standard 44-pin CQFP.

where, I_0 is the sum of the input devices gate currents, the detector leakage current and its associated bias network. The total ENC of the readout circuit is the sum of the individual ENC contributions.

4.4 Experimental Results

The readout circuit is fabricated in a 0.13-μm CMOS process. Fig. 4.3 shows a micrograph of the chip that is packaged in a standard 44-pin ceramic quad flat package (CQFP). The main building blocks of the readout channel are marked on the figure. To evaluate the functionality of the readout circuit, a 0.5 pF test capacitance is also integrated on chip. A controlled amount of charge can be injected into the circuit by applying an external step signal to the test capacitor. The capacitance of the detector is modelled by integrating a 0.5 pF capacitance in parallel with the input terminal of the CSA. Figure 4.4 shows the signals at the output terminals of the CSA and pulse shaper for an injected charge of about $\pm$2.5 fC. According to this figure, the CSA and the pulse shaper can accept signals of both polarities. The long discharge time constant of the CSA allows for shaping times in the order of μs. The measured shaping time is about $1\mu s$.

Figure 4.5 shows the voltage peak amplitude at the output of the CSA (upper curve) and the pulse shaper (lower curve) versus injected charge. Based on this fig-

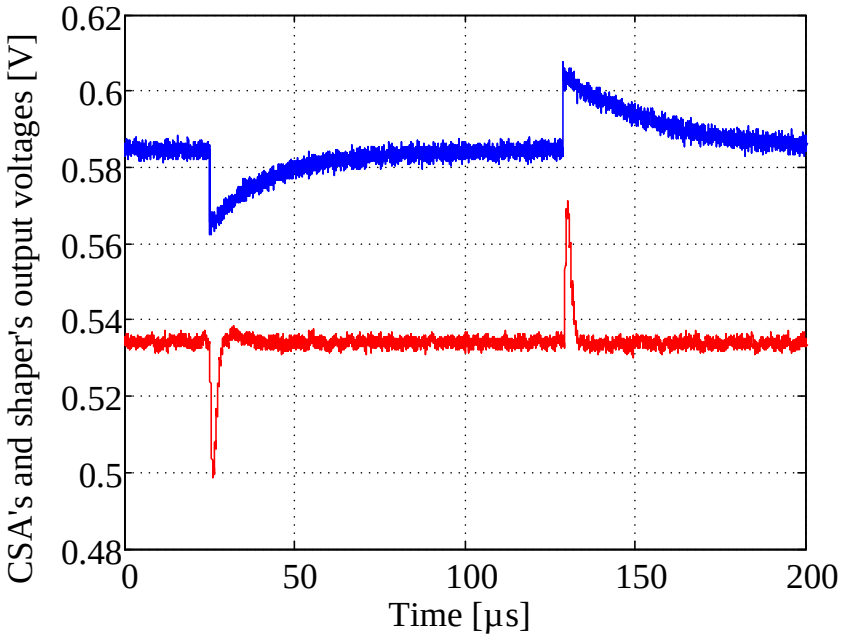


Figure 4.4: Measured waveforms at the output of the CSA (upper) and the pulse shaper (lower) for an injected charge of about ± 2.5 fC.

ure, the conversion gains of the CSA and the shaper are about 8.8 and 13.9 mV/fC, respectively. The measured gain for the CSA is in good agreement with the theoretical value when the effects of the parasitic capacitances as well as the detector capacitance are taken into account. The charge integration at the output of the CSA is linear from about -9 to 6 fC. The gain linearity can be improved by biasing the input device of the CSA more into the strong inversion region.

The noise performance of the readout circuit is also evaluated. The noise measurement is done in a shielded chamber. Agilent PXA N9030A with a frequency range of 3 Hz to 26.5 GHz is used to measure the output voltage noise density. The input impedance of the instrument is derived by HP 1144 Active Probe. Figure 4.6 shows the measured total output voltage noise density of the integrated readout circuit. The measurement includes the noise of the active probe, power supplies and the instrument. To calculate the noise of the readout circuit, the noise of the measurement system must be excluded. Figure 4.7 shows the measured voltage noise density of the probe, power supplies, and the instrument. The equivalent noise

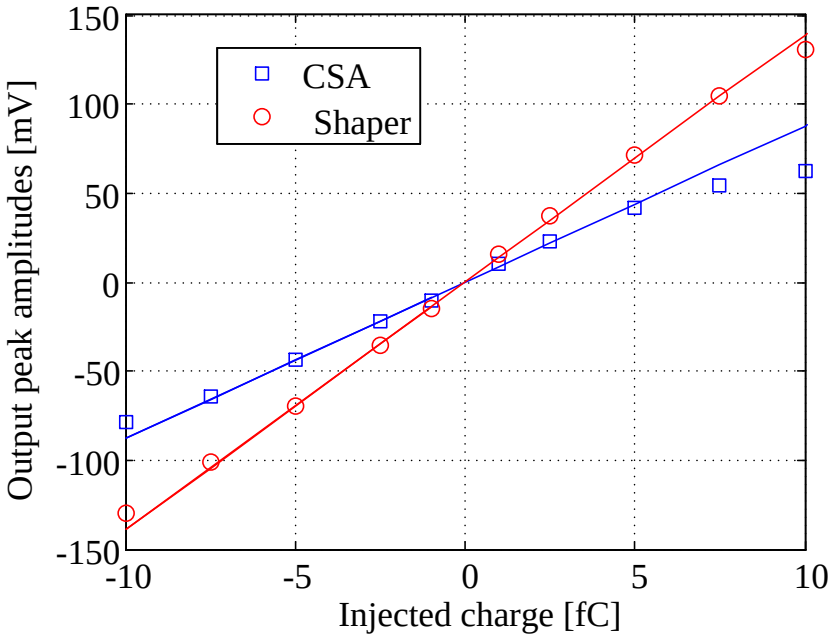


Figure 4.5: Measured voltage peak amplitudes at the outputs of the CSA and the shaper versus injected charge.

charge of the readout circuit can be calculated by subtracting the noise of the measurement system in quadrature [147]. The measured ENC of the readout circuit is about 111 $\bar{e}$-rms. The CSA consumes 37.5 μW of power from power supplies of $Vdd = 1.2V$ and $Vddm = 0.9V$ and occupies 0.0021 mm^2 of silicon area. Table 4.1 compares the performance of the designed readout circuit with similar work in the literature.

4.5 Summary and Conclusions

In this chapter, the design of a novel low-power continuous-reset CMOS charge-sensitive amplifier is presented. The proposed CSA is intended for capacitive sensor readout circuits, in particular, interface circuits for solid-state detectors used in medical imaging and X-ray spectroscopy. A proof-of-concept interface circuit is designed and fabricated in a 0.13-μm CMOS process and consists of the proposed CSA, a pole-zero cancellation circuit, and a second-order semi-Gaussian

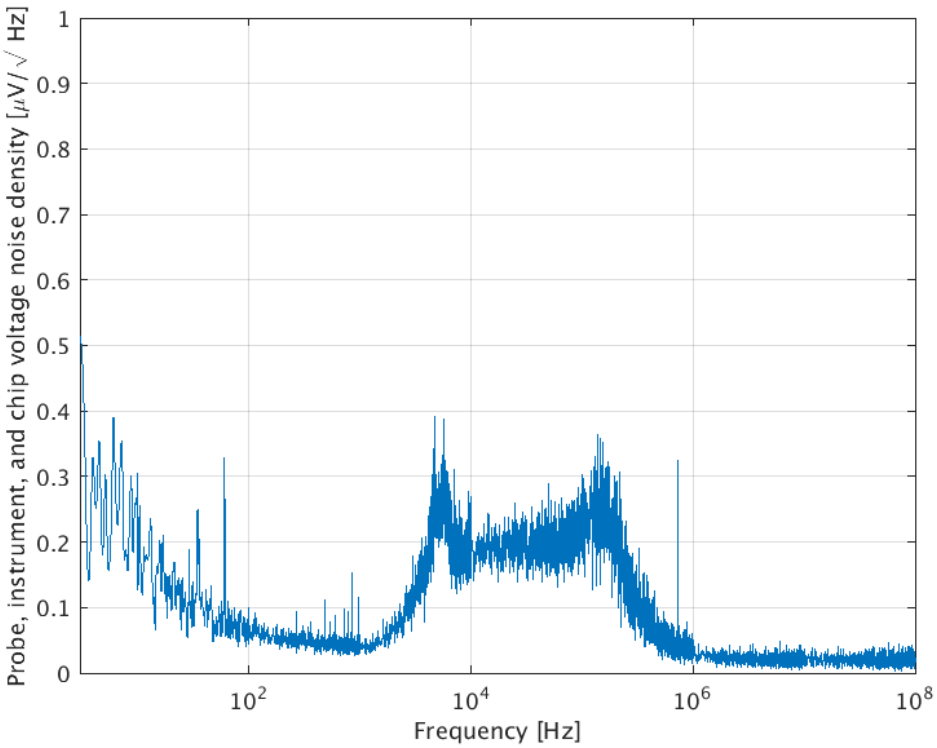


Figure 4.6: Measured total output voltage noise density of the integrated readout circuit. The measurement includes the noise of the active probe and the instrument.

programmable pulse shaper. Measurement results show that the conversion gains of the CSA and the pulse shaper are about 8.8 and 13.9 mV/fC, respectively. The CSA can accept signals of both polarities and the charge integration is linear from about -9 to 6 fC. The measured equivalent noise charge of the CSA is about 111 $\bar{e}$-rms. The CSA occupies 0.0021 mm^2 of silicon area and consumes 37.5 μW from dual supply voltages of 0.9 and 1.2 V.

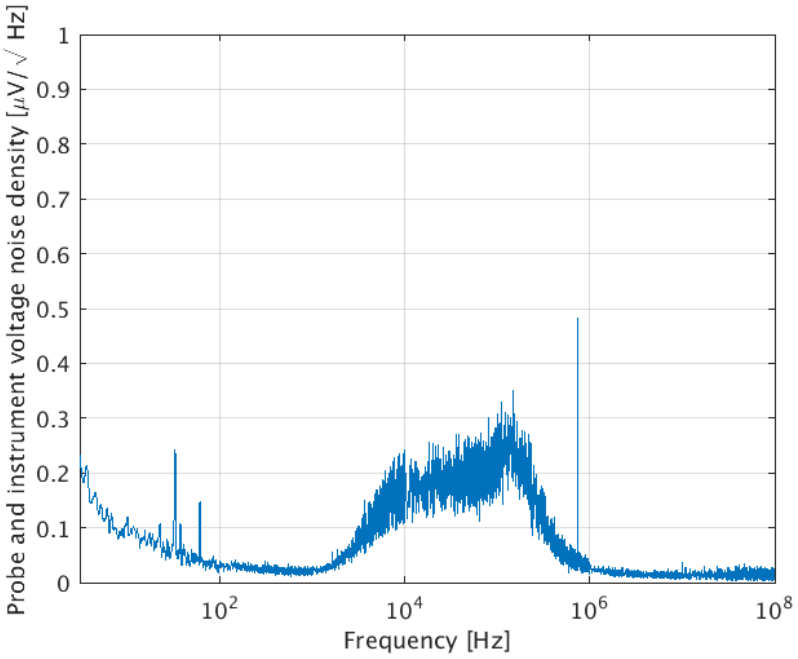


Figure 4.7: Measured voltage noise density of the active probe and the instrument.

Table 4.1: Readout circuit performance comparison

Specification	This work	[23]	[43]	[150]	[151]
CMOS technology	0.13 μm	0.13 μm	0.35 μm	0.35 μm	0.35 μm
Supply voltage (V)	0.9/1.2	1.5	2.2/3	3.3	3.3
Signal processing chain	CSA, PZC, 2^{nd}-order programmable shaper, buffer	CSA, 1^{st}-order shaper, discriminator	CSA, PZC, 2^{nd}-order shaper, discriminator, counter	CSA, 2^{nd}-order programmable shaper, buffer	CSA, 2^{nd}-order shaper, buffer
Charge polarity	Both	Both*	Single	Single	Single
Detector capacitance (pF)	$0.5-8$	–	$1-3$	$2-10$	$2-10$
Shaping time (μs)	$0.5-2$	0.3 (fixed)	0.16 (fixed)	$1-3$	1
Conversion gain	13.9 mV/fC	187.5 nA/fC	337 mV/fC	3.31 mV/fC	2.81 mV/fC (CSA)
ENC ($\bar{e}$-rms) $@C_{det}$	111 @$0.5pF$	105 @$0pF$	110 @$1pF$	382 @$2pF$	281 @$2pF$
CSA power cons.	37.5 μW	–	–	–	165 μW
Chip power cons.	171 μW core 312 μW buffer	16.2 μW analog – digital	4.2 mW core 0.8 mW discriminators	1000 μW	–

* using a polarity bit in the pulse shaper

Chapter 5

Design and Analysis of a 4-Channel Readout System for Solid-State Radiation Detectors

In this chapter the design and analysis of a low-power and low-noise 4-channel readout circuit intended for solid-state radiation detectors (in particular, CZT detectors) is presented. The design is optimized in terms of noise performance and power consumption. A comprehensive noise analysis of the readout system is presented. The analysis is based on the EKV model [82] of MOS transistors which is valid for all regions of operation. The readout circuit is laid out and fabricated in a standard 0.13-μm CMOS technology. Measurement results of the circuit are also presented.

5.1 Readout Circuit Design

The simplified block diagram of the implemented front-end circuit is shown in Figure 5.1. The circuit consists of a charge-sensitive amplifier (CSA), a reset network to provide a discharge path for the feedback capacitor, and a first-order pulse shaper with a pole-zero cancellation (PZC) circuit. All the bias voltages and currents in this figure are generated on chip using a single external reference bias current. The reset network also accommodates the leakage current of the detector and is a modi-

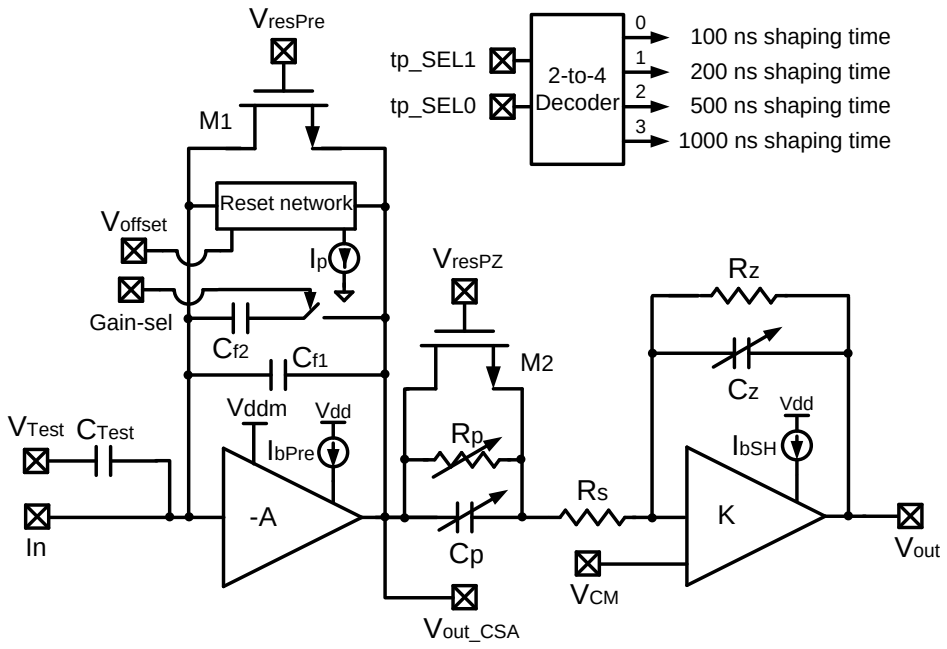


Figure 5.1: Simplified block diagram of one front-end channel. Capacitor banks are used to implement C_p and C_z. A 2-to-4 decoder is used to select the peaking time of the pulse shaper. Buffers/output drivers are not shown for simplicity.

fied version of Krummenacher's low-frequency feedback loop [12]. Output drivers (buffers) are not shown for simplicity. The design of buffers and amplifiers is discussed extensively in the literature [152–155] and thus we will not focus on such designs in this work. Capacitor banks are used in the design to allow adjusting the shaping time of the filter. The pulse shaper is designed to provide 100, 200, 500 and 1000 ns shaping times. The shaping time for each channel can be independently selected by using a 2-to-4 on-chip decoder. The circuit is capable of handling 0 to 5 fC and 5 to 45 fC injected charge. The corresponding conversion gain of the CSAs can be selected using the *Gain-sel* signal. A test capacitor is integrated on chip to enable precise charge injection for test purposes.

In Figure 5.1, transistor M_1 is used to change the effective DC feedback resis-

tance and accordingly the discharge time constant of the CSA. Improper pole cancellation may occur at the output of the pulse shaper as a result of adjustment of the value of the feedback resistance of the CSA or any mismatches or non-idealities in the fabricated resistors and capacitors. Therefore, either an under- or an over-compensated signal may occur at the output of the pulse shaper. The former will have an undershoot which is not completely eliminated and the latter will cause the output to decay to the baseline with the preamplifier time constant. To overcome these problems, we have introduced transistor M_2 in the PZC circuit which enables cancellation of the pole due to preamplifier's pulse decay time. The adjustment can be made by varying the bias voltage of M_2 such that the pulses at the output of the pulse shaper return to baseline in the minimum time with no undershoot. The detailed design of the main building blocks and a comprehensive noise analysis of the readout system will be presented in the following subsections.

5.1.1 Design of the Charge-Sensitive Amplifier

Charge-sensitive amplifiers are widely used in the design of readout circuits for various capacitive sensors, in particular, for solid-state radiation detectors. Insensitivity of their gain to the detector capacitance variations is the main motivation of using CSAs in the front-end circuit of such systems [22]. To maximize the achievable resolution, the noise of the readout circuit must be minimized. The noise of the overall system is typically dominated by the noise of the CSA. Furthermore, to minimize the length of the interconnect between the detector pixels and their corresponding CSA, which in turn minimizes the coupling and crosstalk noise, each CSA is typically placed as close as possible to its corresponding detector pixel. Due to this proximity low-power consumption of the CSA also becomes important as the excessive heat generated by the CSA would increase the noise of the system and also may deteriorate the performance of the detector. This is particularly important in high resolution systems with a large number of readout channels. Therefore, designing a low-noise low-power CSA is of paramount importance in such systems.

The circuit schematic of the proposed CSA is shown in Figure 5.2. A single-ended configuration is used in the design of the CSA to save power. In the CSA

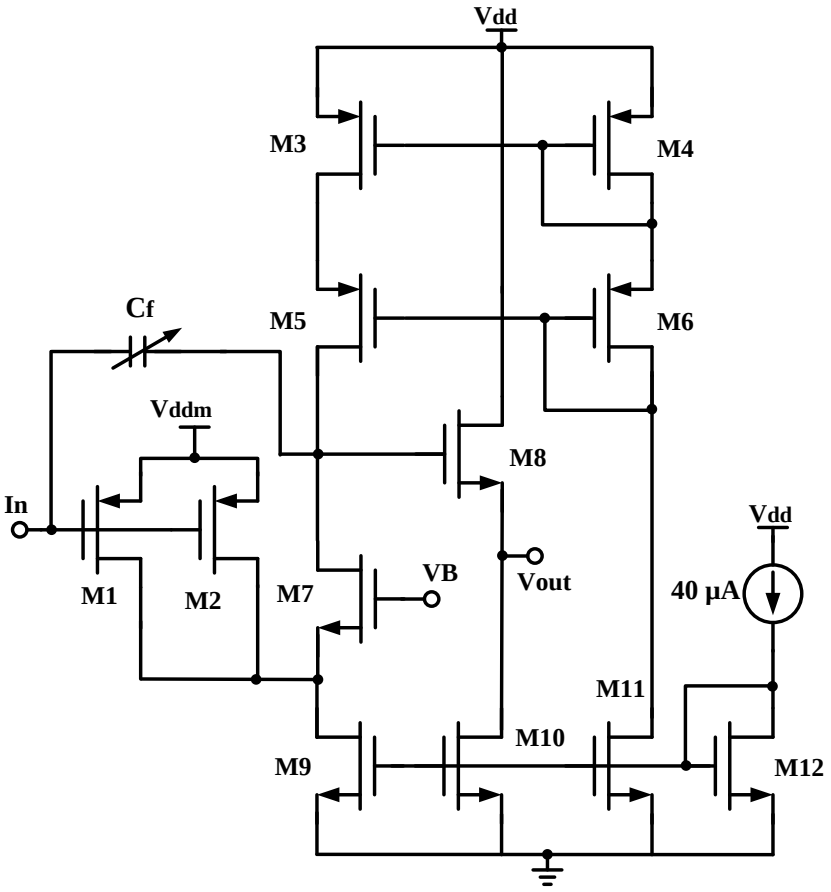


Figure 5.2: Circuit schematic of the CMOS charge-sensitive amplifier. Proper bias voltages and currents are supplied from an integrated bias circuitry.

design it is desired to increase the transconductance of the input device in order to improve both the speed and noise performance. This is achieved by using a folded-cascode topology. P-type MOS devices, i.e., M_1 and M_2, are chosen as the input devices of the CSA since they exhibit a lower flicker noise contribution as compared to n-type MOS devices [149]. Furthermore, the source terminals of the input devices are connect to $Vddm$, a supply voltage that can be made much lower than Vdd. This lower supply voltage will in turn results in a reduced power consumption of the CSA as the input devices are biased at high current level to increase

the speed and reduce the white noise. To reduce the flicker noise contribution and to improve the matching among different readout channels, the gate length of the input devices is chosen to be slightly larger than the minimum feature size. The feedback capacitor of the CSA is discharged through the reset network. The reset network also provides a DC path for the leakage current of the detector. The device dimensions of the CSA are given in Table 5.1.

Table 5.1: Device sizes of the CSA

M_1: 100/0.2	M_2: 100/0.2	M_3: 200/1	M_4: 200/1
M_5: 100/1	M_6: 100/1	M_7: 200/0.5	M_8: 200/1
M_9: 30/2.5	M_{10}: 10/2.5	M_{11}: 5/2.5	M_{12}: 10/2.5

All the dimensions are in μm.

5.1.2 Design of the Pulse Shaper with a PZC Circuit

In detector readout circuits, the output of the CSA is often passed through a filter before further signal processing, for example, for amplitude or peak-time measurements. Such filtering is referred to as pulse shaping as it affects the amplitude or timing of the resulting pulse signal. The most common pulse shaping method is to produce a pulse whose peak amplitude is proportional to the detected charge in the detector.

Since these filters are typically active structures, in this design, we use a first-order pulse shaper in order to minimize the power overhead of the active filter. The pulse shaper is designed to provide four different peaking times. The desired peaking time can be selected with a 2-to-4 decoder integrated on chip.

The decay of the charge amplifier pulses usually causes an undershoot in the pulse shaper output signal [22]. If another event occurs while the output signal is recovering, it will be superimposed on the undershoot and a pulse pile-up error will occur. For the large signals that overload the amplifier, the undershoot tail can last for a long time. To overcome these problems, a PZC circuit is placed between the CSA and the pulse shaper (See Figure 5.1). The PZC circuit must be carefully designed to properly cancel the pole associated with the decay of the CSA signal.

Referring to Figure 5.1, it can be shown that if $R_s \ll R_p$ and $R_z \times C_z = R_s \times C_p$,

Table 5.2: Device sizes of the main amplifier of the pulse shaper

M_1: 14/0.52	M_2: 14/0.52	M_3: 28/0.35	M_4: 28/0.35
M_5: 20/5	M_6: 40/5	M_7: 80/5	M_8: 110/0.35

All the dimensions are in μm.

then the transfer function of the cascade of the pulse shaper and the PZC circuit can be written as

$$H(s) = \frac{V_{out}(s)}{V_{out,CSA}(s)} = -\frac{R_z}{R_p}\frac{1+R_pC_ps}{(1+st_p)^2}, \tag{5.1}$$

where, t_p is the peaking time, defined as

$$t_p = R_zC_z = R_sC_p. \tag{5.2}$$

In time domain, the pulse shaper output signal due to one electron charge delivered by the detector can be derived as [71]

$$V_{out}(t) = L^{-1}\left\{(+q)\frac{R_f}{1+sR_fC_f}\frac{-R_z}{R_p}\frac{1+R_pC_ps}{(1+st_p)^2}\right\}, \tag{5.3}$$

where, q denotes the charge of one electron (i.e., $q = 1.6\times10^{-19}$ C), R_f is the effective feedback resistance of the CSA, and C_f is the total feedback capacitance. Pole cancellation occurs when $R_fC_f = R_pC_p$ and thus the output voltage can be written as

$$V_{out}(t) = \frac{-q}{C_f}\frac{C_p}{C_z}\frac{t}{t_p}e^{-\frac{t}{t_p}}. \tag{5.4}$$

The peak amplitude of the signal occurs at $t = t_p$ and equals to

$$V_{o,max} = |V_{out}(t = t_p)| = \frac{q}{C_f}\frac{C_p}{C_z}e^{-1}. \tag{5.5}$$

A two-stage amplifier is used to realize the gain block of the pulse shaper. The schematic of the amplifier is shown in Figure 5.3 and the device sizes are listed in Table 5.2. The amplifier draws ~ 60 μA from a 1.2 V supply, and provides a gain of 56.6 dB with a phase margin of 46° and a unity gain frequency of 46.6 MHz.

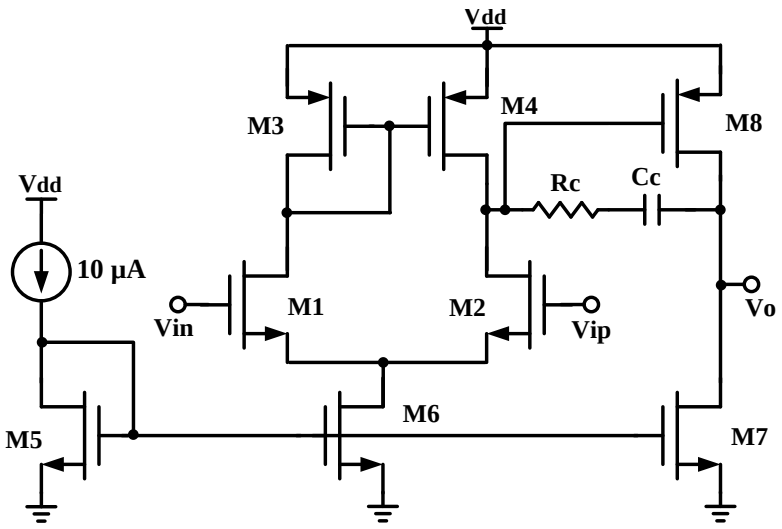


Figure 5.3: Circuit realization of the gain block of the pulse shaper.

5.1.3 Design of the Reset Network

As explained in Chapter 2, the generated charge from the detector is integrated on the feedback capacitor. After integration, the capacitor must be discharged in order to reset the system and prepare it for the next event. The role of a reset network is to provide a path for discharging the capacitor. The reset network must be carefully designed as it directly contributes to the noise of the system. The discharge time of the CSA must be significantly larger than the shaping time and also short enough to prevent pulse pile-ups at high event rates. Implementing a large discharge time has the challenge of integrating a high value feedback resistor in the reset network.

In this design, we need a circuit that can accommodate leakage current of CZT detectors which is in the range of 1 fA to 50 nA. The Krummenacher low-frequency feedback loop [12] appears to be a good choice for compensation of the leakage current of the CZT detectors based on the analysis of common reset mechanisms described previously in Chapter 2. The reset network that we have implemented is a modified version of the Krummenacher low-frequency feedback loop and is illustrated in Figure 5.4. In the original configuration the DC feedback resistance is fixed and is realized by the transconductance of the differential pair in the feedback network (i.e., $R_f = 1/g_{m3a}$). Once the bias current of the differential pair is set, the

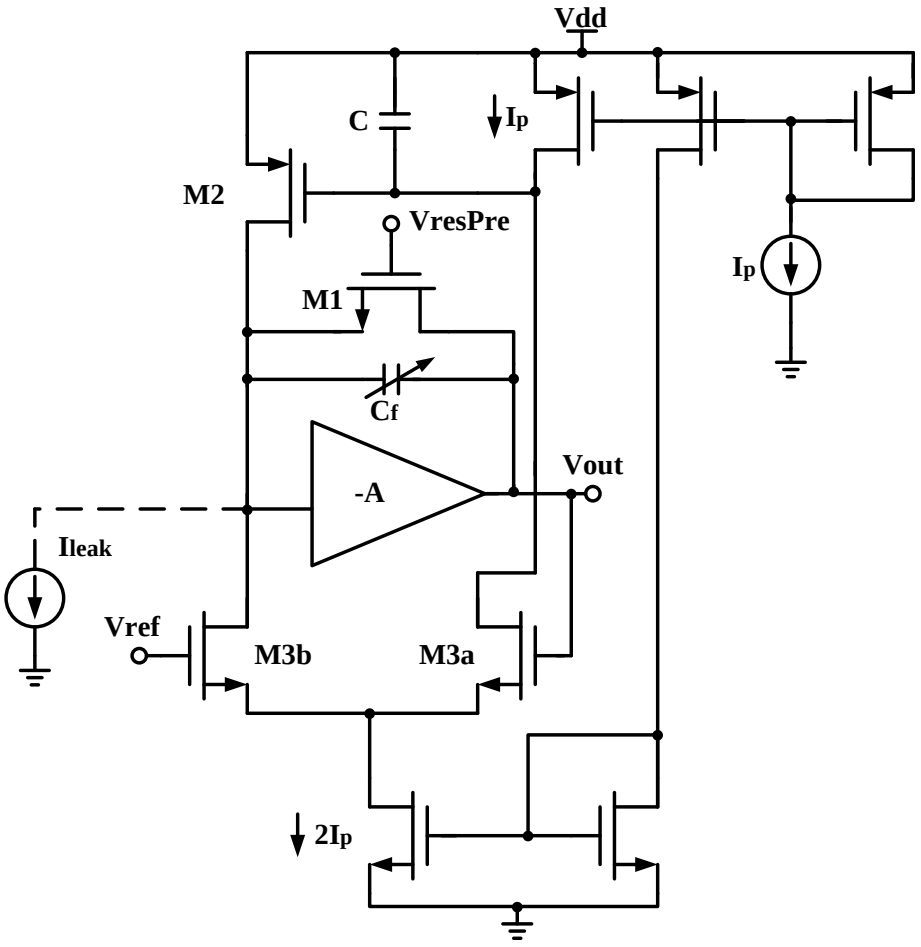


Figure 5.4: The designed reset network which is a modified version of the Krummenacher low-frequency feedback loop. Drain current of transistor M_2 is adjusted to compensate the leakage current of the detector. Transistor M_1 is introduced to adjust the decay time constant of the CSA.

discharge time constant of the CSA will be fixed. In some applications, it might be necessary to adjust the decay time constant of the CSA in order to deal with various event rates. We have modified the circuit by introducing a MOS device that can be used to change the effective DC feedback resistance and accordingly the discharge time constant of the CSA. The bias current of the reset network is set to 250 pA to lower the noise contributions of the MOS devices in the network.

5.1.4 Noise Analysis and Optimization

As explained previously in Section 3.2, the noise of a detector readout system is usually expressed in terms of the ENC. The noise of the readout circuit is modelled by series and parallel noise sources referred to the input of the circuit [156]. The series and parallel noise power spectral densities are uncorrelated. Following the procedure described in Section 3.2, the input-referred series and parallel noise sources are derived analytically and are given by the following equations.

$$ENC_{w,ser}^2 = \alpha_w n_{sub} \gamma \frac{4k_B T}{g_m} \frac{C_{tot}^2}{4\pi q^2 e^{-2} t_p} \times \left| B\left(\frac{3}{2}, \frac{1}{2}\right) \right|, \tag{5.6}$$

$$ENC_{f,ser}^2 = \frac{K_{fs}}{WLC_{ox}} \frac{2\pi^2 t_p^2 C_{tot}^2}{q^2 e^{-2} (2\pi t_p)^{3-\alpha_{fs}}} \times \left| B\left(\frac{3-\alpha_{fs}}{2}, \frac{1+\alpha_{fs}}{2}\right) \right|, \tag{5.7}$$

$$ENC_{w,par}^2 = 2qI_0 \frac{t_p}{4\pi q^2 e^{-2}} \times \left| B\left(\frac{1}{2}, \frac{3}{2}\right) \right|, \tag{5.8}$$

$$ENC_{f,par}^2 = A_{fp} \frac{{t_p}^2}{2q^2 e^{-2} (2\pi t_p)^{1-\alpha_{fp}}} \times \left| B\left(\frac{1-\alpha_{fp}}{2}, \frac{3+\alpha_{fp}}{2}\right) \right|. \tag{5.9}$$

In these equations, B represents the Beta function. The total ENC of the readout circuit is the sum of the individual ENC contributions and is given by

$$ENC_{tot}^2 = ENC_{w,ser}^2 + ENC_{f,ser}^2 + ENC_{w,par}^2 + ENC_{f,par}^2. \tag{5.10}$$

In the 0.13-μm CMOS process used in this analysis, the frequency-dependent parallel current noise sources of the readout circuit can be neglected without sig-

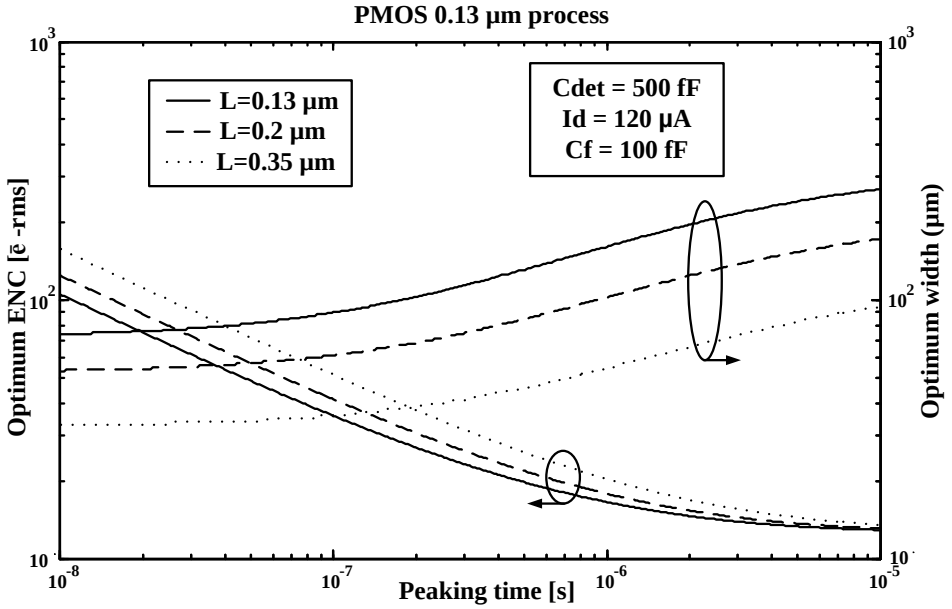


Figure 5.5: Theoretical optimum ENC of the front-end circuit and the corresponding optimum channel width as a function of peaking time for a PMOS input device for the 0.13-μm CMOS process used in this work. Since the input device size does not affect the detector leakage current, the noise associated with this leakage current is not taken into account in this optimization.

nificantly affecting the overall noise performance of the system [79]. Note that in a properly designed circuit, for the purpose of optimization of the input device size of the CSA, the detector leakage current and the noise sources in the reset network can be ignored since these noises are typically independent of the input device size. Obviously, the noise contributions from the detector and the reset network must be included in the noise calculations of the system. To optimize the noise performance of the readout system, one has to minimize (5.10) with respect to the design parameters of the CSA and those of the pulse shaper simultaneously. Figure 5.5 shows the theoretical optimum ENC of the front-end circuit and the corresponding optimum channel width as a function of the peaking time for a p-type MOS input device in the 0.13-μm CMOS process used in this work. It is assumed that the detector has a capacitance of 0.5 pF and the overall drain current of the CSA input

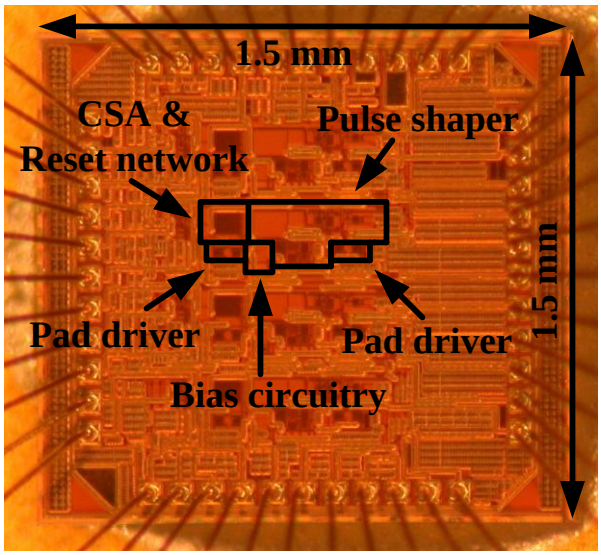


Figure 5.6: Chip micrograph. The chip includes four identical readout channels and is packaged in a standard 44-pin CQFP.

devices is 120 μA. The optimization has been performed for three different channel lengths. Based on Figure 5.5, the optimum width increases with increasing the peaking time, whereas the optimum ENC decreases as the peaking time increases. For larger peaking times, the increase in the optimal width is more pronounced. This can be explained by taking a closer look at the individual ENC contributions. At large peaking times, the series flicker noise is the main contributor to the total ENC whereas at small peaking times the series white noise dominates the overall noise. Since the flicker noise is inversely proportional to $W \times L$ of the input device, for large peaking times, the optimal ENC is achieved by increasing the device size. At small peaking times, however, the optimum width does not vary significantly with respect to the peaking time, since the series white noise of the input device is a weak function of the device dimensions.

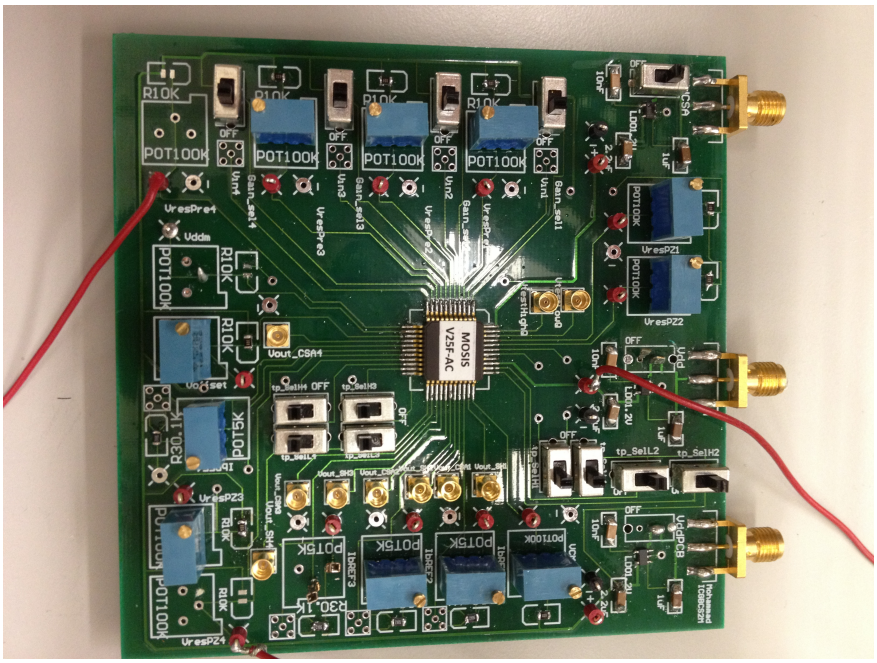


Figure 5.7: Custom-designed FR4 printed circuit board (PCB).

5.2 Experimental Results

The designed ASIC is implemented in a standard 0.13-μm CMOS technology. Figure 5.6 shows a micrograph of the chip that is packaged in a standard 44-pin ceramic quad flat package (CQFP). The main building blocks of the chip are marked on the figure. To evaluate the performance of the chip, we have designed a custom FR4 printed circuit board (PCB) where the chip is mounted on. Figure 5.7 shows the picture of the fabricated PCB. The ASIC contains four identical readout channels with a total die area of $1.5 \times 1.5\ mm^2$. The power consumption of each readout channel is about 1 mW when connected to a 1.2 V supply. The specifications of the 4-channel device are summarized in Table 5.3.

5.2.1 Transient Response of the Readout System

Figure 5.8 shows the measured waveforms at the output of the pulse shaper for three values of VresPZ. The injected charge is about 10 fC which is injected to the input terminal of the CSA by applying an external pulse to an integrated test

Table 5.3: Specifications of the ASIC

Specification	Value
Fabrication process	Standard 0.13-μm CMOS
Die size	$1.5 \times 1.5\ mm^2$
Package	CQFP-44
Number of channels	4
Power supply	1.2 V
Power consumption	1 mW/channel
Rate	Max. 100 kcycles/s
Sensor	$<$ 5 pF capacitance $<$ 50 nA dark current

capacitance of 250 fF. As shown in this figure, the output overshoot voltage is cancelled by adjusting the gate voltage of the MOS device in the PZC network. After adjustment, the output signal quickly returns to the baseline which verifies that the PZC circuit functions as expected.

Figure 5.9 shows the measured voltage at the output of the pulse shaper for high and low charge ranges. The voltage gain is estimated to be 8.5 and 50 mV/fC for high and low ranges, respectively. The integration is linear up to 5 and 45 fC for the low and high ranges, respectively.

The desired peaking time for each channel can be selected using two digital inputs (tp_SEL1 and tp_SEL0 as shown in Figure 5.1). Figure 5.10 shows the measured waveforms at the output of the pulse shaper for various peaking times. From this figure, the measured peaking times are 108 ns, 220 ns, 560 ns, and 1.14 μs. The VresPZ voltage is kept constant during the measurement. It is possible to bring the peaking times closer to their theoretical value by adjusting this voltage.

The discharge time constant of the CSA can be adjusted by varying the bias voltage of transistor M_1 (i.e., $VresPre$) in Figure 5.1. The captured waveforms at the output of the CSA for different values of $VresPre$ are shown in Figure 5.11. According to this figure, the discharge time can be adjusted from about 1 to 7 μs. A short discharge time is desired in applications where a high event rate is required, whereas, a long decay time is useful in applications where a long shaping time and a low noise performance are required.

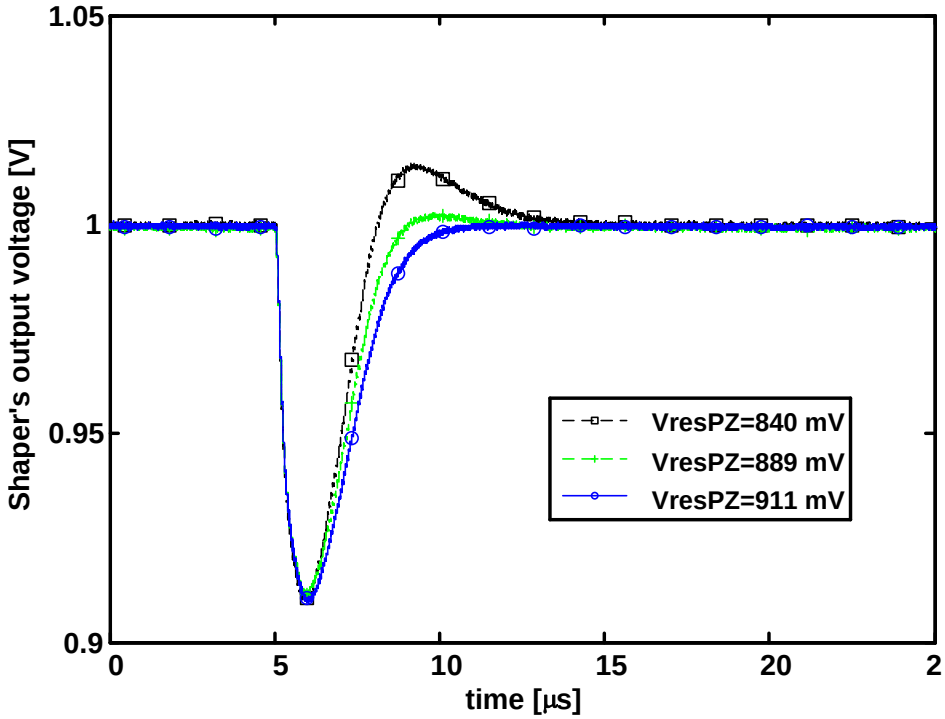


Figure 5.8: Captured waveforms at the output of the pulse shaper for an injected charge of about 10 fC. The overshoot voltage is cancelled by adjusting the gate bias voltage (i.e., $VresPZ$) of the MOS device in the PZC network.

5.2.2 Noise Evaluation of the Readout System

In Section 3.3 we described how to measure the noise of the readout system. Figure 5.12 shows the block diagram of the designed noise measurement setup. The setup consists of a PCB test board, an active probe, and three types of instruments. The instruments include two power supplies, a function generator, and a spectrum analyzer. Separate power supplies are used for the chip and the components on the PCB. Low dropout (LDO) linear voltage regulators are placed on the board to provide clean voltage to the chip and other components. They also compensate for voltage drops on the supply cables. The digital inputs are provided to the chip using toggle switches. Voltage dividers are placed all over the board to provide

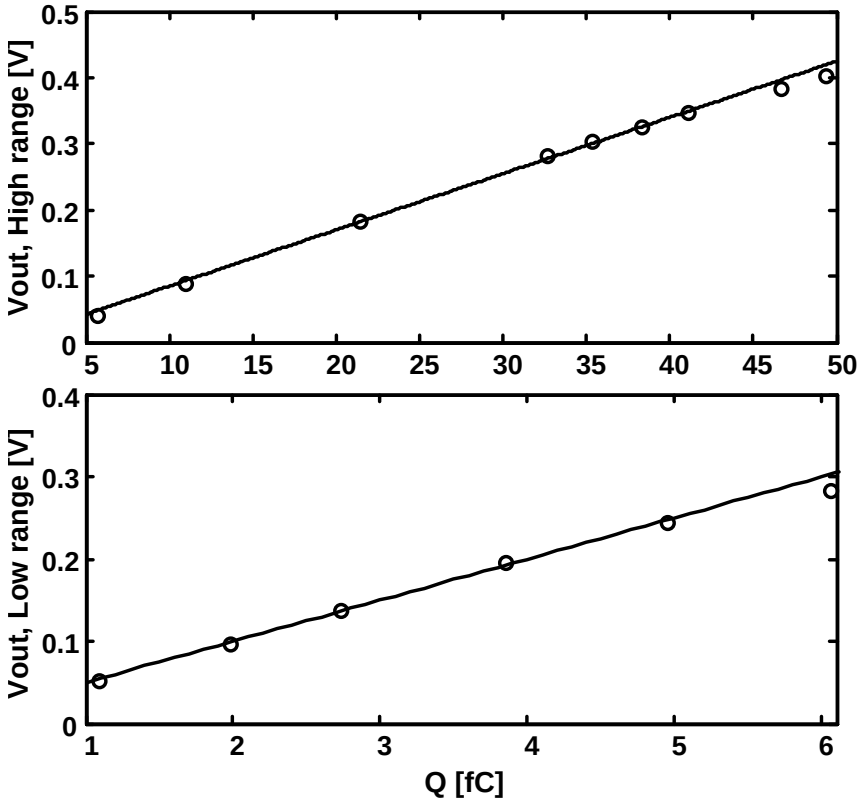


Figure 5.9: Measured voltage at the output of the pulse shaper for high and low ranges. The integration is linear up to 5 and 45 fC for the low and high ranges, respectively.

analog bias voltages to the chip. Please note that only one switch and one voltage divider is shown on the figure for simplicity. A function generator will produce pulses which will inject a precise amount of charge into the circuit at desired intervals. The spectrum analyzer will be used to measure the signal to noise ratio at the output of the pulse shaper.

The designed text fixture operates with a 5 V supply voltage. One Xantrex LXQ-30-2 power supply is used to power up the device under test (DUT). The output voltage of this instrument ranges from 0 to 30 V and the maximum available bias current is 2 A which is much higher than the minimum required current to operate the DUT. The accuracy and precision of the power supply is of no concern

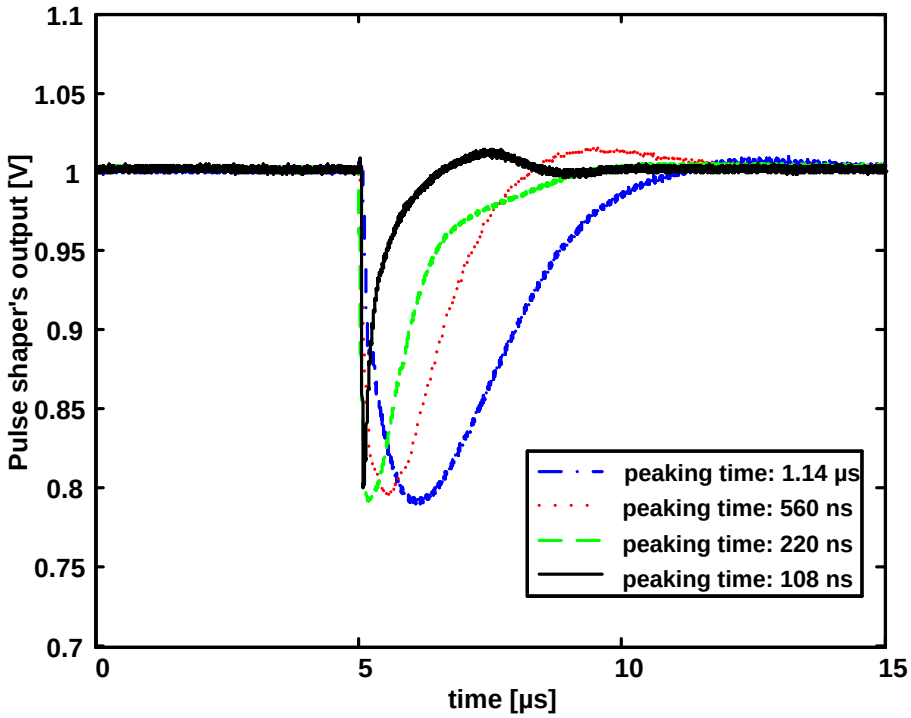


Figure 5.10: Measured waveforms at the output of the pulse shaper for various peaking times. VresPZ voltage is not altered during the measurement.

because the power supply will be set to provide an input voltage of 5 V which is much higher than the minimum required voltage for operating the regulators. The DUT is designed conservatively and therefore can tolerate even a 2 V change in the supplied voltage.

We have used Agilent 33250A for generating pulses with desired amplitude and frequency. This instrument is an arbitrary function generator and is capable of producing up to 50 MHz pulse waveforms with variable rise/fall times. The output amplitude of this instrument can be set with a resolution of 0.1 mV and an accuracy of ($\pm$1% of setting $\pm$1 mVpp) which is acceptable for our measurements.

The instrument that we choose to measure the signal-to-noise ratio at the output of the circuit must satisfy two important requirements. The first requirement is that

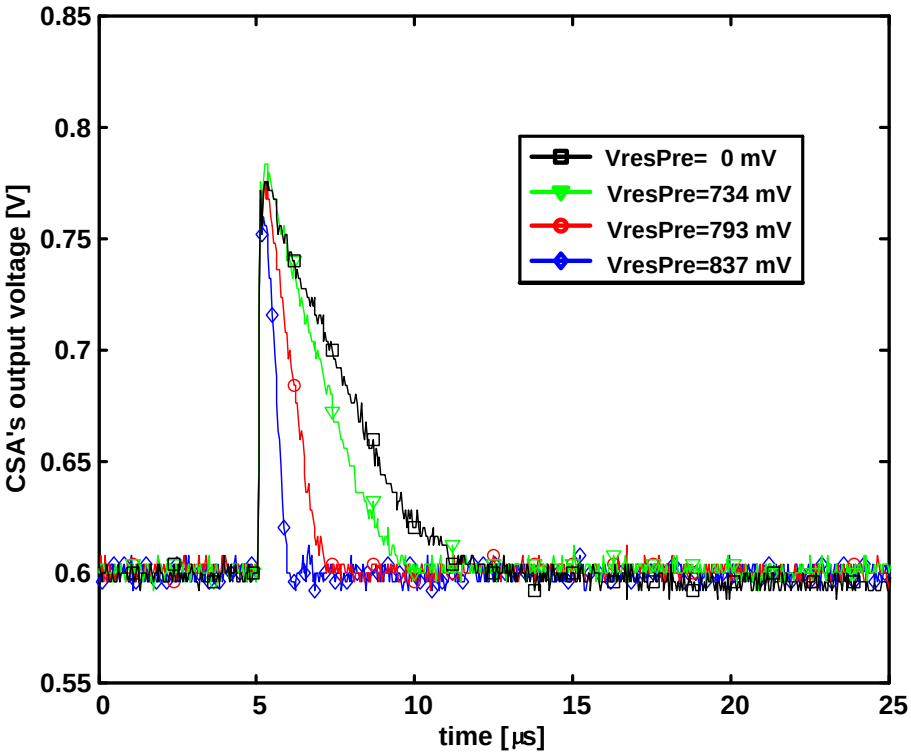


Figure 5.11: Measured waveforms at the output of the CSA for various values of the *VresPre* control voltage. The discharge time of the CSA can be adjusted from about 1 to 7 μs.

the minimum dynamic range of the instrument must be higher than that of the system. Lets assume that we need to measure an ENC of as low as 10 $\bar{e}$-rms. This results in a calculated signal-to-noise ratio of about 56 dB when 1 fC charge is injected into the circuit. Most of current spectrum analyzers have a dynamic range of 100 dB or more and can satisfy the minimum dynamic range requirement. The second requirement is that the instrument must be able to measure the noise of the system at very low frequencies. This is essential in order to determine noise of the system accurately as most of noise power falls within low frequencies.

Amongst available signal analyzers, Agilent N9030A is the only instrument that can cover very low frequencies. The frequency range of this instrument is 3 Hz to 26.5 GHz. The only problem with this instrument is that the input DC level

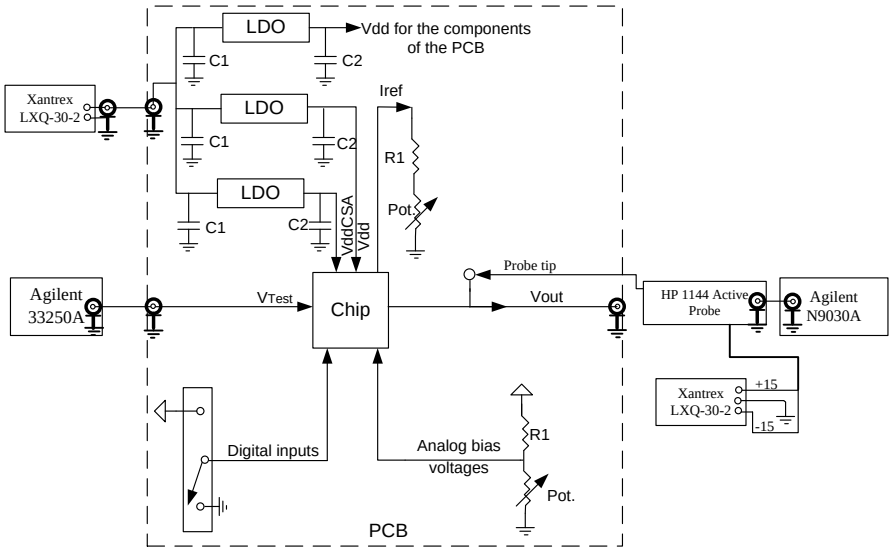


Figure 5.12: Noise measurement setup diagram. Several switches and voltage dividers are used to supply the digital inputs and the bias voltages to the chip, respectively. Note that only one switch and one voltage divider is shown for simplicity.

must be within ± 0.2 V when DC coupled. The output signal from the DUT has a DC level of around 0.8 V. Besides, the integrated chip buffers are not designed to derive the 50 Ω input impedance of the instrument. To overcome these problems, we use the HP 1144 Active Probe. The probe has a bandwidth of 800 MHz which is much higher than the bandwidth of our system. The integrated chip buffers can easily derive the input impedance of the active probe which is 2 pF in parallel with 1 MΩ. The probe has a rise time of 440 ps or less which is sufficient for our measurements.

Figure 5.13 shows the measured voltage noise density at the output of the pulse shaper for a peaking time of 1140 ns. The measurement is done in a shielded chamber. Figure 5.14 shows the measured ENC of the readout circuit for the available peaking times. The calculated ENC of the readout system varies between 66 to 101 $\bar{e}$-rms for a peaking time in the range of 108 to 1140 ns. This is in agreement

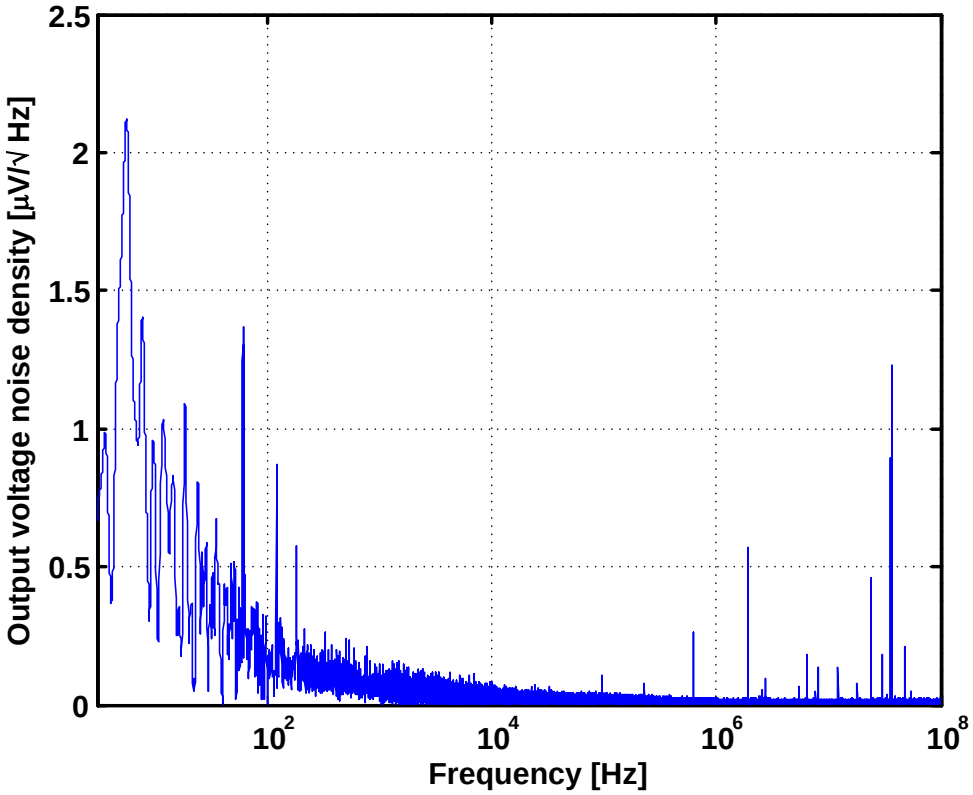


Figure 5.13: Measured voltage noise density at the output of the pulse shaper for a peaking time of 1140 ns.

with the theoretical results where the ENC of the system decreases with an increase in peaking time. Table 5.4 summarized the performance of the proposed readout circuit and compares it with relevant designs.

5.3 Summary and Conclusions

In this chapter, the detailed design and analysis of a low-power low-noise four-channel readout circuit for solid-state radiation detectors, in particular CZT, is presented. Each readout channel includes a charge-sensitive amplifier, a reset network to accommodate the leakage current of the detectors, and a first-order pulse shaper with a pole-zero cancellation circuit. The CSAs have two gain settings for 0 to

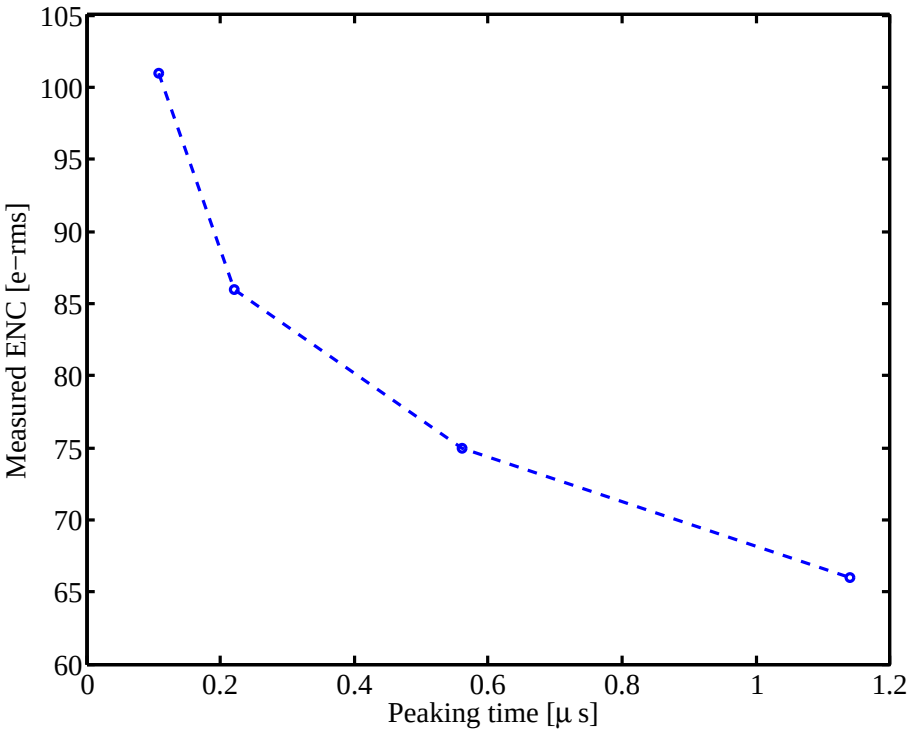


Figure 5.14: Measured equivalent noise charge of the system versus different peaking times for a 250 fF detector capacitance.

5 fC and 5 to 45 fC injected charge. The pulse shaper is programmable and is designed to provide four different shaping times. The discharge time constant of each CSA can also be adjusted to accommodate various event rates. Furthermore, a comprehensive noise analysis of the readout system is presented. To facilitate noise analysis, the equivalent noise charge equations are derived analytically. Optimization of the noise performance of the front-end circuit is also discussed. The application-specific integrated circuit (ASIC) is fabricated in a 0.13-μm CMOS process. For a detector capacitance of 250 fF, the measured ENC varies between 66 to 101 $\bar{e}$-rms at available peaking times. The power consumption of each channel is measured to be only 1 mW.

Table 5.4: Readout circuit performance comparison

Specification	This work	[44]	[157]	[158]	[159]	[160]
Fabrication process	0.13-μm CMOS	0.35-μm CMOS	0.25-μm CMOS	-	0.8-μm CMOS	0.8-μm BiCMOS
Signal processing chain	CSA, leakage compensation, shaper, PZC	CSA, PZC, fast/slow shaper, comparator, Sample-and-Hold	CSA, shaper, PZC, Baseline Holder, Peak-Detect & Hold	CSA, shaper, discriminator, Sample-and-Hold	CSA, shaper, two discriminators, counters	Reset CSA, shaper, PZC
Detector capacitance [pF]	0.25	0*	0*	1	3	0*
Peaking time [μs]	0.1-1.14	8	2	10	0.8	1.2
Power consumption per channel [mW]	1	3	2	2.8	4	0.5
ENC [$\bar{e}$-rms]	66-101	89	≈ 100	85**	200	$220-500$

* without detector attached ** in the presence of a leakage current of 20 pA

Chapter 6

Design and Analysis of a Complete Readout System for Solid-State Radiation Detectors

6.1 Introduction

In the previous chapter we presented the detailed design and analysis of a four channel device which consisted of a CSA with leakage compensation, pole-zero cancellation circuit, and a first-order pulse shaper. The focus of the design was on design of the CSA, and noise optimization. The focus of this chapter is on the design and analysis of the pulse shaper and the signal processing blocks of a readout system. The design of the signal processing blocks of the readout signal is challenging as it requires design and simulation of mixed-signal circuits. As a proof of concept, we will design a complete readout system. The integrated readout system consists of a CSA with leakage compensation, a Gaussian pulse shaper, a peak-detect-hold (PDH), a discriminator, and an analog-to-digital converter (ADC). The test chip is laid out and fabricated in a 0.13-μm CMOS technology. Measurement results of the readout circuit will be presented.

The first-order pulse shaper in Chapter 5 consists of one gain stage and a number of passive and active devices. Although the design of this pulse shaper is simple

and its power consumption is small, it is not a good choice for high resolution or high counting rate applications. In high resolution readout systems it is essential to employ a pulse shaper which exhibits a superior noise performance. Gaussian pulse shapers are popular choices for such systems. In high counting rate applications the return to baseline of the pulses must be fast. Gaussian pulse shapers are also good choices for high counting rate applications. The return to baseline of the Gaussian pulse shapers is shortened by increasing the number of integrators, however, the power consumption of the circuit will increase accordingly as these filters are often realized using active circuits.

6.2 Readout Circuit Design

The readout system is intended for the readout of capacitive detectors, particularly, CdZnTe detectors. The block diagram of the readout system is shown in Figure 6.1. The readout system consists of a charge-sensitive amplifier, a reset network, a PZC circuit, a 5^{th}-order Gaussian pulse shaper, a peak-detect-hold (PDH) circuit, a discriminator, a Wilkinson-based analog-to-digital converter, and a digital conversion controller circuit. The peaking time and the gain of the pulse shaper can be adjusted using two 2-to-4 decoders. Most of the bias voltages and currents are generated on chip using an external bias current. The readout system operates as follows.

The weak signal from the sensor is converted to voltage at the output terminal of the CSA. The reset network creates a discharge path for the feedback capacitor and also compensates for the leakage current of the detector. The discharge time-constant of the signal at the output of the CSA can be controlled by adjusting the gate voltage of M_1. After integration over the feedback capacitance, the signal is passed to the pulse shaper. The pulse shaper is a 5^{th}-order Gaussian filter and consists of a differentiator followed by two active filters. The gain and peaking time of the pulse shaper can be controlled using two 2-to-4 decoders. After pulse shaping the signal is passed to the PDH (also called a pulse stretcher) and then the ADC for digitization. A conversion control state machine is designed that controls the digitization process. For systems with a large number of channels, it is impractical to allocate a dedicated ADC per channel due to the high cost in terms of area and power. Thus, it is essential for such systems to multiplex the outputs of

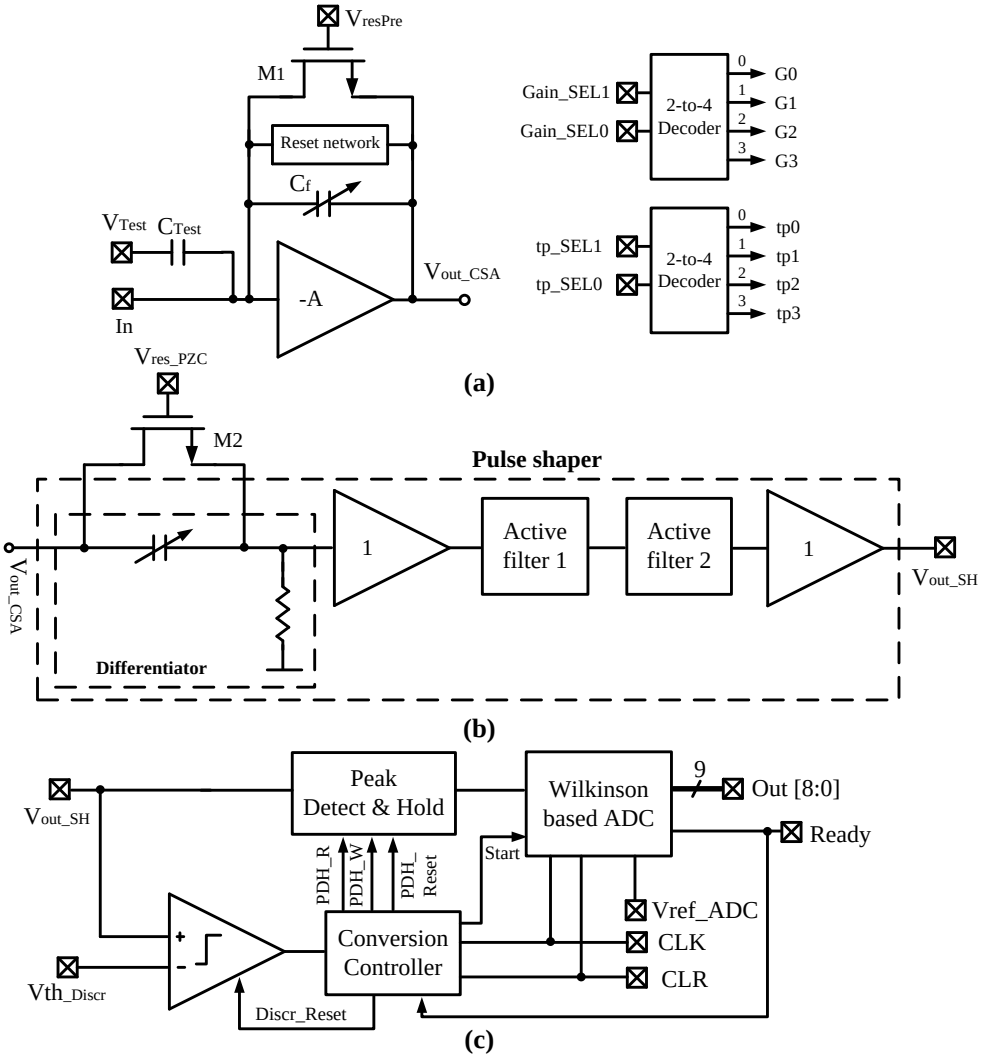


Figure 6.1: Simplified block diagram of the fabricated readout system. The block diagram shows (a) the charge-sensitive amplifier, the reset network, and two 2-4 decoders, (b) a 5^{th}-order Gaussian pulse shaper, and (c) the peak-detect and hold, the discriminator, the Wilkinson-based analog-to-digital converter, and the digital conversion controller.

several channels and use a fewer number of ADCs. To identify the events that need to be digitized a discriminator is used which generates a trigger signal whenever the signal level at the output of the pulse shaper is higher than a threshold level. In the following subsections we will describe the design and analysis of the main building blocks of the readout system in detail.

6.2.1 Charge-Sensitive Amplifier and Reset Network

The implemented CSA is a folded-cascode configuration with single-ended input and output ports. The circuit topology of the CSA is the same as the one described in Section 5.1.1. The implemented reset network is a modified version of the Krummenacher's low frequency feedback loop. The design of the reset network was described in detail in Section 5.1.3.

6.2.2 Gaussian Pulser Shaper

Gaussian pulse shapers are popular choices for many readout circuits. The output signal returns to baseline quickly and a good signal-to-noise ratio is achieved. The implemented pulse shaper is a 5^{th}-order Gaussian filter with adjustable gain and peaking time. The pulse shaper consists of a differentiator followed by a buffer, and two active filters. The structure of the active filter is shown in Figure 6.2. Each active filter has a complex pole pair. The transfer function of the active filter is given by [161]

$$H(s) = \frac{\frac{-R_1}{R_3}}{R_1 R_2 C_1 C_2 s^2 + R_1 C_1 s + 1} \tag{6.1}$$

As can be seen from this equation, resistor R_3 has no effect on the location of the poles of the filter. This suggests that the gain of the filter can be varied by adjusting the value of this resistor. We have used this feature in the design of the pulse shaper. One of the decoders allows adjusting the gain of the pulse shaper by selecting one of the available R_3 resistors.

The circuit schematic of the implemented pulse shaper is shown in Figure 6.3. The design procedure for the pulse shaper is given in detail in Appendix A. The transistor shown in this figure is used for pole-zero cancellation. The transistor

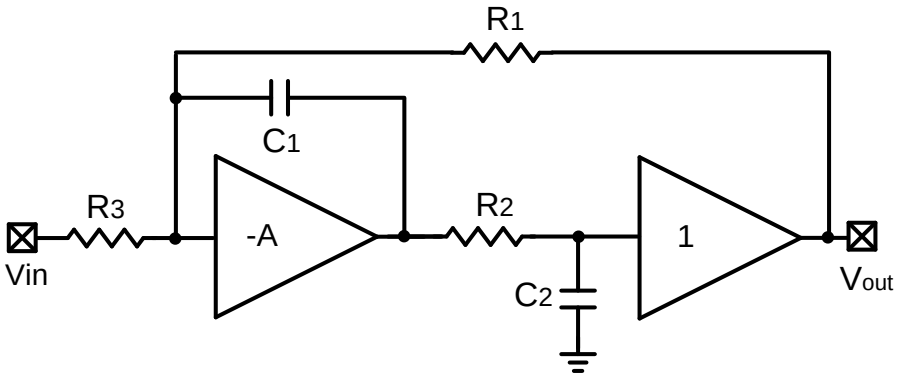


Figure 6.2: Structure of a second-order active filter with complex poles.

introduces a zero in the transfer function of the differentiator and modifies the location of the associated pole with the differentiator. The amplifiers in the design are two-stage CMOS opamps with frequency compensation. The circuit schematic of the amplifiers was shown previously in Figure 5.3.

6.2.3 Peak-Detect and Hold

The output of the pulse shaper is connected to the input of a PDH before the digitization stage. A PDH generates a signal that follows the input signal up to the peak of the signal and stays constant after the peak is detected.

The principle operation of the designed PDH is based on a popular two-phase architecture described in [120]. The circuit schematic of the PDH is shown in Figure 6.4. The designed PDH is offset-free and uses a low-power operational transconductance amplifier (OTA), a current mirror, switches, and a hold capacitor. The switches in this figure are implemented using complementary MOS devices. The circuit schematic and the device sizes of the OTA block of the PDH are shown in Figure 6.5. A PMOS differential pair is chosen as the input stage of the OTA which allows processing of input signals with low common-mode voltages.

The operation of the PDH is as follows. The switches S1, S2, and S5 are closed in the Write (W) phase. The input signal is applied to the negative terminal of the OTA and the OTA drives the current mirror. As the input voltage increases, the OTA sinks the current and the capacitor charges accordingly. When the voltage

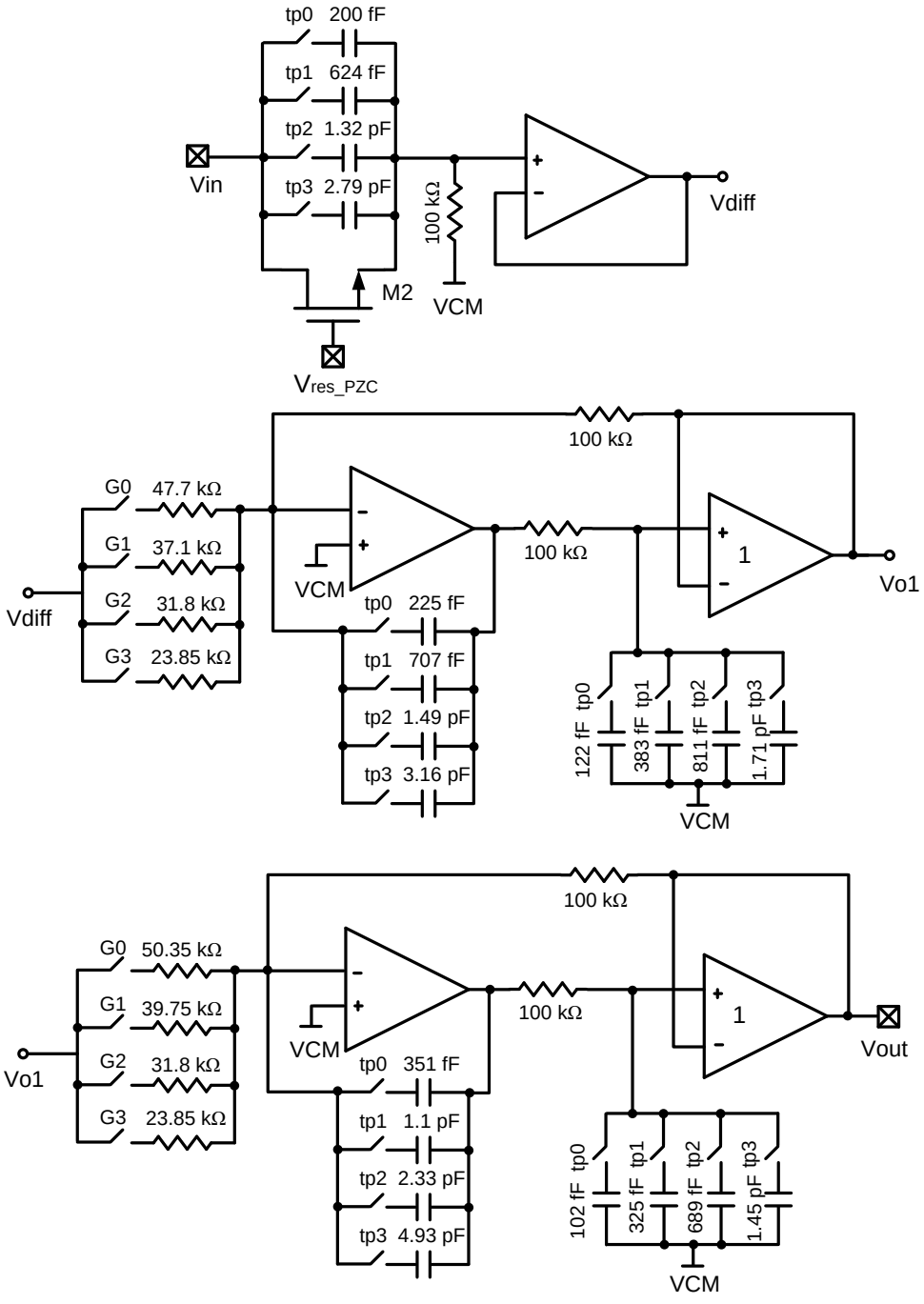


Figure 6.3: Circuit schematic of the 5^{th}-order active Gaussian pulse shaper.

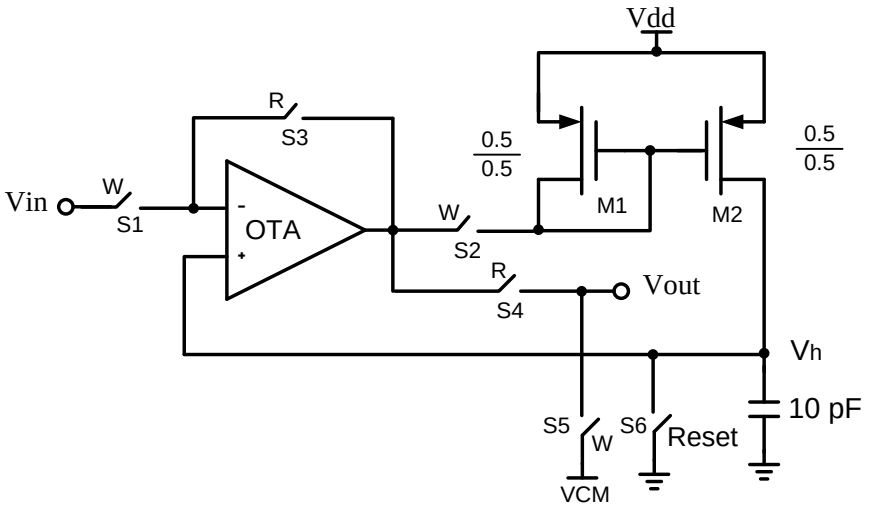


Figure 6.4: Circuit schematic of the implemented peak-detect and hold.

across the capacitor reaches the peak voltage of the input signal, the current mirror stops charging the capacitor and the peak voltage of the input signal is stored on the capacitor. So in the Write phase the circuit tracks the input signal, and detects and holds its peak voltage. The offset voltage of the OTA is also stored on the hold capacitor (C_h). In the Read (R) phase, S1, S2, and S5 switches are opened and S3, and S4 switches are closed. The OTA is placed in a buffer configuration and its output terminal is connected to the output port. In this phase the offset voltage of the OTA is subtracted from the hold voltage of the capacitor (that includes the offset of the OTA from the Write phase) and the peak voltage of the signal is provided to the output. After the voltage is read out, S6 switch is closed which resets the capacitor and the PDH becomes ready to accept another signal. The W, R, and Reset signals are provided by the Conversion Controller block.

6.2.4 Discriminator

A discriminator is often used in readout systems to identify the channels with incidents [23, 162–164]. The discriminator compares the output signal of the pulse shaper with a threshold voltage and toggles whenever its input signal crosses the threshold level. Thus the discriminator generates a pulse whenever the signal at the

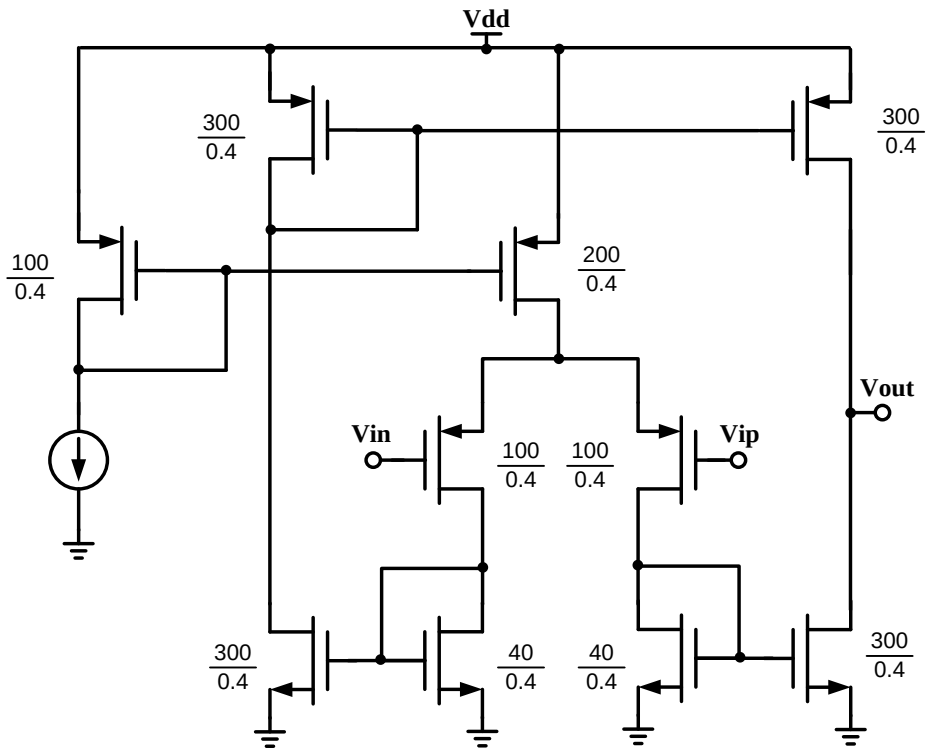


Figure 6.5: Circuit schematic of the implemented operational transconductance amplifier.

output of the pulse shaper crosses the threshold and returns to baseline. The conversion controller reacts to the change in the the output voltage of the discriminator by generating the timing signals for the PDH and ADC. The delay of the discriminator is often desired to be minimized since in some readout systems the PDH is enabled only after the output of the discriminator changes state. Figure 6.6a shows the circuit schematic of the implemented discriminator. When the *Reset* signal is high, the operational amplifiers are placed in a unity gain configuration and the offset voltage of the amplifiers is stored on the capacitors. When the *Reset* signal is low, the discriminator acts as a high-speed comparator.

The circuit schematic of the operational amplifier for the discriminator is shown in Figure 6.6b. The device dimensions are marked on the figure. Each opamp con-

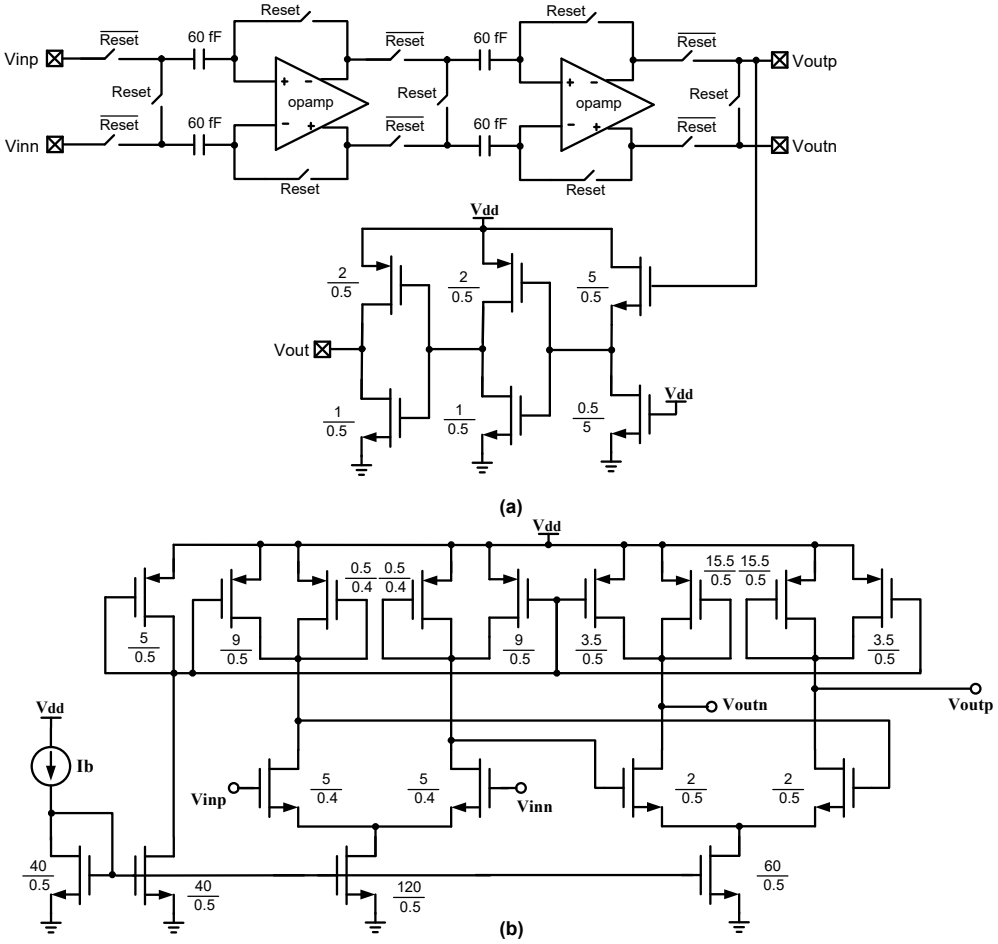


Figure 6.6: Circuit schematic of the implemented (a) discriminator, and (b) operational amplifier block of the discriminator.

sists of two differential pairs with active loads. Figure 6.7 shows the transient simulation results of the discriminator. In this simulation, the applied voltage at the negative input terminal of the discriminator is kept constant at 1.65 V while the voltage at the positive terminal is swept from 1.645 to 1.655 V. When the *Reset* is high, the differential outputs are connected together and the single ended output goes high. To increase the speed of the discriminator, the swing voltage of the differential outputs is kept about 460 mV while the single-ended output has a

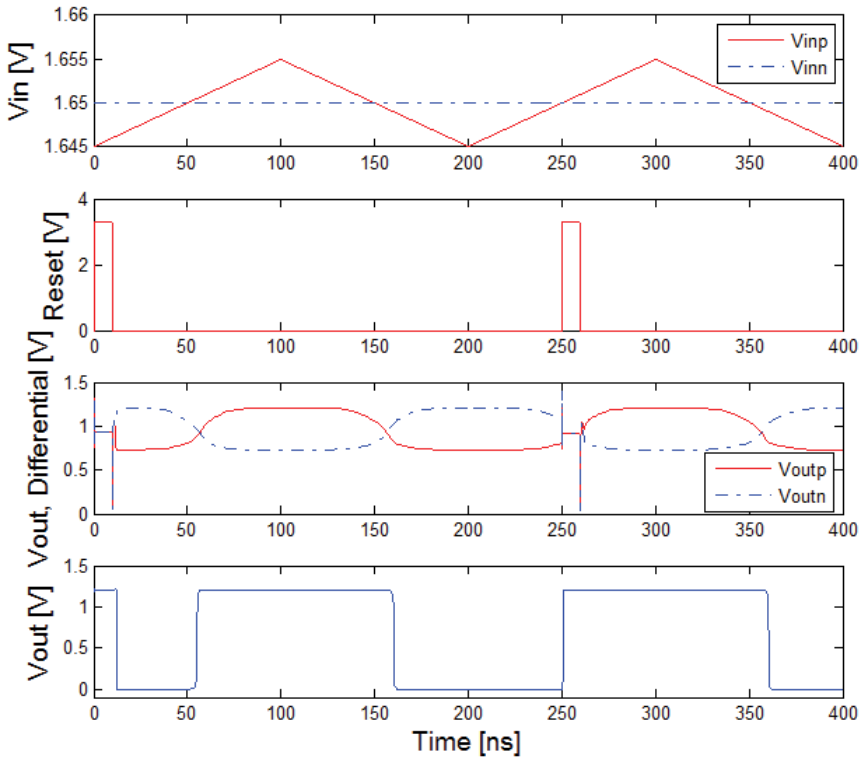


Figure 6.7: Simulated transient response of the discriminator. The discriminator has a propagation delay of less than 10 ns for the input signals shown. The signal rise and fall times are less than 1 ns.

full swing of 1.2 V. According to this figure, the discriminator has a resolution of better than 5 mV. The propagation delay of the discriminator depends on how fast the signals at its input terminals are changing. For the signals shown on Figure 6.7, the propagation delay is less than 10 ns. The rise and fall times of the signal at the single-ended output of the discriminator are less than 1 ns.

6.2.5 Conversion Controller

The conversion controller block is used to control the operation of the PDH, ADC, and Discriminator. At each cycle the conversion controller resets both the PDH and the discriminator and then sets the $Write$ signal which tells the PDH to track the output signal of the pulse shaper. As soon as a pulse appears at the output of

the pulse shaper, the discriminator generates a pulse and also the PDH stores the peak voltage of the pulse. The conversion controller then sets the *Read* signal and the PDH delivers the peak voltage to the ADC for conversion. The conversion controller starts the ADC by setting the *Start* signal. The Verilog model of the conversion controller is given in Appendix B.

6.2.6 Wilkinson-Based ADC

The pros and cons of various types of ADCs was previously discussed in Section 2.4.7. Since in readout circuits for CZT detectors the incidents to be digitized are typically up to 1 ms apart, a Wilkinson-type ADC appears to be a good choice for such circuits. Thus, in this work we focus on the design of a Wilkinson-based ADC.

Overview of Operation

The operating principle of the Wilkinson ADCs is illustrated in Figure 6.8a [165, 166]. A Wilkinson-based conversion technique relies on comparison of the sampled voltage across a discharging capacitor with a reference voltage. The stable analog input voltage is first stored on a capacitor. Then the capacitor is disconnected from the input and immediately a constant current source is turned on which discharges the capacitor with a current equal to I_{dis}. As the discharge commences, a counter is enabled to count the number of clock pulses until the voltage across the capacitor reaches the reference level. At this moment, the comparator changes state and conversion stops. The discharge time of the capacitor and consequently the conversion time (T_{conv}) is a linear function of the input peak amplitude and is given by

$$T_{conv} = C \times \left(V_{p,in} - V_{ref}\right) / I_{dis}, \tag{6.2}$$

where C is the total capacitance that samples the input voltage, $V_{p,in}$ is the peak amplitude of the input signal, and V_{ref} is the reference voltage of the comparator. It can be shown that the differential linearity of this conversion technique is typically high and improves with more precise (i.e., lower jitter) clock pulses. The drawback of this conversion technique is its relatively long conversion time. While this long conversion time may not be tolerable for some applications, it is not a concern for

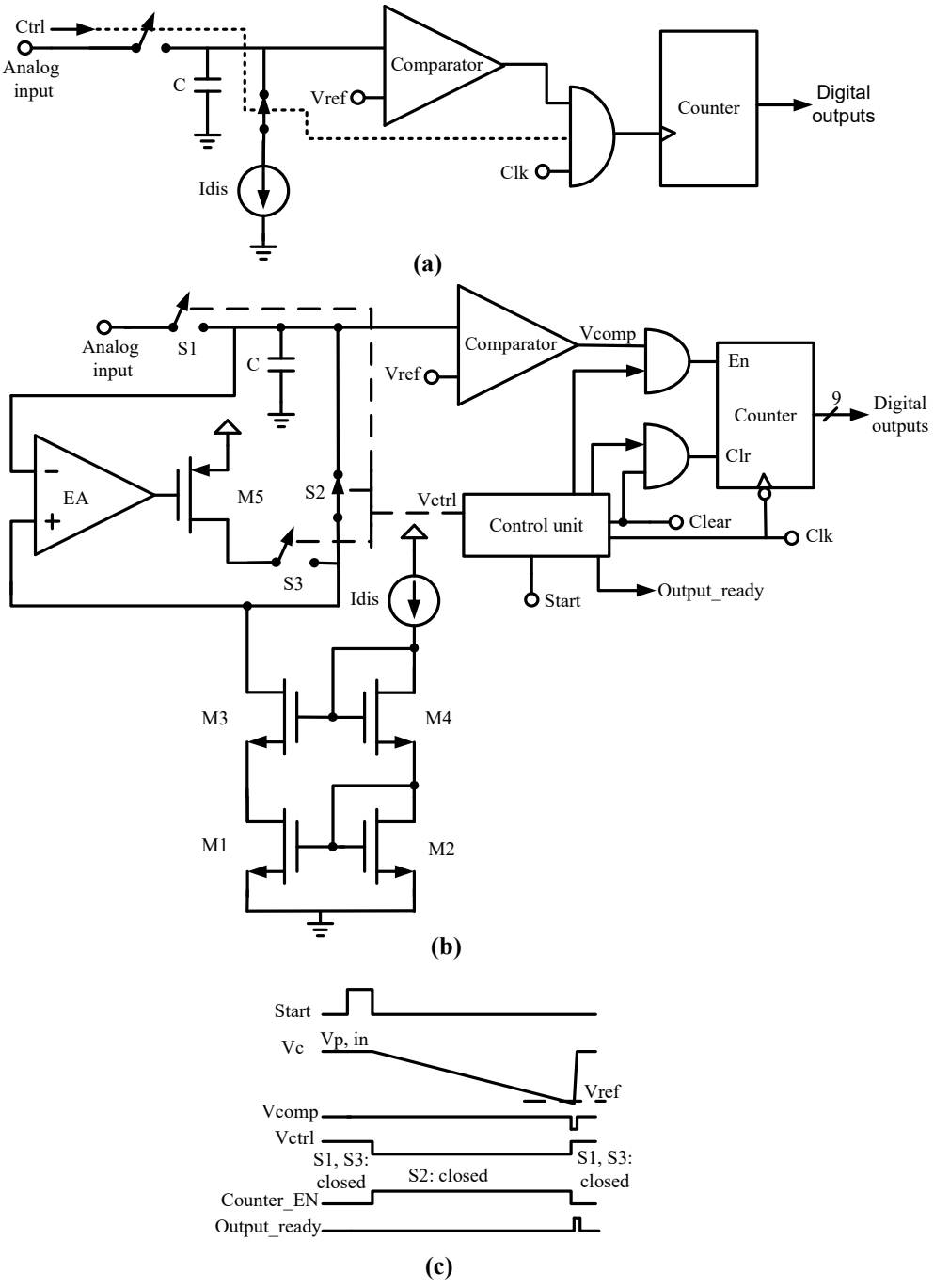


Figure 6.8: (a) Generic block diagram of a Wilkinson digitizer, (b) simplified circuit of the proposed Wilkinson-type ADC, and (c) timing signals of the proposed ADC.

the CZT application.

The Proposed Design

Figure 6.8b shows a simplified circuit of the proposed ADC. The design consists of the main building blocks of a Wilkinson-type digitizer (including a comparator, a 9-bit counter, and a discharging current source) plus an error amplifier (EA), a MOS transistor and a switch. The comparator in this design is implemented using an internal hysteresis [167] with offset cancellation [168, 169]. It also includes CMOS output buffers. The EA is a two-stage op-amp with Miller compensation [167]. The analog and digital blocks operate with different supply voltages and appropriate level shifters are used where necessary.

The control unit is a finite-state machine which controls the counter, enables sampling and discharge phases (using $Vctrl$ signal), and sets the $Output\_ready$ signal when the conversion is done. In the sampling phase, the switch S_2 is opened and switches S_1 and S_3 are closed. The analog input is stored on the capacitor C while the discharge current is diverted to M_5. The discharge phase commences with the falling edge of the $Start$ signal, a trigger signal provided by the discriminator. In this phase, S_2 is closed and S_1 and S_3 are opened. The discharge current source is connected to the capacitor via a current mirror and linearly discharges the voltage across the capacitor until the stored voltage reaches the reference level and consequently the output voltage of the comparator goes low. The $Output\_ready$ signal is raised at the end of the conversion and stays high for one clock cycle. The digital outputs keep their value until the $Start$ signal goes high again. The timing signals for the proposed ADC are shown in Figure 6.8c and the Verilog model of the control unit is given in Appendix C.

As mentioned earlier in this section, compared to a traditional Wilkinson-type digitizer Figure 6.8b contains additional circuitry which provides a path for the discharge current during the sampling phase. In the sampling phase, S_3 is closed and the discharge current flows into M_5 whose gate voltage is controlled by the EA. The input terminals of the EA are connected to both ends of S_2 which forces the drain voltage of M_3 to be equal to the sampled voltage across the capacitor. The EA ensures that the drain voltage and the current of M_3 stays constant when the

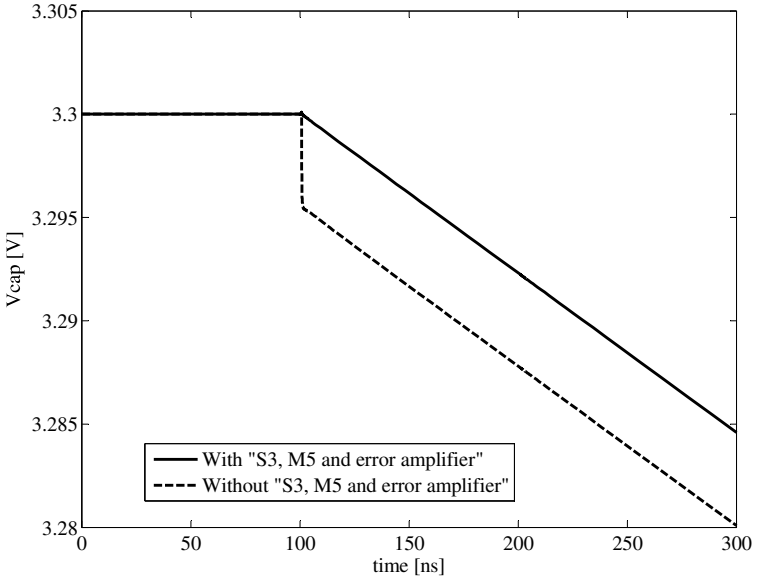


Figure 6.9: Simulated voltage across the capacitor. In the absence of the EA, M_5 and S_3, a voltage drop of about 5 mV is observed during the sampling period.

discharge phase commences. Without this proposed path for the discharge current, drain current of M_3 will suddenly rise from 0 to I_{dis} and the sampled voltage across the capacitor will drop instantly when S_2 is closed. This is due to the capacitor charge sharing between the capacitor on the drain of M_3 and the sampling capacitor. Figure 6.9 shows that with the inclusion of the above-mentioned circuitry the capacitor starts to discharge smoothly while in the absence of the circuit, a sudden voltage drop of as high as 5 mV ($\sim$1 LSB of the converter) occurs.

ADC Simulation Results

The ADC is designed and laid out in a 0.13-μm CMOS process (see Figure 6.10). The area of the converter is 0.026 mm^2 and the total power consumption from both 3.3 V (analog) and 1.2 V (digital) supplies is 631 μW. The power consumption of the converter is mainly due to the comparator and EA blocks and can be further reduced by employing an EA with a lower gain. The control unit is designed and placed and routed using a library of standard cells. To increase the dynamic range

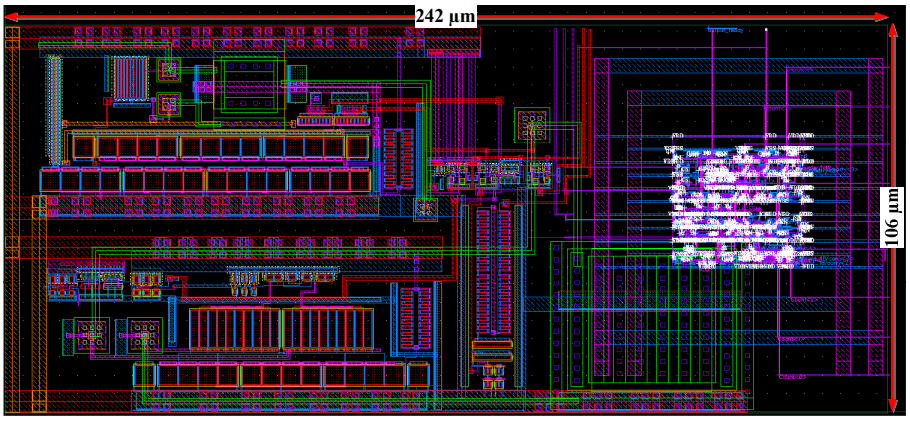


Figure 6.10: Layout of the proposed ADC in a 0.13-μm CMOS process.

of the digitizer, thick-oxide devices are used to implement the analog section.

The input dynamic range of the ADC is 2.7 V, ranging from 0.6 V (minimum signal) to 3.3 V (maximum signal). Minimum input signal is chosen such that the transistors M_1 and M_3 operate in saturation region at all times to minimize non-linearities. With a total capacitance of about 7.585 pF and a discharge current of 1 μA, the discharge phase for the maximum signal takes 20.48 μs. Consequently, to achieve a 9-bit resolution (LSB of 5.273 mV), a clock frequency of 25 MHz is required. Figure 6.11 shows the simulated transient behaviour of the ADC for the maximum input voltage. The stored voltage across the capacitor is discharged by I_{dis} starting at the falling edge of the *Start* signal. When the voltage across the capacitor reaches the reference level of 0.6 V, conversion stops and the *Output_ready* flag is raised. Careful examination of the ADC output shows that no output code is missing and all the states are identifiable.

As explained earlier, a Wilkinson-type digitizer exhibits excellent differential linearity. The simulated differential non-linearity (DNL) and integral non-linearity (INL) of the proposed ADC are shown in 6.12. The DNL and INL of the ADC are $\pm$0.065 LSB and 0.954 LSB, respectively.

One source of nonlinearity is the gate parasitic capacitances of the MOS input devices of the EA and those of the comparator which directly add to the effective discharge capacitance. These parasitic capacitances are highly nonlinear and their

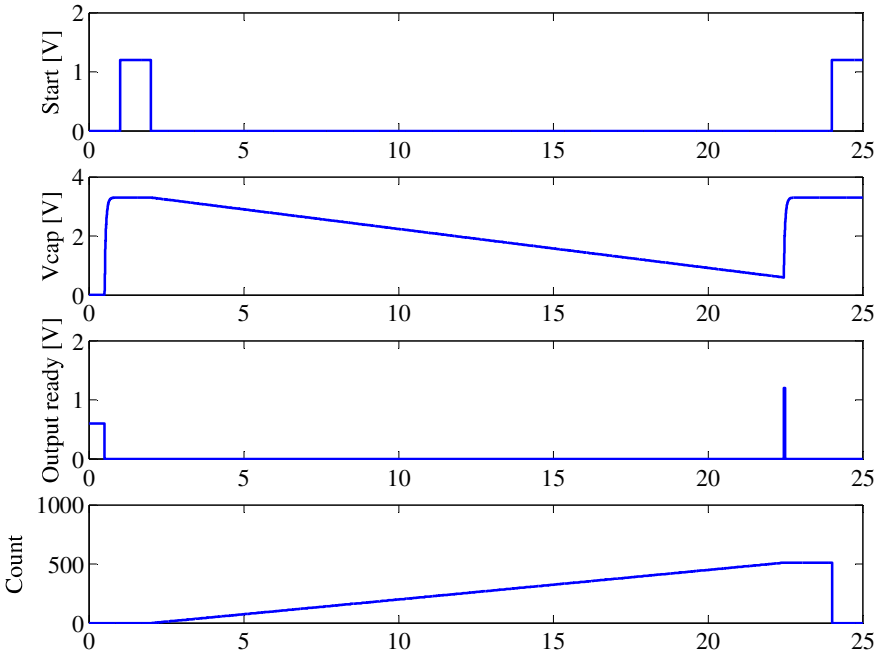


Figure 6.11: Simulated transient behaviour of the digitizer for maximum input voltage. The sampled voltage across the capacitor discharges linearly with the falling edge of the *Start* signal. The *Output_ready* flag is raised at the end of conversion. The ADC has no missing codes.

value strongly depend on the region of operation of the devices. Considering the wide dynamic range of the ADC, the value of these parasitic capacitances could vary drastically which would deteriorate the linearity of the converter. Therefore, special attention must be paid to minimizing the value of these parasitic capacitances by choosing appropriate sizes for the input devices of the EA and the comparator such that their parasitic capacitances are insignificant as compared to the capacitance C. In our design, the parasitic capacitances form less than 0.4% of the total sampling capacitance.

To calculate the dynamic specifications of the ADC a sinewave with a frequency of 90 Hz and a peak-to-peak value of 2.7 V is sampled at about 46.5 kHz and is applied to the converter. Figure 6.13 shows the spectrum of the reconstructed output voltage. From this figure, the spurious free dynamic range (SFDR), the ratio between the fundamental signal and the highest spur in the spectrum, is about

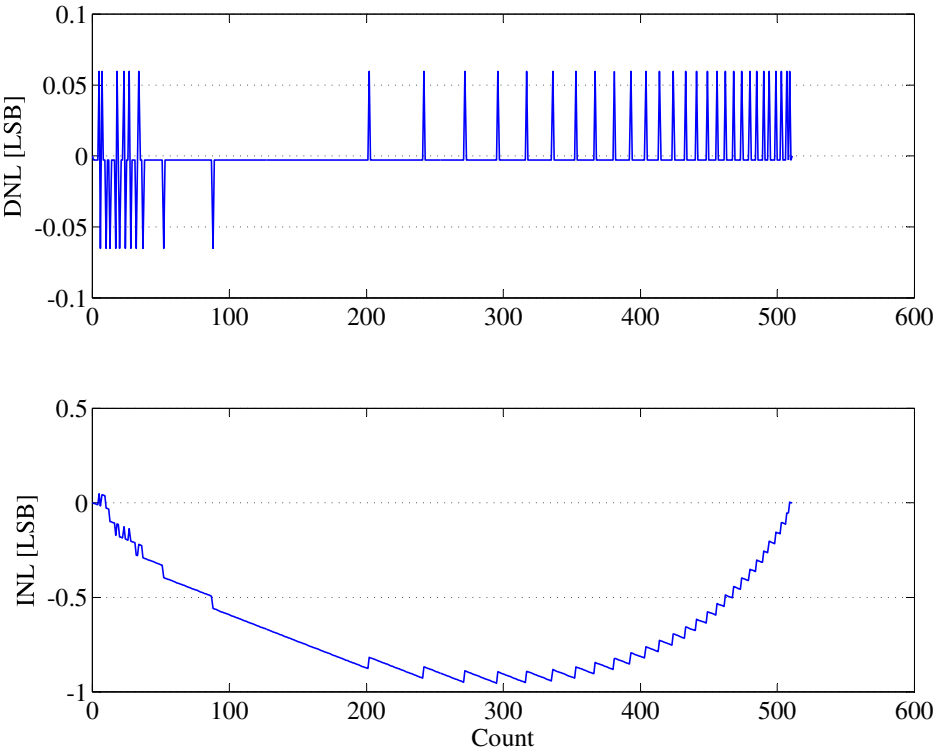


Figure 6.12: Simulated differential and integral nonlinearities of the ADC. The converter shows excellent differential linearity. Maximum DNL and INL are $\pm$ 0.065 LSB and 0.954 LSB, respectively.

55 dBc.

The signal-to-noise and distortion ratio (SNDR) for the ADC is about 50.2 dB corresponding to an effective number of bits of $ENOB = (50.2 - 1.76)/6.02 = 8.05$. The signal-to-noise ratio (SNR) is about 54.7 dB. Table 6.1 summarizes the performance of the ADC and compares it with relevant literature. As can be seen from the table, the performance of the proposed ADC compares favourably in terms of DNL, dynamic range, area and power consumption with that of other designs.

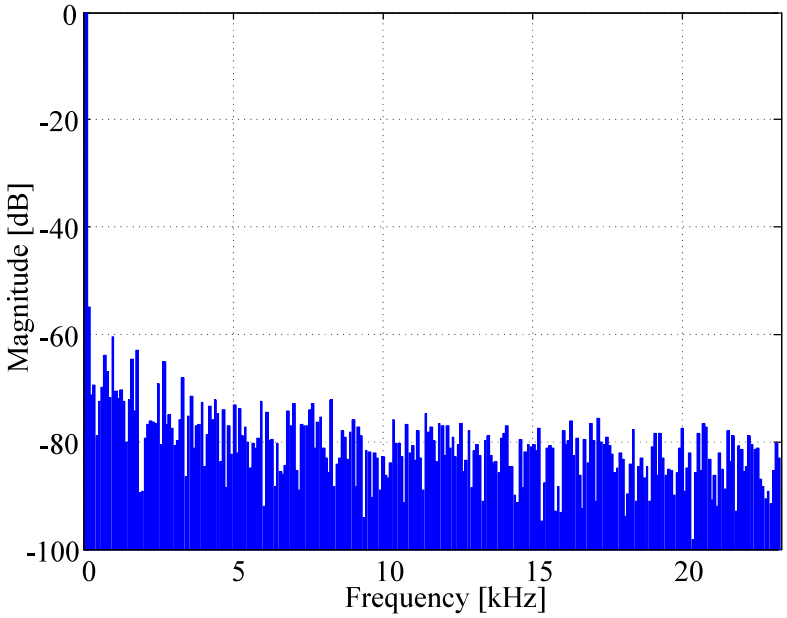
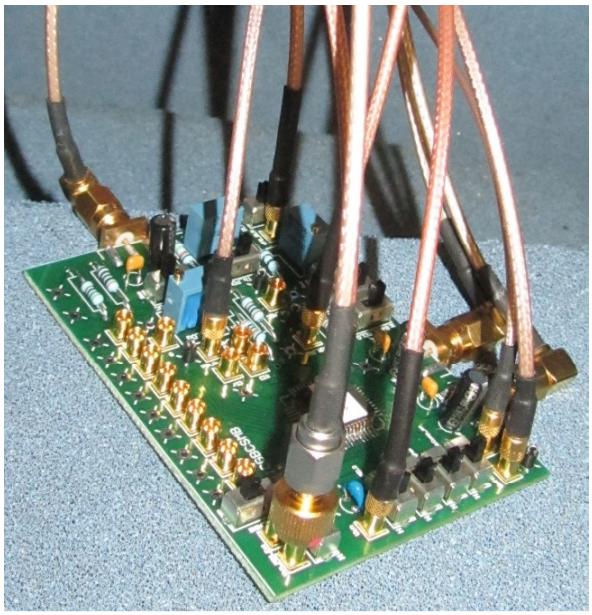


Figure 6.13: Simulated spectrum of the output signal for a sinewave input with an amplitude of 2.7 V and a frequency of 90 Hz.

6.3 Experimental Results

To evaluate the functionality of the designed readout circuit a chip was designed and implemented in a 0.13 μm CMOS process. A 2-layer printed circuit board was also designed and fabricated in order to measure the performance of the chip. Figure 6.14a shows the photograph of the board. For sensitive measurements (e.g., noise measurement) the board was placed in a shielded chamber which absorbs external noise and interfering signals. The photograph of the board in the shielded chamber is shown in Figure 6.14b. A test capacitor is used to inject precisely controlled amount of charges into the circuit. The capacitance of the detector is also modelled by integrating a 0.5 pF capacitance in parallel with the input terminal of the CSA.



(a)

(b)

Figure 6.14: Photographs of the (a) printed circuit board, and (b) the shielded chamber used for evaluating the performance of the fabricated chip.

Table 6.1: ADC performance summary and comparison

	This work*	[131]**	[134]***
Architecture	Wilkinson	Wilkinson	Wilkinson
Process (CMOS)	0.13 μm	0.35 μm	0.35 μm
Resolution (Bit)	9	12	10
Dynamic range (V)	2.7	2	-
f_{clk} (MHz)	25	100	50
Max conversion time	20.48 μs	400 ns	42 μs
ENOB (Bit)	8.05	-	-
SNR (dB)	54.7	-	-
SFDR (dBc)	≈ 55	-	-
DNL (LSB)	< 0.065	< 0.58	< 0.5
INL (LSB)	< 0.954	< 0.63	< 1
Supply voltage	3.3 V (analog), 1.2 V (digital)	-	3.3 V
Power consumption	0.631 mW	24 mW + 0.3 mW/channel	4.8 mW
Area (mm^2)	0.026 (w/o pads)	2.138 (die)	-

*Post-layout simulation results **Measurement results ***Simulation results

6.3.1 Amplification and Pulse Shaping

Figure 6.15 shows a sample oscilloscope waveform captured at the output of the pulse shaper. As expected, the integrated 5^{th}-order pulse shaper generates a smoother pulse in comparison with a CR-RC pulse shaper.

The pulse shaper shown in Figure 6.3 has an nMOS device (i.e., M_2) in the differentiator stage which is used for the purpose of pole-zero cancellation. The device makes it possible to compensate for non-idealities by modifying the location of the pole which is associated with the differentiator. The gate voltage of the nMOS device is controlled by the Vres_PZC signal. Figure 6.16 shows the measured waveforms at the output of the pulse shaper for three values of $Vres\_PZC$. Based on this figure, the undershoot at the output of the pulse shaper is removed

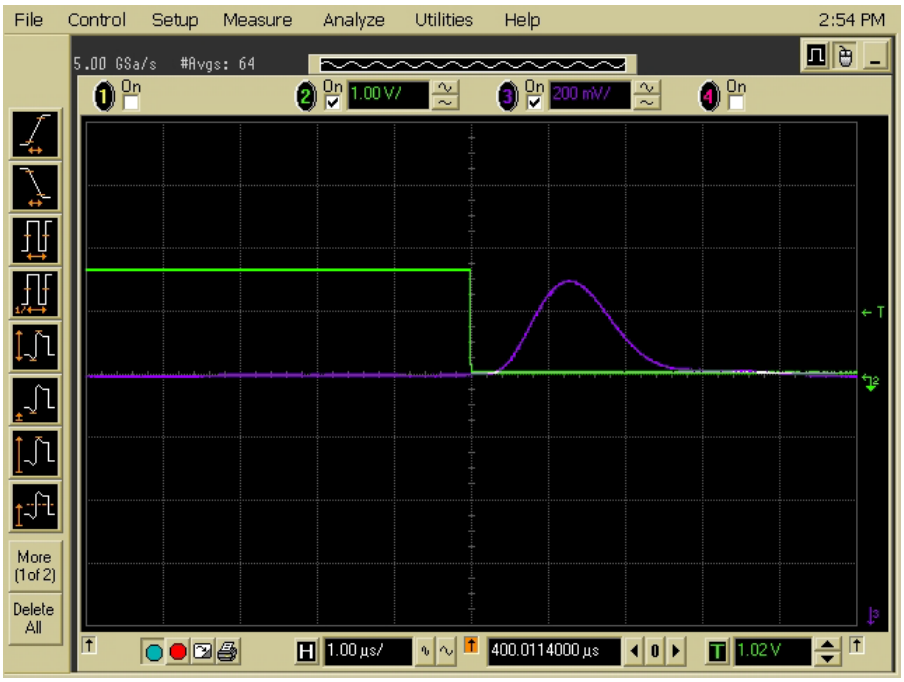


Figure 6.15: Sample oscilloscope waveforms. The waveform in green shows the applied step signal to the input capacitor and the waveform in violet shows the signal captured at the output of the pulse shaper.

effectively by adjusting the value of $Vres\_PZC$ signal.

The peaking time of the pulse shaper can be changed using an integrated 2-to-4 decoder. Figure 6.17 shows the measured waveforms at the output of the pulse shaper for the available peaking times. The measured peaking times are 290, 490, 764, and 1145 ns.

The amplification gain of the pulse shaper can be programmed using an integrated 2-to-4 decoder. Figure 6.18 shows the measured waveforms at the output of the pulse shaper for the available gain settings. The peaking time of the pulse shaper is kept constant.

The gain linearity of the circuit can be examined by plotting the change in the output voltage of the pulse shaper versus injected charge. Figure 6.19 shows the measured voltage at the output of the pulse shaper for injected charges of up to 40 fC. The output voltage is measured and compared for the available gain set-

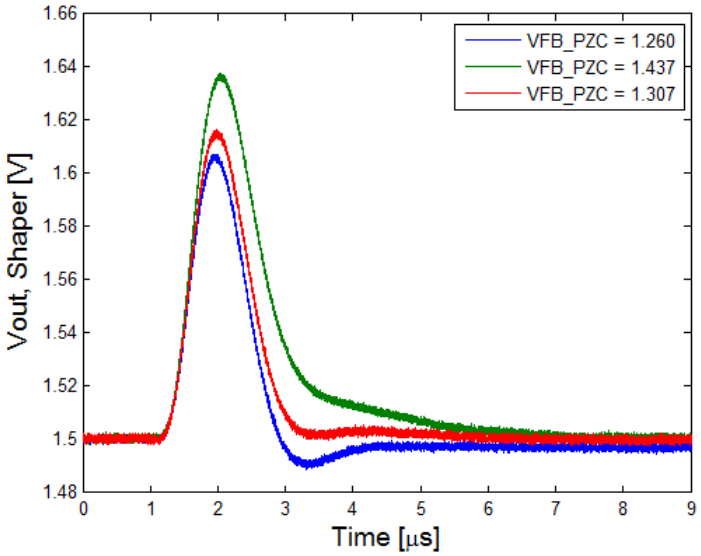


Figure 6.16: Captured waveforms at the output of the pulse shaper for three values of the *Vres_PZC* control signal (refer to Figure 6.3. The undershoot at the output signal is effectively removed by adjusting the value of the *Vres_PZC* signal.

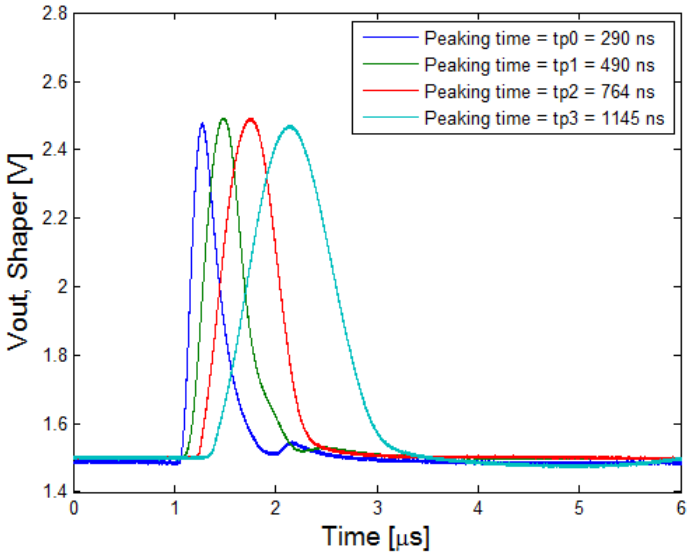


Figure 6.17: Captured waveforms at the output of the pulse shaper for various peaking times.

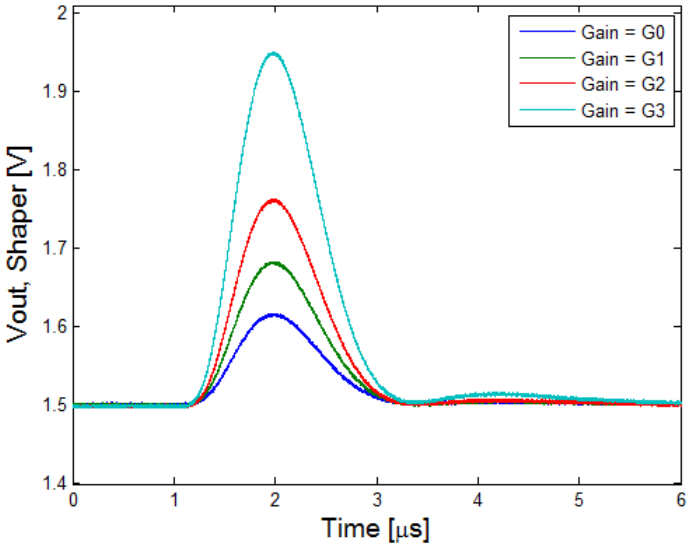


Figure 6.18: Captured waveforms at the output of the pulse shaper for the available gain settings.

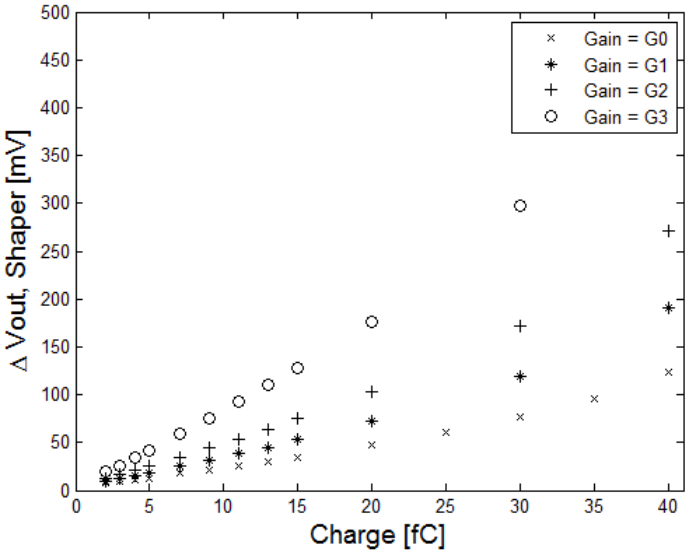


Figure 6.19: Measured change in the output of the pulse shaper for injected charges of up to 40 fC.

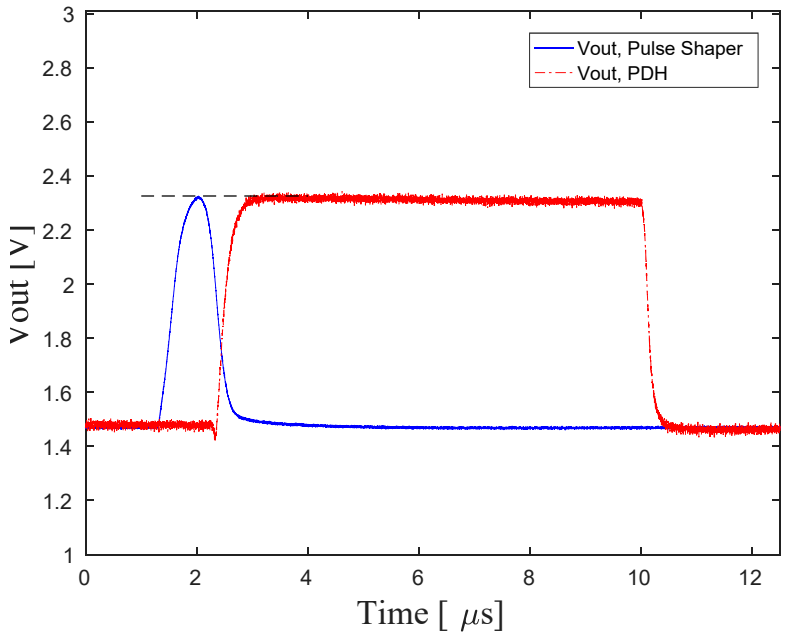


Figure 6.20: Captured waveforms at the outputs of the pulse shaper and the PDH.

tings (i.e., G0 to G3). The peaking time of the pulse shaper is kept constant. The measured charge gain of the readout circuit are 1.96, 3.06, 4.51, and 7.87 mV/fC.

6.3.2 Pulse Height Digitization and Processing

The output of the pulse shaper is passed to the PDH and the discriminator for further processing. The discriminator generates a pulse whenever the amplitude of the input pulse is higher than its threshold voltage. The Conversion Controller block generates the timing signals for the operation of the PDH and the discriminator. In order to test the functionality of the aforementioned blocks, the output signal of the PDH must be carefully examined. Figure 6.20 shows the signal from the pulse shaper and the generated signal by the PDH. Comparing the peak voltage

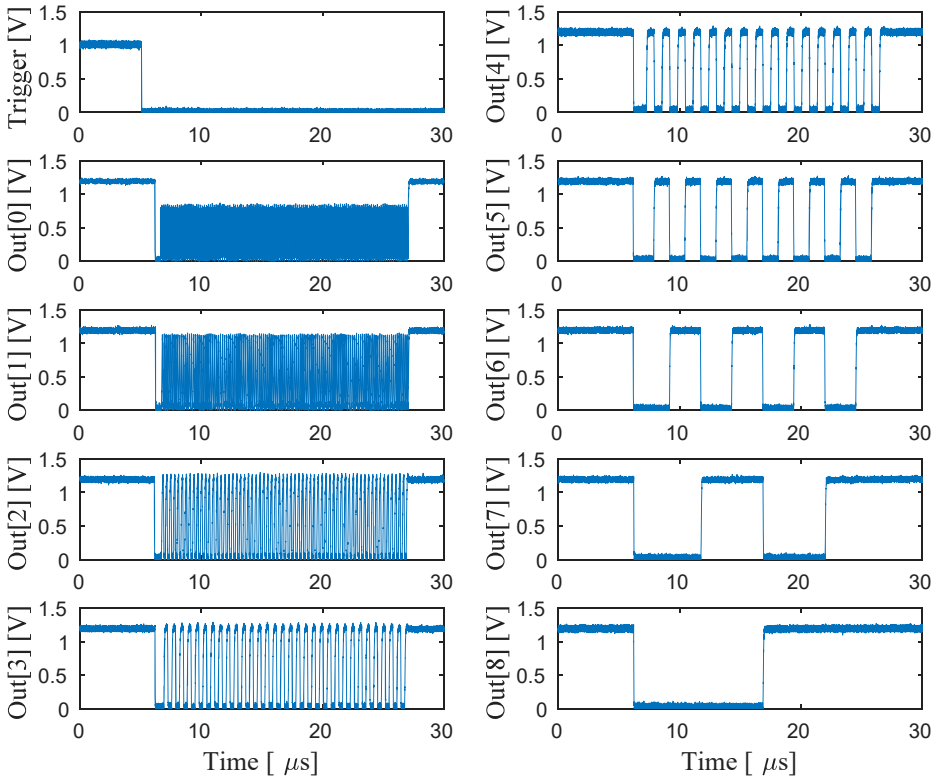


Figure 6.21: Captured waveforms at the outputs of the Wilkinson-based ADC for an input voltage of 3.3 V.

of the pulse shaper with that of the PDH confirms that the PDH detects the peak voltage of its input signal with a high accuracy. The output signal of the PDH has a negligible voltage droop which means the sampling time could be delayed without compromising the resolution of the readout circuit. After conversion is done by the ADC, the PDH is reset by the Conversion Controller block and its output signal returns to baseline. Examining the waveforms shown on Figure 6.20 also confirms that the discriminator and the Conversion Controller blocks operate as expected. The reason is that the timing signals that are essential for the operation of the PDH are generated by the Conversion Controller block. The Conversion Controller block itself is a finite state machine and generates the controlling signals based on the input received from the discriminator.

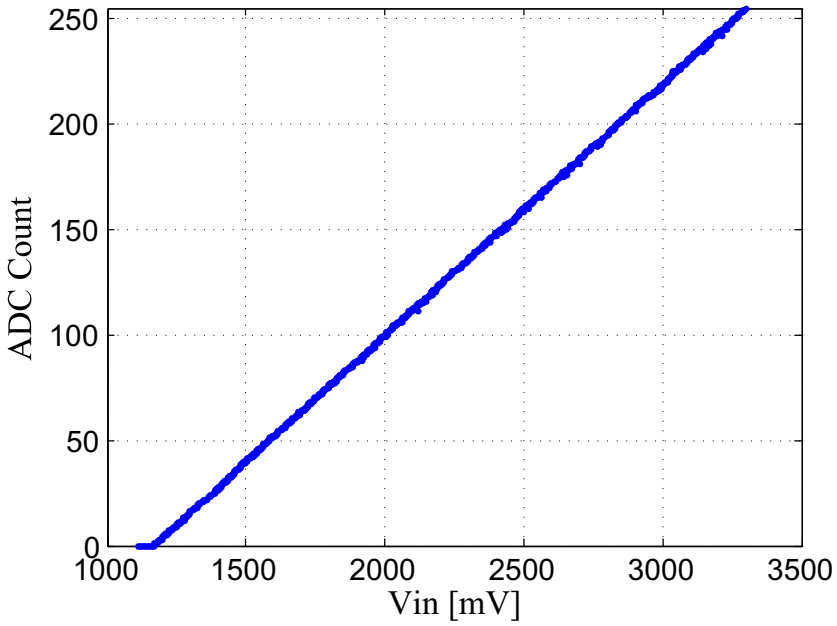


Figure 6.22: Measured transfer curve of the proposed ADC.

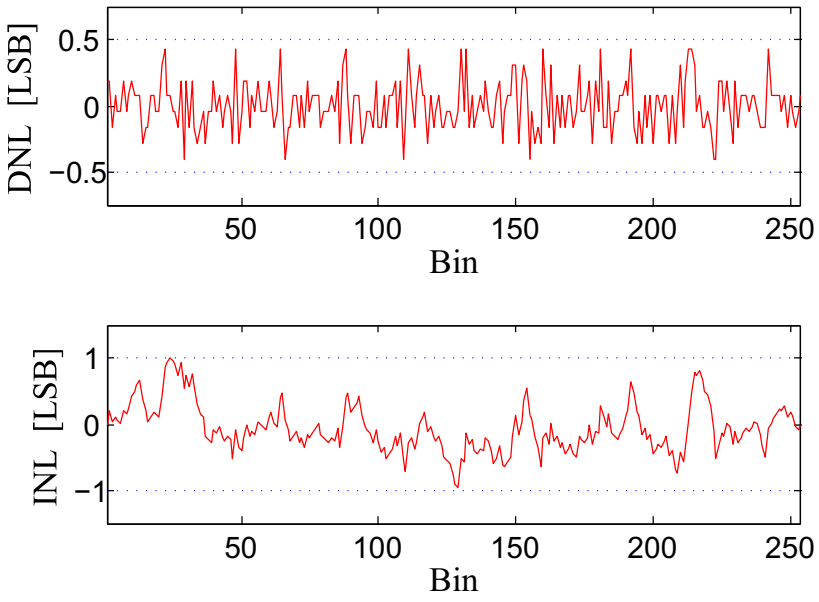


Figure 6.23: Calculated INL and DNL of the ADC from histogram testing.

The performance of the Wilkinson-based digitizer is also evaluated. In order to evaluate the performance of the ADC separately from that of the preceding blocks, the input terminal of the ADC must be kept at a constant voltage. The input terminal of the ADC is not directly accessible since the output terminal of the PDH is connected to the input terminal of the ADC. To measure the performance of the ADC, the PDH is bypassed by keeping its output voltage at a fixed voltage. As the start of conversion is controlled by the Conversion Controller block, a triggering pulse must be applied to the input terminal of the discriminator. If a pulse with sufficient amplitude is also applied to the input terminal of the readout circuit, the pulse shaper will generate a triggering pulse for this purpose.

Figure 6.21 shows the captured waveforms at the outputs of the digitizer for an input voltage of 3.3 V. The clock frequency is 25 MHz, and the reference voltage of the digitizer is 0.6 V. An active probe (HP 1144) is used for deriving the input impedance of the oscilloscope.

The linearity of the digitizer is evaluated using the linear ramp histogram (or code density) method. In this method a rising or falling linear ramp is applied to the input of the digitizer. The number of occurrences (or hits) of each code is directly proportional to the width of the code. If the code hits of a specified code is higher than the average, the step is wider than one LSB converter step. This indicates a positive DNL. Similarly, a negative DNL occurs when the code hits of a specified code is less than the average. The first (i.e., code 0) and the last codes are meaningless and their code occurrences are ignored in the linear ramp histogram calculations. The INL for each code can be calculated by adding the DNL errors as each code occurrence stands for a DNL of each step.

During the measurements on the ADC, two of the remaining packaged chips were accidentally damaged since the design did not contain any ESD structures. The rest of the measurements are reported for another chip. The most-significant bit (MSB) of the ADC on this chip is stuck at zero and only the first eight bits of the digitizer are functional. To capture the outputs of the ADC simultaneously, the output terminal are connected to eight high-speed comparators and the threshold voltage of the comparators is set to 250 mV. The outputs of the comparators are read out by a microcontroller. The microcontroller sends out the digital values to a personal computer by a Universal Asynchronous Receiver/Transmitter (UART).

A software is developed in C# language which receives and records the serial data. The software also communicates with Rigol's DP832A power supply over National Instruments' Virtual Instrument Software Architecture (VISA) protocol. The measurement process starts by the software which sets the voltage on the power supply. The ADC starts the digitization process at every negative-edge of the applied trigger signal. The conversion results are ready at every positive-edge of the trigger signal. After the voltage on the power supply is set and becomes stable, the microcontroller captures the digital codes at the outputs of the comparators and transfers the results to the computer. The output voltage of the power supply is gradually varied to create a ramp signal. After the measurement is finished, the captured analog input voltage and the ADC codes are then used in MATLAB to plot the transfer curve of the ADC and to calculate the INL and DNL of the digitizer. The source code and details of the developed software program are given in Appendix D.

Figure 6.22 shows the transfer curve for the first eight bits of the proposed ADC. Examining the transfer curve of the digitizer shows that no output code is missing. The extracted INL and DNL of the ADC are plotted in Figure 6.23. The DNL and INL of the converter vary from -0.4035 to 0.4317 LSB and from -0.962 to 0.9978 LSB, respectively. The measured DNL is less than 0.5 LSB but considerably higher than the theoretical result. One reason for the increase in the non-linearity of the digitizer is the effects of the power supply. The power supply can set the voltage with a resolution of 1 mV and a stability of 0.01% + 1 mV. Another reason is that the outputs of the ADC are not buffered on the chip and when the comparators load the outputs, the output amplitudes of the converter decrease which can lead to measurement errors. This is especially significant for the least-significant bit of the ADC which toggles at every clock cycle. To address this problem, the outputs of the ADC must be buffered before interfacing to the outside world. In future work, the number of output pins of the chip can be reduced by designing an I^2C or a serial interface for transferring the ADC digital codes to a personal computer for saving and further processing.

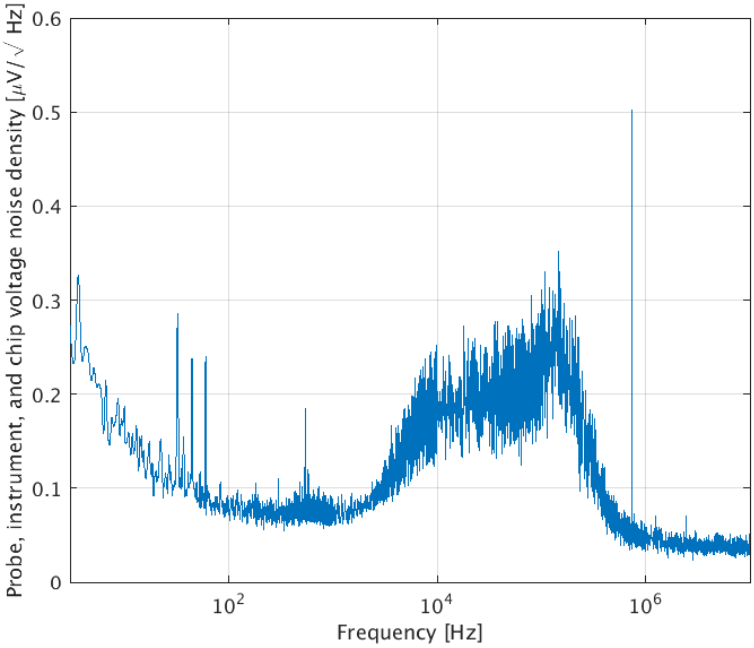


Figure 6.24: Measured total output voltage noise density of the integrated readout circuit. The measurement includes the noise of the active probe and the instrument.

6.3.3 Noise Behavior

The noise performance of the readout circuit is evaluated. The noise measurement is done in a shielded chamber. The output voltage noise density is measured by Agilent PXA N9030A which covers measurement in the range of 3 Hz to 26.5 GHz. An active probe (HP 1144) is used to derive the input impedance of the instrument. The measured total output voltage noise density of the integrated readout circuit is shown in Figure 6.24. To calculate the noise of the readout circuit, the noise of the instrument and the probe must be excluded. The measured voltage noise density of the probe and the instrument is shown in Figure 6.25. The equivalent noise charge of the readout circuit is calculated to be about 58 $\bar{e}$-rms according to the method explained in detail in Section 3.3. Table 6.2 summarizes the performance of the proposed readout circuit and compares it with relevant designs. The proposed design in [37] (2016) achieves a low-noise performance but the power

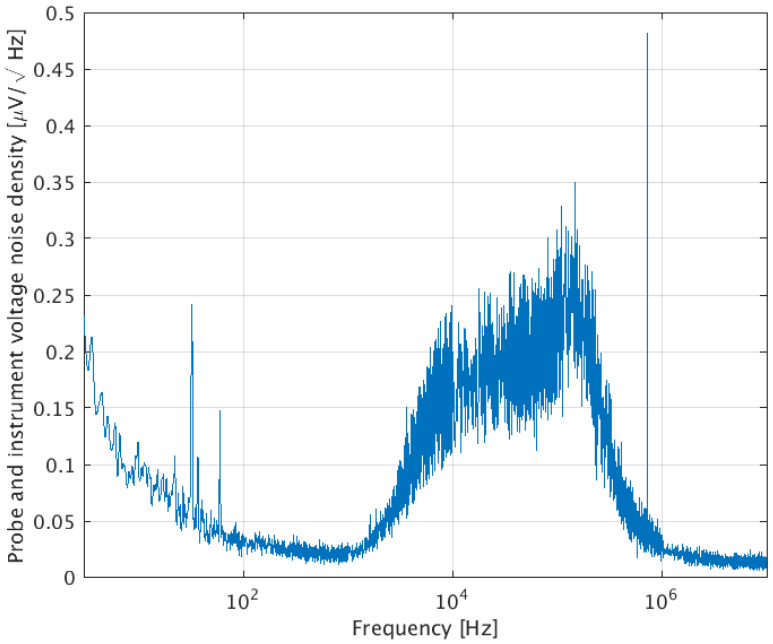


Figure 6.25: Measured voltage noise density of the active probe and the instrument.

consumption is high. The fabricated prototype integrated circuit achieves a good noise performance while the power consumption is kept at a low level. The analog circuits proposed in this work function with a supply voltage of 3.3 V for increasing the dynamic range of the input. As a result, the performance of the proposed ASIC can be compared with similar works in older technologies. The 0.18 μm ASIC proposed in [55] (2010) includes a shared pipelined ADC, but the achieved noise performance is too high for the consumed power. The proposed design in [35] (2015) has a high power consumption considering the fact that only a CSA, a first-order pulse shaper and a buffer are integrated on chip. The proposed designs in [170] (2014) and [44] (2010) achieve a good performance in terms of power consumption and noise, however, the integrated circuits do not include an ADC. The designed ASIC in [54] (2005) is intended for the readout of CZT CPG sensors. However, the ENC of the readout system is too high for the consumed power. The poor noise performance is mainly due to use of an n-type MOS device as the

input device of the CSA which has a higher flicker noise than a p-type device.

6.4 Summary and Conclusions

In this chapter, the detailed design and analysis of the pulse shaper and the signal processing blocks of a complete readout system for solid-state radiation detectors is presented. The design of the signal processing blocks of the readout signal requires design and simulation of mixed-signal circuits. The integrated readout system consists of a CSA with leakage compensation, a 5^{th}-order programmable Gaussian pulse shaper with a pole-zero cancellation circuit, a PDH, a discriminator, and a Wilkinson-based analog-to-digital converter. We presented and discussed the state-of-the-art designs of the main block of the system. As a proof of concept, a prototype chip that integrates the readout system is designed and fabricated in a 0.13-μm CMOS technology. To facilitate noise analysis, the equivalent noise charge equations are derived analytically. Measurements results of the prototype chip are presented which confirm the feasibility of the design. Noise measurement results show that the integrated readout system exhibits a lower noise as compared to the readout system designed in Chapter 5 thanks to the use of a higher order pulse shaper. The readout system performs favourably in terms of power consumption and noise behavior in comparison with similar works in the literature.

Table 6.2: Readout circuit performance comparison

Specification	This work	[37] (2016)	[35] (2015)	[170] (2014)	[55] (2010)	[44] (2010)	[54] (2005)
Fabrication process	0.13-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.35-μm CMOS	0.25-μm CMOS
Supply Voltage [V]	0.8, 1.2, 3.3	$\pm$1.5	-	-	1.8	$\pm$1.65	2.5
Signal processing chain	CSA, leakage compensation, PZC, 5^{th}-order programmable shaper, PDH, Discriminator, ADC	CSA, leakage compensation, filters, amplifier, PDH, discriminator, buffer	CSA, CR-RC shaper, buffer	CSA, fast and slow shapers, PZC, discriminator, memory	CSA, PZC, 2^{nd}-order shaper, comparator, DAC, shift register, decoder, pipeline ADC (shared)	CSA, PZC, fast/slow shaper, comparator, sample-and-hold	CSA, 5^{th}-order shaper, baseline holder, bandgap reference, discriminator
Detector capacitance [pF]	0.5	0.5	0.5	0.5	0	0.5	10
Peaking time [μs]	1.145	1.5	3	1.5	0.09	8	5
Charge gain [mV/fC]	1.96-7.87	200	4.9	65	-	100-300	18, 36
Power consumption per channel [mW]	1.97	8	2.8	3	3.8 (Channel), 4.5 (ADC)	3	>8.3
ENC [$\bar{e}$-rms]	58	73	137	91	> 200	93	500
Area per channel [mm^2]	0.44	0.34	0.33	0.65	0.02 (Channel), 0.02 (ADC)	0.7	>1.6

Chapter 7

Conclusions and Future Work

7.1 Research Summary and Contributions

The focus of this work has been on the design, analysis, and experimental result of integrated circuits for capacitive radiation detectors. We discussed the main aspects of designing a high performance readout system and explained the system- and circuit-level requirement as well as the trade-offs between them that need to be taken into account. The advantages and drawbacks of the available technologies for the integration of the system are reviewed. In order to achieve the highest performance, we presented the state-of-the-art designs of each block of the readout system. We compared the designs and discussed the advantages and drawbacks of each one.

To maximize the resolution of detection, we presented a comprehensive noise analysis of state-of-the-art capacitive detector readout circuits. The analysis takes into account the new noise sources associated with deep sub-micron technologies. It is based on the EKV model of MOS transistors, a model which is valid for all regions of operation. We showed that in deep sub-micron technologies the noise due to the gate leakage current cannot be neglected especially at large peaking times. In these processes the gate leakage current is strongly dependent on the drain-to-source voltage of the input MOS device when the device is biased in weak or moderate inversion regions. The noise analysis in this work confirms that the parallel noise sources must be accurately modelled when improving the resolution of

readout system implemented in an advanced CMOS process is concerned. We also discussed the practical aspects of noise measurement using various instruments.

As a proof of concept, the analysis and design of three interface circuits are presented. The proposed circuits are fabricated in a standard 0.13 μm CMOS process. The focus of the first developed interface circuit is on the design the charge-sensitive amplifier (CSA) block of a readout system. A novel CSA is proposed which consists of a regulated folded-cascode stage and a source follower buffer. A gain-boosting technique is employed in both upper and lower branches of the cascode stage of the CSA in order to enhance the overall gain of the amplifier with negligible overhead power consumption. The proposed CSA can accept signals of both polarities and consumes only 37.5 μW. The integrated interface circuit uses the proposed CSA, a pole-zero cancellation circuit, and a 2^{nd}-order semi-Gaussian programmable pulse shaper. The measured noise of the integrated circuit is 111 $\bar{e}$-rms. The second interface circuit consists of a CSA, a reset network, and a 1^{st}-order pulse shaper with a PZC circuit. The main focus of this work is on the noise analysis of readout systems for solid-state radiation detectors. The analytical equations for the estimation of the noise of the readout system are derived and the noise performance of the readout circuits are optimized. For a detector capacitance of 250 fF, the measured noise of the system varies between 66 to 101 $\bar{e}$-rms at four different peaking times. The power consumption of the circuit is about 1 mW. The third interface circuit consists of a CSA with leakage compensation, a 5^{th}-order programmable Gaussian pulse shaper, a peak-detect and hold, a discriminator, and an improved Wilkinson-based digitizer. This design focuses on the design of the pulse shaper and signal processing blocks of the readout system. Noise measurement results show that the integrated readout system exhibits only 58 $\bar{e}$-rms noise thanks to the use of a high-order pulse shaper. The readout system consumes about 1.97 mW. The design performs favourably in terms of power consumption and noise behavior in comparison with similar works in the literature.

7.2 Future Work

The performance of the proposed readout systems can be enhanced by further reducing the power consumption of the power-hungry analog blocks. In the readout

systems designed in this work, the same amplifier is used in the design of the pulse shapers, and the ADC. The overall power consumption of the readout circuits can be reduced significantly by designing amplifiers specific for the intended application. Furthermore, as modern readout systems integrate many readout channels, the power consumption of the integrated readout circuits can be further reduced by making the assumption that the ADC will be shared between more than one readout channel. In future work, the readout channel must be modified and a controller must also be designed to address the proposed changes. The number of output pins of the chip can also be further reduced by designing an I^2C or a serial interface for transferring the ADC digital codes to a personal computer for saving and further processing.

The proposed readout circuits in this work have been tested by injecting a controlled amount of charges into the circuit where an integrated capacitor simulates the behavior of the detector. The noise of the readout systems is also evaluated in a shielded chamber where no external noise is present. It is worth to evaluate the functionality of the readout systems with a detector attached. As the system will be exposed to radiation, such tests must be performed in special laboratories by trained individuals.

As the number of integrated readout channels in state-of-the-art designs is typically large and the available power budget for each readout channel is extremely limited, further research must be carried out to decrease the power consumption of each readout channel. Since most of ASICs consist of both analog and digital circuits, one possible solution is to use digital control circuits to whenever possible shut down or put into standby mode parts of the chip without compromising the performance. This solution could be very effective to reduce the overall power consumption specially when shutting down the power-hungry analog blocks is possible.

The advanced bulk CMOS technologies have enabled integration of highly densed and fast signal processing circuits on chip. This is particularly beneficial for implementing more functionalities (e.g., image processing) on the chip. Applications that require very high data rates also benefit from advancements in CMOS processes. Further research is needed to address the challenges of implementing the readout systems in these technologies. Some of the challenges include reduced

power supply voltage, increased mismatches and variations, radiation effects, and noise evaluation and modeling.

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Appendix A

Detailed Design of a 5^{th}-Order Gaussian Pulse Shaper

In this Appendix we describe the design of a 5^{th}-order Gaussian pulse shaper. Let's assume that the pulse shaper has one real pole and two complex pairs. The block diagram of the pulse shaper is shown in Figure A.1. The transfer function of the pulse shaper can be written as

$$H(s) = \frac{A_0}{\sigma s + A_0} \frac{(A_1^2 + W_1^2)}{(\sigma s + A_1)^2 + W_1^2)} \frac{(A_2^2 + W_2^2)}{(\sigma s + A_2)^2 + W_2^2)}, \tag{A.1}$$

where σ is the rms deviation of the normal distribution. The pole locations of the filter (i.e., A_0, A_1, A_2, W_1, and W_2) are given in Table A.1 according to [161]. The real pole can be synthesized using a simple differentiator followed by a buffer. Equating the locations of the real poles

$$s = \frac{-A_0}{\sigma} = \frac{-1}{R_0 C_0}, \tag{A.2}$$

results in the following equation.

$$R_0 C_0 = \frac{\sigma}{A_0} \tag{A.3}$$

The complex pairs of poles can be synthesized using the active filters shown in

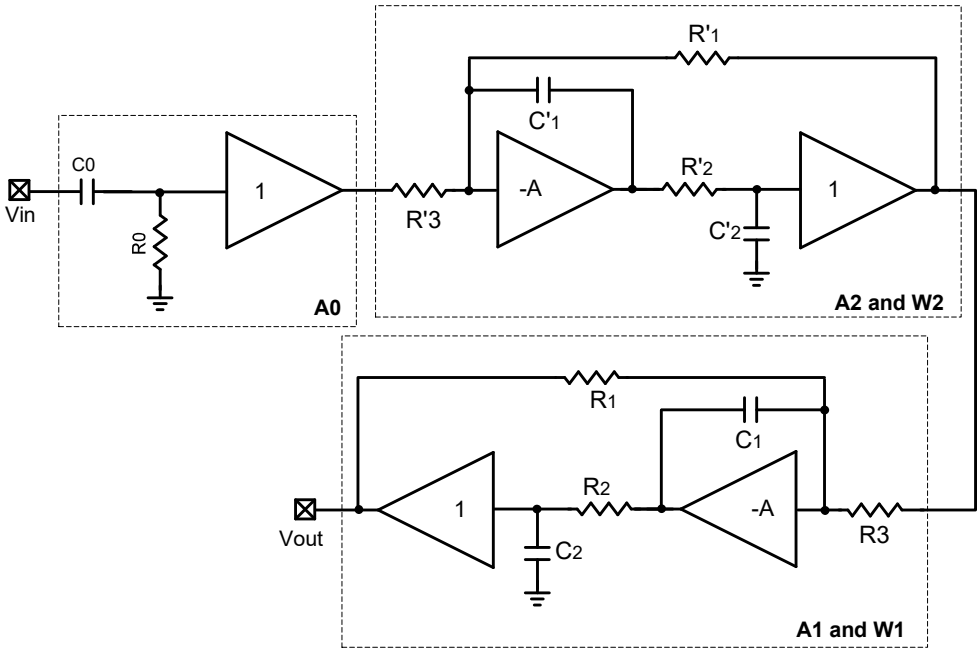

Figure A.1: Block diagram of a 5^{th}-order Gaussian pulse shaper

Figure 6.2. The transfer function of the active filter is given by [161]

$$H(s) = \frac{\frac{-R_1}{R_3}}{R_1R_2C_1C_2s^2 + R_1C_1s + 1} \tag{A.4}$$

The active filter has a pair of complex poles given by

$$s = (\frac{1}{2R_2C_2}) - 1 \pm j\sqrt{(\frac{4R_2C_2}{R_1C_1} - 1)}. \tag{A.5}$$

Equating the location of the first pair of poles in equations A.1 and A.5

$$s = \frac{-A_1}{\sigma} \pm j\frac{W_1}{\sigma} = (\frac{1}{2R_2C_2}) - 1 \pm j\sqrt{(\frac{4R_2C_2}{R_1C_1} - 1)} \tag{A.6}$$

results in the following equations.

$$A_1 = \frac{\sigma}{2R_2C_2} \tag{A.7}$$

Table A.1: Pole locations of the 5^{th}-order pulse shaper

Parameter	Value
A_0	1.4766878
A_1	1.4166647
W_1	0.5978596
A_2	1.2036832
W_2	1.2994843

and

$$W_1 = \frac{\sigma}{2R_2C_2}\sqrt{(\frac{4R_2C_2}{R_1C_1} - 1)} \tag{A.8}$$

We have set $R_1 = R_2$ in our design. The value of the capacitor C_2 can be calculated using equations (A.7) and (A.3) as

$$C_2 = \frac{2R_2}{A_1}\sigma = \frac{2R_2}{A_1}A_0R_0C_0. \tag{A.9}$$

The value of capacitor C_1 can be calculated using equations (A.8), (A.7), and (A.9) as

$$C_1 = \frac{4R_2C_2}{R_1}\frac{1}{(\frac{W_1}{A_1})^2 + 1} = \frac{8R_2}{A_1}\frac{A_0R_0C_0}{(\frac{W_1}{A_1})^2 + 1}. \tag{A.10}$$

Similar equations can be derived for the second pair of poles.

Appendix B

Verilog Model for the Conversion Controller Block of the Complete Readout System

```
//Verilog HDL for the "Conversion_Controller" block

// clk freq.: 25 MHz
// List of Circuit I/Os:
// clr: asynchronous clear, negative edge-triggered
// clk: clock signal, negative edge-triggered
// Vdiscr: Input signal from the discriminator
// ADC_output_ready: Input signal from the ADC showing end of conversion
// Discr_reset: output signal to reset the discriminator
// ADC_start: output signal to ADC to start the conversion
// PDH_reset: output signal to reset the PDH
// PDH_W: output signal to PDH to enable tracking (Write phase)
// PDH_R: output signal to PDH to enable reading (Read phase)

// The following module generates the timing signals for the
// peak-detect and hold, Discriminator and ADC.
```

```
module Conversion_Controller(clk, clr, Vdiscr, ADC_output_ready,
Discr_reset, ADC_start, PDH_reset, PDH_W, PDH_R); // definition of the module

input clk, clr, Vdiscr, ADC_output_ready;
output Discr_reset, ADC_start, PDH_reset, PDH_W, PDH_R;

reg Discr_reset, ADC_start, PDH_reset, PDH_W, PDH_R;
reg [3:0] state; // state register

parameter zero=0, one=1, two=2, three=3, four=4, five=5, six=6,
seven=7, eight=8, nine=9, ten=10, eleven=11, twelve=12, thirteen=
13, fourteen=14, fifteen=15;

always @(state)
        begin
                case (state)
                        zero:
                                begin
                                        PDH_W=0;
                                        PDH_R=0;
                                        PDH_reset=1;
                                        Discr_reset=1;
                                        ADC_start=0;
                                end
                        one:
                                begin
                                        PDH_W=1;
                                        PDH_R=0;
                                        PDH_reset=0;
                                        Discr_reset=0;
                                        ADC_start=0;
                                end
                        two:
```

```
        begin
                PDH_W=1;
                PDH_R=0;
                PDH_reset=0;
                Discr_reset=0;
                ADC_start=0;
        end
three:
        begin
                PDH_W=0;
                PDH_R=0;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=0;
        end
four:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
five:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
six:
        begin
```

```
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
seven:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
eight:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
nine:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
ten:
        begin
                PDH_W=0;
```

```
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
eleven:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
twelve:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
thirteen:
        begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
        end
fourteen:
        begin
                PDH_W=0;
                PDH_R=1;
```

```
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=1;
            end
        fifteen:
            begin
                PDH_W=0;
                PDH_R=1;
                PDH_reset=0;
                Discr_reset=1;
                ADC_start=0;
            end
        default:
            begin
                PDH_W=0;
                PDH_R=0;
                PDH_reset=1;
                Discr_reset=1;
                ADC_start=0;
            end
    endcase
end

always @(negedge clk or negedge clr)
    begin
        if (clr==0)
            state = zero; // initial state
        else
            case (state)
                zero:
                    state = one;
                one:
                    if (Vdiscr==1) // if the discriminator output is high
```

```
then change the state to state two otherwise stay in state one
                    state = two;
                else
                    state = one;
            two:
                if (Vdiscr==0) // if the discriminator output is low
then change the state to state three otherwise stay in state two
                    state = three;
                else
                    state = two;

        three:
            state = four;

        four:
            state = five;

        five:
            state = six;

        six:
            state = seven;

        seven:
            state = eight;

        eight:
            state = nine;

        nine:
            state = ten;

        ten:
```

```
                state = eleven;

            eleven:
                state = twelve;

            twelve:
                state = thirteen;

            thirteen:
                state = fourteen;

            fourteen:
                state = fifteen;

            fifteen:
                if (ADC_output_ready==1) // wait for the ADC_output_ready
                signal
                        state = zero;
                else
                        state = fifteen;

        endcase
    end

endmodule
```

Appendix C

Verilog Model for the Controller Block of the Wilkinson-Based ADC

```
//Verilog HDL for the Control block of the ADC

// clk freq.: 25 MHz

// Input/Output ports:
// clk: global clock
// clr: clear signal, negedge-triggered
// start: start signal is generated by the output of the comparator.
// Start is '1' when the shaper's output is higher than a
//reference voltage
// ADC_ctrl: a timing signal generated by the state machine to
// control the sampling and conversion
// output_ready: shows the end of conversion
// Count: Conversion results (9 bits)
// Vcomp: Comparator output

module ADC_controller(clk, clr, start, Vcomp, ADC_ctrl,output_ready, Count);
```

```
input clk, clr, start, Vcomp;
output ADC_ctrl, output_ready;
output [8:0] Count;

wire Counter_overflow, Counter_CLR, Counter_en;
wire Counter_en_FSM, Counter_CLR_FSM;

counter_9bits counter(clk, Counter_CLR, Counter_en, Count, Counter_overflow);
//9-bit counter
statem state_machine(clk, rst, start, Counter_overflow, Vcomp, ADC_ctrl, output_ready,
Counter_CLR_FSM, Counter_en_FSM);
//state machine

and (Counter_en, Counter_en_FSM, Vcomp);
or (Counter_CLR, Counter_CLR_FSM, clr);
not (rst, clr);
endmodule


//////////////////////////////////////////////////////////////
////////////////////// Counter //////////////////////////////
//////////////////////////////////////////////////////////////

// clr: asynchronous clear, active low
// clk: clock, negedge-triggered
// out: Count results
// overflow: overflow

module counter_9bits (clk, clr, en, out, overflow);
input clk, clr, en;
output [8 : 0] out;
reg [8 : 0] tmp;
```

```
output overflow;
always @(negedge clk or negedge clr)
        begin
                if (clr==0)
                        tmp = 0;
                else if (en)
                        tmp = tmp + 1;
        end
assign out = tmp;
assign overflow = (tmp == 9'b111111111);
endmodule

//////////////////////////////////////////////////////////
////////////////////// state machine ////////////////////////
//////////////////////////////////////////////////////////

module statem(clk, clr, start, Counter_overflow, Vcomp, ADC_ctrl,
output_ready, Counter_CLR, Counter_en);

input clk, clr, start, Counter_overflow, Vcomp;
output ADC_ctrl, output_ready, Counter_CLR, Counter_en;

reg ADC_ctrl, output_ready, Counter_CLR, Counter_en;
reg [1:0] state;

parameter zero=0, one=1, two=2, three=3;

always @(state)
        begin
                case (state)
                        zero:
                                begin
                                        ADC_ctrl=1;
```

```
                output_ready=0;
                Counter_CLR=0;
                Counter_en=0;
            end
        one:
            begin
                ADC_ctrl=1;
                output_ready=0;
                Counter_CLR=1;
                Counter_en=0;
            end
        two:
            begin
                ADC_ctrl=0;
                output_ready=0;
                Counter_CLR=0;
                Counter_en=1;
            end
        three:
            begin
                ADC_ctrl=1;
                output_ready=1;
                Counter_CLR=0;
                Counter_en=0;
            end
        default:
            begin
                ADC_ctrl=1;
                output_ready=0;
                Counter_CLR=0;
                Counter_en=0;
            end
endcase
```

```
        end

always @(posedge clk or posedge clr)
        begin
                if (clr)
                        state = zero;
                else
                        case (state)
                                zero:
                                        if (start)
                                                state = one;
                                        else
                                                state = zero;
                                one:
                                        if (start==0 && Vcomp==0)
                                                state = three;
                                        else if (start==0)
                                                state = two;
                                                else
                                                        state = one;
                                two:
                                        if (Counter_overflow || (Vcomp==0))
                                                state = three;
                                        else
                                                state = two;
                                three:
                                        state = zero;

                        endcase
        end

endmodule
```

Appendix D

Developed Software Program for Automating the ADC Data Collection

In this Appendix we present how to use National Instruments' Virtual Instrument Software Architecture (VISA) to control any message-based hardware. VISA can be used to configure, program, or troubleshoot instruments comprising USB, Serial, GPIB, VXI, PXI, or Ethernet interfaces. In our work we used VISA to control Rigols DP832A power supply to generate a ramp signal. A software is developed in C# in Microsoft Visual Studio .Net environment which uses the VISA .NET library for communicating with the instrument. The software also communicates with a microcontroller over a serial communication protocol. The microcontroller sends the measured ADC counts to the software for storage and processing. It also sends commands to the software to set the voltage on the instrument. To use the VISA protocol in Microsoft Visual Studio .Net environment, the corresponding libraries must be first installed. They can be downloaded from the National Instruments website. The software can be controlled through a simple graphical user interface (GUI). The GUI has two buttons. The first button creates a message-based session and the second one closes the session. The developed source code is given below.

```
using System;
```

```
using System.Windows.Forms;
using System.IO.Ports;
using NationalInstruments.Visa;

namespace NationalInstruments.VISA.VISA_MCU_Interface
{

public class MainForm : System.Windows.Forms.Form
{
        private MessageBasedSession mbSession;
        private System.Windows.Forms.Button openSessionButton;
        private System.Windows.Forms.Button closeSessionButton;

        private System.ComponentModel.Container components = null;

        public MainForm()
        {
                InitializeComponent();
                SetupControlState(false);

                // connect to the microcontroller over a serial port
                // to receive the commands
                // Microcontroller is connected to COM4 port
                SerialPort mySerialPort = new SerialPort("COM4");
                mySerialPort.BaudRate = 115200; // baud rate
                mySerialPort.Parity = Parity.None; // no parity
                mySerialPort.StopBits = StopBits.One; // one stop bit
                mySerialPort.DataBits = 8; // 8 bits data
                // no handshaking
                mySerialPort.Handshake = Handshake.None;
                mySerialPort.RtsEnable = true; // RTS enabled
                mySerialPort.DataReceived += new SerialDataReceivedEventHandler(DataReceivedHandler);
                mySerialPort.Open(); // open the port
```

```
        }
        private void DataReceivedHandler(object sender, SerialDataReceivedEven-
tArgs e)
        {
                SerialPort sp = (SerialPort)sender;
                // file name and path to write the measurement data
                string filename = "C:\ADC_Measurement_Results.txt";
                System.IO.StreamWriter objWriter;
                objWriter = new System.IO.StreamWriter(filename, true);
                // get the command from the microcontroller
                string indata = sp.ReadLine();
                // if Start command is received
                if (indata.Contains("Starting"))
                {
                        sp.DiscardInBuffer(); // discard the input buffer
                }
                // else if set voltage command is received
                else if (indata.IndexOf("Set Vin to:") == 0)
                {
                        int temp = indata.IndexOf("\r");
                        try
                        {
                                // parse the voltage to set
                                string Vin = indata.Substring(11, temp - 11);
                                //Convert the voltage to Volts
                                double Vin_double = Convert.ToDouble(Vin) / 1000;

                                // if voltage to set is lower than 3.3V,
                                // set the voltage on the power supply
                                if (Vin_double <= 3.3)
                                {
                                        string s1 = ":VOLT " + Vin_double.ToString() +
```

```
”\n”;
                                    string textToWrite = ReplaceEscSeq(s1);
                                    mbSession.RawIO.Write(textToWrite);
                                }

                        }
                        catch
                        {
                                indata = ”Could not set the voltage properly! Input data
is:” + indata;
                                // write the error message to the file
                                objWriter.WriteLine(indata);
                        }
                }
                else
                {

                // else write the received measurement data to the file
                        objWriter.Write(indata);
                }
                objWriter.Close(); // close the file

        }
        protected override void Dispose( bool disposing )
        {
                if(disposing)
                {
                        if(mbSession != null)
                        {
                                mbSession.Dispose();
                        }
                        if (components != null)
                        {
```

```
                components.Dispose();
            }
        }
        base.Dispose( disposing );
    }

    #region Windows Form Designer generated code
    private void InitializeComponent()
    {
        System.ComponentModel.ComponentResourceManager resources =
new System.ComponentModel.ComponentResourceManager(typeof(MainForm));
        this.openSessionButton = new System.Windows.Forms.Button();
        this.closeSessionButton = new System.Windows.Forms.Button();
        this.SuspendLayout();
        //
        // openSessionButton
        //
        this.openSessionButton.Location = new System.Drawing.Point(106,101);
        this.openSessionButton.Name = ”openSessionButton”;
        this.openSessionButton.Size = new System.Drawing.Size(110,25);
        this.openSessionButton.TabIndex = 0;
        this.openSessionButton.Text = ”Open Session”;
        this.openSessionButton.Click += new System.EventHandler(this.openSession_Click);
        //
        // closeSessionButton
        //
        this.closeSessionButton.Location = new System.Drawing.Point(106,155);
        this.closeSessionButton.Name = ”closeSessionButton”;
        this.closeSessionButton.Size = new System.Drawing.Size(111,25);
        this.closeSessionButton.TabIndex = 1;
        this.closeSessionButton.Text = ”Close Session”;
        this.closeSessionButton.Click += new System.EventHandler(this.closeSession_Click);
        //
```

```
        // MainForm
        //
        this.AutoScaleBaseSize = new System.Drawing.Size(6,15);
        this.ClientSize = new System.Drawing.Size(336,318);
        this.Controls.Add(this.closeSessionButton);
        this.Controls.Add(this.openSessionButton);
        this.Icon = ((System.Drawing.Icon)(resources.GetObject("$this.Icon")));
        this.MaximizeBox = false;
        this.MinimumSize = new System.Drawing.Size(354,365);
        this.Name = "MainForm";
        this.StartPosition = System.Windows.Forms.FormStartPosition.CenterScreen;
        this.Text = "VISA MCU";
        this.ResumeLayout(false);

}
#endregion


[STAThread]
static void Main()
{
        Application.Run(new MainForm());
}

private void openSession_Click(object sender, System.EventArgs e)
{
        // create a message-based session
        using (SelectResource sr = new SelectResource())
        {
                // resoure name
                sr.ResourceName = "USB0::0x1AB1::0x0E11::DP8C182401945::INSTR";
                using (var rmSession = new ResourceManager())
                {
```

```
                mbSession = (MessageBasedSession)rmSession.Open(sr.ResourceName);
                SetupControlState(true);
            }
        }

        // select CH3 of the power supply
        string s1 = ":INST CH3\n";
        string textToWrite = ReplaceEscSeq(s1);
        mbSession.RawIO.Write(textToWrite);
        // set the voltage on CH3 to 3.3V
        s1 = ":VOLT 3.3\n";
        textToWrite = ReplaceEscSeq(s1);
        mbSession.RawIO.Write(textToWrite);
        // enable the output of CH3
        s1 = ":OUTP CH3,ON\n";
        textToWrite = ReplaceEscSeq(s1);
        mbSession.RawIO.Write(textToWrite);
}

private void closeSession_Click(object sender, System.EventArgs e)
{
        SetupControlState(false);
        mbSession.Dispose();
}

private void SetupControlState(bool isSessionOpen)
{
        openSessionButton.Enabled = !isSessionOpen;
        closeSessionButton.Enabled = isSessionOpen;
}

private string ReplaceEscSeq(string str)
{
```

```
            return str.Replace("\\n", "\n").Replace("\\r", "\r");
        }

        private string InsertEscSeq(string str)
        {
            return str.Replace("\n", "\\n").Replace("\r", "\\r");
        }
}
}
```