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MASTER'S THESIS

DESIGN AND IMPLEMENTATION OF LEAKY WAVE ANTENNA CONTROL CIRCUIT

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ABSTRACT

Wireless communication research is seeking new methods to increase the performance of the communications systems. Traditional ways to increase the data rate with higher transmission power or smaller cell size of the network have diminishing returns. Adding more transmitter and receiver antennas is a trend in next generation wireless systems. RLWA (Reconfigurable Leaky Wave Antenna) systems have been introduced to be an alternative way of increasing the performance of communications systems. Therefor research of RLWA integration as part of the already working wireless systems is important.

This thesis is a design and implementation work of RLWA control circuit. Designed circuit is aimed to be the bridge between the antenna element and WARP (Wireless Open-Access Research Platform). Operation theories of used integrated circuits such as step-up converters, operational amplifiers and digital to analog converters are discussed.

Design process of the control circuit is explained in detail. Schematic and PCB (Printed Circuit Board) are designed using Cadsoft Eagle software. Implemented device is using 12 V DC power supply. Antenna input consists of two analog control signals from 10 V to 30 V. Control circuit input consists of two 8 bit digital signals. Transient analysis simulations are included for the designed circuit parts using Matlab and LTSpice software. Implementation of the design is verified in practice with test setup. Measurement results from the test setup are presented.

Key words: Reconfigurable Leaky Wave Antenna, Wireless Open-Access Research Platform, Circuit Design, Digital to Analog Conversion.

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TIIVISTELMÄ

Langattoman tietoliikenteen tutkimus on etsimässä uusia keinoja tiedonsiirtojärjestelmien suorituskyvyn parantamiseen. Tiedonsiirtonopeuden kasvattaminen perinteisillä menetelmillä kuten kasvattamalla lähetystehoa tai pienentämällä verkon solukokoa ei ole enää yhtä tehokasta, koska ylläpitokustannukset kasvavat ja häiriösignaalin taso nousee suhteessa kohinaan. Lähetys- ja vastaanottoantennien lukumäärän lisääminen tulee olemaan yksi käytetyistä keinoista seuraavan sukupolven langattomissa tietoliikennejärjestelmissä. RLWA (Reconfigurable Leaky Wave Antenna) –järjestelmien avulla voidaan toteuttaa vaihtoehtoinen tapa parantaa tiedonsiirtojärjestelmien suorituskykyä. Tämän takia on tärkeää tutkia RLWA:n yhdistämistä jo toimivaan langattomaan järjestelmään.

Tässä diplomityössä suunnitellaan ja toteutetaan RLWA:n ohjauspiiri. Suunniteltu piiri toimii siltana antennielementin ja langattoman avoimen kehitysalustan välillä. Työssä tarvittavien integroitujen piirien, kuten jänniteregulaattorin, operaatiovahvistimien ja digitaali-analogiamuuntimien toimintaperiaatteet käydään läpi.

Ohjauspiirin suunnittelutyö selitetään yksityiskohtaisesti. Kytkentäkaavio ja PCB (Printed Circuit Board) suunnitellaan käyttäen Cadsoft Eagle sovellusta. Toteutettu laite käyttää 12 V DC virtalähdettä. Laitteen sisääntulo koostuu kahdesta 8 bittisestä digitaalisesta signaalista. Laite syöttää 10 V – 30 V analogista signaalia antennille. Suunnitelluille piirin osille tehtiin simulaatioita käyttäen transientti analyysiä Matlab ja LTSpice ohjelmistoilla. Toteutetun laitteen toiminta varmennetaan liittämällä se osaksi WARP:ia (Wireless Open-Access Research Platform). Koekytkennän mittaustulokset esitellään.

Avainsanat: muunneltava leaky wave –antenni, langattomien tiedonsiirtomenetelmien kehitysalusta, digitaali-analogiamuunnos, piirisuunnittelu.

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PREFACE

"To achieve great things, two things are needed: a plan, and not quite enough time."
- Leonard Bernstein

This master thesis was done for the CWC (Centre for Wireless Communications) in Wireless Networking Lab. The purpose of this thesis was to design and implement an antenna control board for WARP. Antenna control board replaces an old design and allows further research with reconfigurable antenna systems.

I would like to thank my thesis supervisor Lic.Tech. Risto Vuohtoniemi for the advices and help he gave me along the writing process and secondary examiner Dr. Sc. Juha-Pekka Mäkelä for his insight. I would like to thank my instructor M. Sc. Markku Jokinen for all the support in the implementation process, Mr. Martti Huttunen and Professor Kari Määttä for the practical design advices. Also I would like to thank all the team members of WNL, the team leader M. Sc. Tuomo Hänninen and other CWC employees for the assistance in the thesis work.

I would like to thank my parents Mika and Pirkko for the endless support and care they managed to give me along the way to this point, I wouldn't be here without them. Finally I would like to thank all my old and new friends for all the good times.

Oulu, 1. December 2014

Jaakko Nevala

LIST OF SYMBOLS AND ABBREVIATIONS

CMC	Center Multimedia Communications
CRLH	Composite Left-Right Hand
CWC	Centre for Wireless Communications
DAC	Digital to Analog Converter
DC	Direct Current
ERAS	Electrically Reconfigurable Antenna System
ESR	Electrical Series Resistance
FET	Field Effective Transistor
FPGA	Field Programmable Gate Array
GPP	General Purpose Processor
I/O	Input-Output
IEEE	Institute of Electrical and Electronics Engineers
LED	Light Emitting Diode
MGT	Multi-Gigabit Transceiver
MIMO	Multiple Input Multiple Output
OTA	Over-The-Air
PC	Personal Computer
PCB	Printed Circuit Board
PLL	Phase Locked Loop
RF	Radio Frequency
RLWA	Reconfigurable Leaky Wave Antenna
RSSI	Received Signal Strength Indicator
RX	Receiver
SDR	Software Defined Radio
SISO	Single Input Single Output
SMA	SubMiniature version A
SPICE	Simulation Program with Integrated Circuit Emphasis
TL	Transmission Line
TX	Transmitter
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver/Transmitter
WARP	Wireless Open-Access Research Platform
WLAN	Wireless Local Area Network

C_i	capacitance of capacitor *i*
D	duty cycle
d	unit cell length
f_c	crossover frequency
f_{sw}	switching frequency
I_{IN}	total input current
I_{LOAD}	load current
L_i	inductance of inductor *i*
P_{TOT}	total input power
R_i	resistance of resistor *i*
U_i	operational amplifier *i*
ΔV_{P-P}	voltage ripple
V_{in}	input voltage

V_{out}	output voltage
V_{ref}	reference voltage
ϵ_r	dielectric constant

1. INTRODUCTION

Wireless communication networks are being studied actively nowadays. Modern society demands higher data rates for higher amount of users. A single user data rate can be increased by allocating more power to the transmitter and receiver elements to achieve higher signal-to-noise ratio. However, when the wireless network cell has multiple users and a high amount of available power resources, interference can become the dominating factor compared to the channel noise. The interference can be effectively reduced with intelligent digital signal processing algorithms and antenna null steering systems. [1, 2]

Next generation wireless networks attempt to use radio spectrum more efficiently since the radio spectrum is a limited resource and the amount of used spectrum bandwidth is already high. Efficient usage can be achieved through spectrum sensing systems. The accuracy of spectrum sensing can be improved with electrically reconfigurable antenna systems (ERAS). This can be achieved by exploiting the antenna pattern and polarization diversity. [3]

MIMO systems (Multiple Input Multiple Output) where multiple antennas are used in the transmitter and the receiver are being integrated into the new wireless communications systems. MIMO systems achieve better performance compared to the SISO systems (Single Input Single Output) by increasing the system capacity and reliability. [4]. Further analysis suggests that reconfigurable antennas can distribute and collect the energy used in the MIMO communication systems more efficiently compared to the traditional passive antenna elements. According to [5, 6], reconfigurable MIMO system can use the propagation channel more efficiently without disadvantages like complex coding or higher transmitted power according to the research.

Future research on the reconfigurable antenna systems requires more analytic results regarding the real life test environment. Integrating a software radio research platform with the reconfigurable antenna requires a separate controller device. This thesis work provides means for further research on reconfigurable antenna systems by developing control electronics for an electronically steerable antenna. The developed control device allows implementation of real life measurement scenarios where active antenna beamforming, is introduced into wireless reconfigurable MIMO systems.

In this thesis, we introduce a design and implementation of a leaky wave antenna control circuit that replaces and simultaneously improves the performance of an older version of the control circuit. The designed circuit is first simulated as accurately as possible to ease the implementation process by introducing as many real world non-idealities as possible. The implementation part of the work includes a PCB layout design and reflow soldering of the components. The implemented board is finally verified with thorough electrical circuit tests and antenna radiation pattern measurements to ensure the proper operation of the designed system.

This thesis has the following structure. Chapter 2 presents the used hardware and software in the system. Specifications for the antenna control circuit are introduced. Chapter 3 focuses on the circuit components used in the controller. Operation principles of a boost converter and specific operational amplifier design are introduced. Chapter 4 presents detailed design work of the controller. Simulations are presented to support the design. Chapter 4 focuses on the measurements of the system setup. Discussion and summary are in Chapter 5 and Chapter 6.

2. WIRELESS OPEN-ACCESS RESEARCH PLATFORM

Wireless Open-Access Research Platform (WARP) system is a custom made user reprogrammable wireless test platform. Idea of WARP is to combine theoretical research with the real hardware to a flexible test environment. The WARP project was founded at the Center for Multimedia Communications (CMC), Rice University. The hardware has been designed by the employees of Rice University. Since WARP is an open source platform, it can be used in educational and research projects. This platform can be programmed to perform as a prototype of an advanced wireless network. Implementation of Orthogonal Frequency Division Multiplexing (OFDM) physical layer is included in the reference design.

It is possible to use WARP with WARPLab framework and Reconfigurable Leaky Wave Antenna (RLWA) to research benefits of ERAS. Designing and implementation of an antenna controller, which connects the previously mentioned systems is presented of this thesis.

2.1. Directional antennas

Omnidirectional antennas are characterized with the doughnut shaped radiation pattern, which covers 360° angle with stable gain in horizontal plane. Power is divided evenly for each direction. Typical application area for omnidirectional antenna is a mobile device, which has small physical size and non-stationary location. Directional antenna has non-circular radiation pattern. Gain is focused in one or several directions. Directional antennas are used mainly in base stations and satellite communications. Size of a directional antenna is typically so large that including it to a wireless mobile device is problematic. Radio-frequency identification readers typically have directional antennas to keep a high antenna energy efficiency. [7]

Directional antennas have several benefits as opposed to the omnidirectional antennas depending on the specifications of the application. Wireless ad hoc networks consists of several nodes, which are able to communicate between each other. By using directive antennas in wireless ad hoc networks, less interference is produced than when using the omnidirectional antennas. This allows several simultaneous transmissions between nodes, which increases the total network capacity. Transmission is more energy efficient since the required gain can be achieved with lower total transmission power. Maximum transmission range increases as well if the maximum allocated power is equal when using omnidirectional antennas. Although, replacing the omnidirectional antennas in existing ad hoc networks would not be beneficial without redesigning the network entirely. For example, widely used medium access layer IEEE 802.11 in WLAN (Wireless Local Area Network) doesn't take account the usage of directional antennas [8]. Omnidirectional antennas, on the other hand, do not require intelligent position planning or directional adjustments so the architecture of the layer is easier to design. Transmission is not depended on the position of the mobile device, because there are no dead angles when using omnidirectional antennas. This requires less design work and actual products are cheaper to manufacture. [7, 9]

Directional antennas can be divided into categories by how the radiation is generated. Materials and the structure changes between different antenna types. Travelling wave antenna propagates a travelling wave along the antenna structure. Speed of the guided travelling wave can be controlled by different structure designs.

If the phase velocity of the travelling wave is slower than the speed of light in free space, the travelling antenna considered as a slow-wave antenna. Fast-wave antennas, also known as leaky wave antennas, are travelling wave antennas where travelling wave phase velocity is higher than the speed of light in free space.

Leaky wave antennas offer simple feeding, high directivity and frequency beam scanning capability [10]. The leaky wave antennas can be divided into different categories by the structure and characteristics of the antenna. Transmission line leaky wave antennas are composed from units cells. Special case, where transmission line is constructed from materials with negative permittivity and permeability is called left handed transmission line. Left handed transmission line structure is presented by a shunt capacitor and a series inductor, which resembles a low pass filter. Right handed transmission line structure is the opposite; a shunt inductor and series capacitor circuit. The right and left handed transmission line circuits are shown in Figure 2.1. Unit cell length is represented with *d*. By combining these two structures, a CRLH (Composite Right/Left Handed) transmission line is formed. Constructing an antenna with multiple CRLH unit cells allows effective beam-scanning in the horizontal plane. Beam angle is now dependent on the input frequency. Further on, to allow electrically controlled transmission line with the beam-scanning capability, a varactor diode structure is designed. By changing biasing voltage of the varactor diode, capacitance of the CRLH circuit can be adjusted so that the radiated energy direction steers in the horizontal plane. [11, 12, 13]

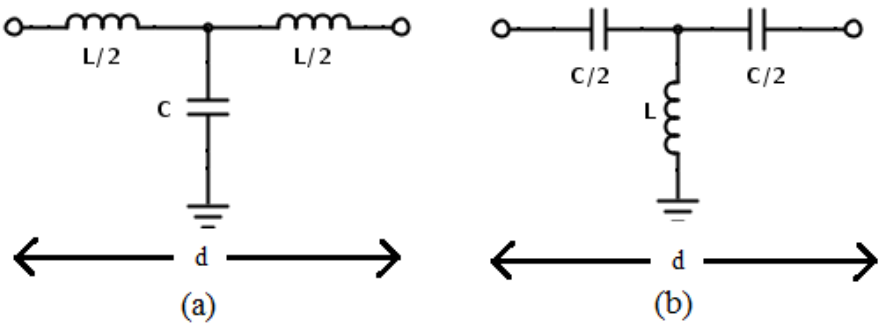

Figure 2.1. (a) Right handed transmission line (b) Left handed transmission line.

2.2. System setup structure

General Purpose Processor Software Defined Radio (GPP-SDR) with antenna beam steering setup can be constructed with the hardware and software introduced bellow. The user can implement a custom signal processing and integrate the beam steering to be a part of the process.

The system structure of the GPP-SDR is shown in Figure 2.2. The user PC is connected to the WARP board via Ethernet connection so WARPLab framework can easily interact with the WARP board. This allows, for example, steering the beam of the RLWA with the antenna controller. The radio card is connected to the Field Programmable Gate Array (FPGA) via digital I/O connection. Transceiver on the radio card is controlled by the radio controller. [14]

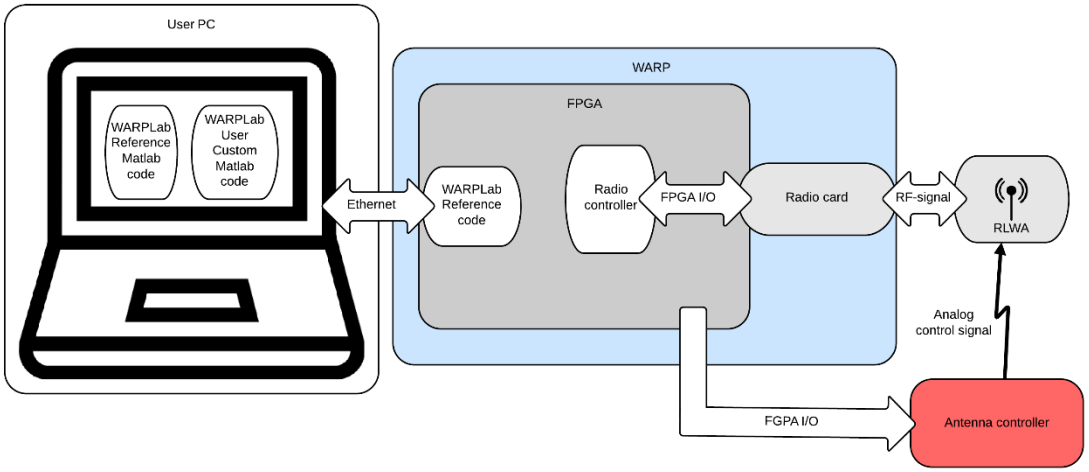

Figure 2.2. GPP-SDR system structure.

2.3. FPGA board

FPGA is the core of the WARP board. The board is built around Xilinx Virtex FPGA device which includes two PowerPC processors. Variety of different connection types are available such as Multi-Gigabit Transceiver (MGT), USB, Ethernet, RS-232 UART and +3.3 V 16 bit digital I/O. The board includes 7-segment displays and push buttons for further user I/O activity. Several daughter cards can be attached to the WARP board such as radio-, clock-, AD/DA- or custom I/O-cards. The board uses 12 V DC power supply. WARP project includes a framework for accessing radio link using Matlab-software with user PC. The WARP board is shown in Figure 2.3. [14]

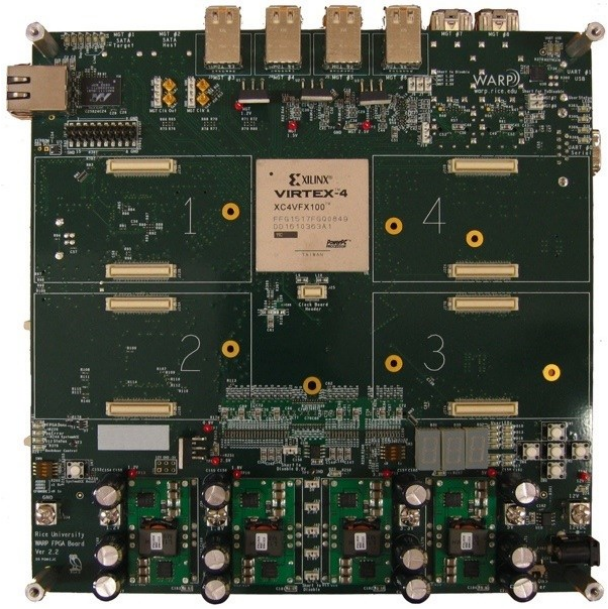

Figure 2.3. WARP board.

2.4. Radio board

The radio board in the WARP platform is a dual-band direct-conversion transceiver. The transceiver structure is shown in Figure 2.4. Receiver parts are marked with blue color and transmitter parts with red color. The digital-to-analog converter of the transmitter is fed with separate I and Q parts of the signal from the TX buffer. Signals are amplified in the baseband before the upconversion to the radio frequency is performed. Local oscillator signals are generated using a Phase Locked Loop (PLL) which ensures a stable frequency and eliminates possible phase errors. RF-signal is amplified and then send to the antenna. [14]

The receiver structure performs pre amplification, down conversion, base-band amplification and analog-to-digital conversion for the received signal. The receiver measures also the received signal strength and transforms it to digital signal along with the I and Q parts of the data signal. Radio board has a dual-band MAX2829 transceiver circuit. It supports radio frequencies from 2.4 GHz to 2.5 GHz and from 4.9 GHz to 5.875 GHz. Radio board is connected to the FPGA board using two 80 bit data headers. Two SubMiniature version A (SMA) connectors are included in the board for coaxial RF connections. The transceiver is MIMO capable and supports up to 40 MHz signal bandwidth. The radio board is shown in Figure 2.5. [14]

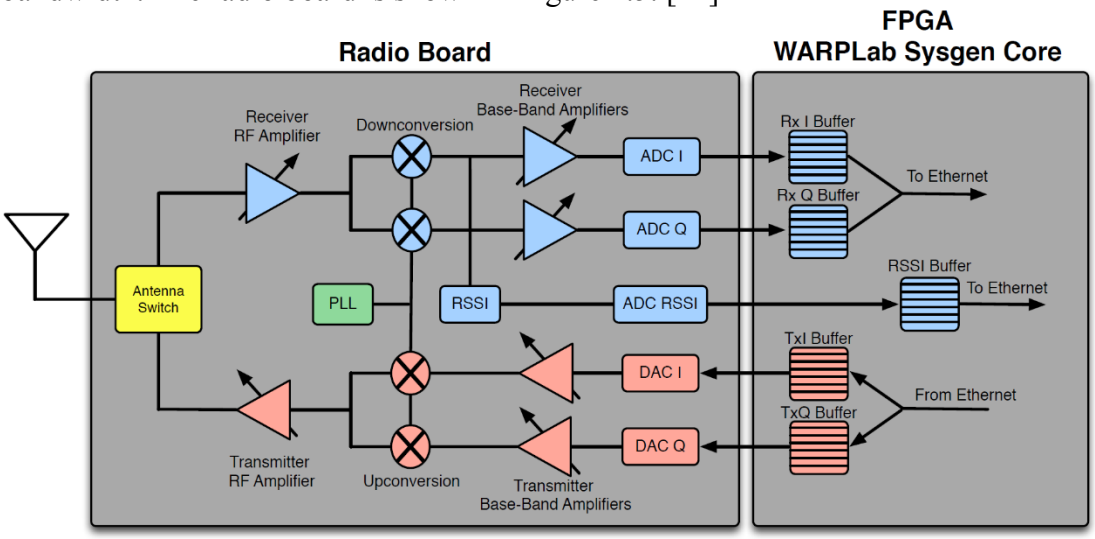

Figure 2.4. Transceiver structure of the radio board.

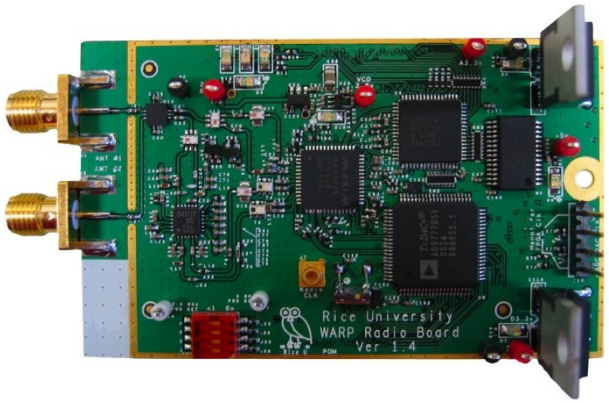

Figure 2.5. WARP radio board.

2.5. WARPLab framework

WARPLab is a framework for accessing WARP with Matlab from a user PC and is used to develop and customize physical layer algorithms. The framework is split between the user PC and WARP nodes. WARPLab reference Matlab code allows interaction with multiple WARP nodes. Connecting multiple WARP boards to a single computer requires an external Ethernet switch. User PC is processing all baseband calculations while transceiver signal processing is handled by the WARP board.

Baseband module is processing the samples being sent to and from the radio interfaces. The baseband section consists of RSSI, TX and RX buffer elements. RSSI buffer can hold up to 2^{12} samples, TX and RX buffers can hold up to 2^{14} samples. These samples can be interacted by using specific Matlab commands. [14]

2.6. Reconfigurable leaky wave antenna

Antenna element with dynamically adjustable frequency, radiation or polarization patterns is called a reconfigurable antenna. A Composite Right-Left-Handed (CRLH) leaky wave antenna is used in this thesis. The antenna consists of cascaded metamaterial microstrip unit cells, which are in a periodic structure populated with varactor diodes in series and shunt. Radiation is created from the power leakage as the signal wave proceeds through the structure. Radiation pattern of the CRLH antenna can be reconfigured without sacrificing any vital attributes like high gain or good impedance matching. Beam steering is done by modulating a Direct Current (DC) voltage across varactor diodes. Circuit model of the unit cell is shown in Figure 2.6. [15, 16]

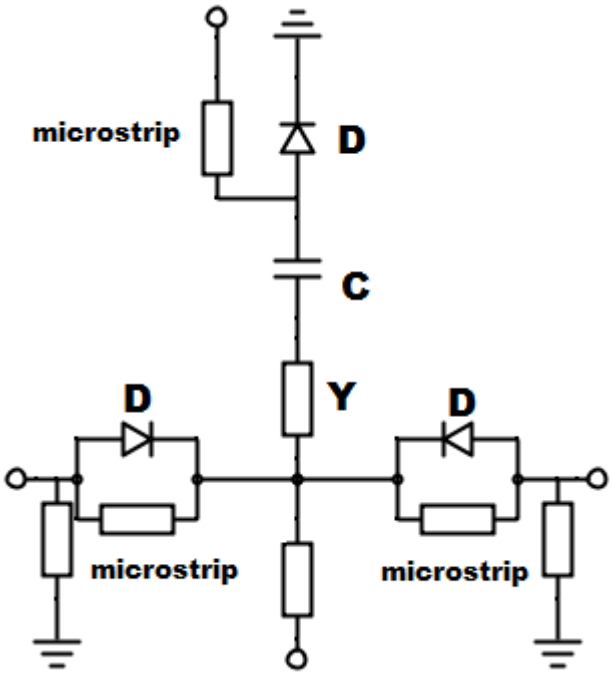

Figure 2.6. Unit cell structure of the composite right-left handed leaky wave antenna.

The reconfigurable leaky wave antenna has two separate RF-ports for radio signals and two ports for DC control signals. Center frequency of the antenna can be configured from 2.41 GHz to 2.46 GHz by modulating the DC control signals. The antenna gain also varies slightly proportionally to the control voltages. The antenna is built using a low loss Rogers 4360 substrate having dielectric constant ϵ_r = 6.15. Adjusting the voltage level of control signals will steer the beams of the antennas. The beam of the port 1 can be steered from 0° to +60° and the port 2 from 0° to -60°. The antenna accepts control signal voltages from 0 V to 30 V and can form an infinite number of different radiating patterns. The antenna is shown in Figure 2.7. [17, 18]

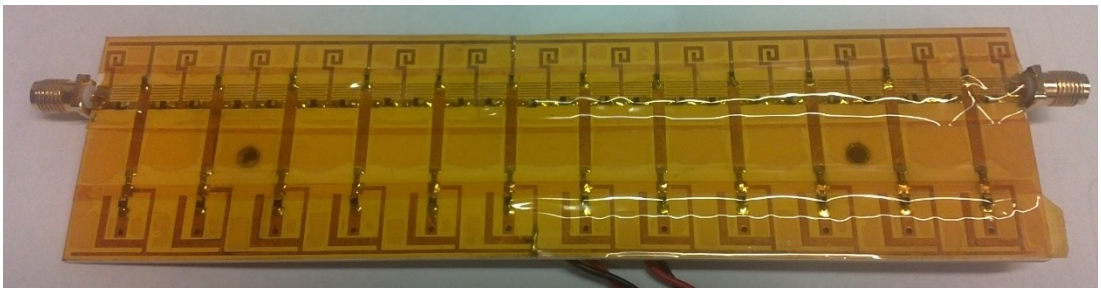

Figure 2.7. Reconfigurable leaky wave antenna.

2.7. Antenna controller specifications

RLWA is connected to the WARP system with a control board. Previous version of the control board is suboptimal for this job. Improvements are considered in output linearity, physical size, form of power supply and efficiency. The control board is shown in Figure 2.8. The control board has several passive heat sinks for linear regulators. The board is built using mainly through-hole components, which require more space than surface-mount components. Efficiency can be increased by using switching regulators rather than linear regulators. Block diagram of antenna control circuit is shown in Figure 2.9. As can be seen from the figure two digital 8 bit signals are connected to the controller input ports. Buffering components are used to prevent any damage afflicted back to the WARP board. Digital-to-analog conversion and amplification components are used to convert the digital signal to analog for the antenna input.

Control circuit should be designed and built following the given specifications. The main specifications are ruled by the input and output devices. Failing to follow these specifications will prevent the I/O devices from working properly. Output device, a reconfigurable leaky wave antenna, is using supply voltage between 10 – 30 V. The control board must be able to output two signals within this range with the best possible resolution. The second main specification is the input device. WARP GPP-SDR integration controls the RLWA using +3.3 V 16 bit data signal. Custom made user Matlab code control input doesn't use standardized communication protocol such as RS-232, which must be taken into account when designing the digital input to the antenna controller. Dividing the data signal into two 8 bit channels allows them both to control individual outputs. Control board should use +12 V DC supply voltage. It is justified as the WARP FPGA board uses the same supply voltage and this would

reduce the usage of extra transformers. Lowering the size of the board, energy efficiency and component costs were also key factors in the design work. [14, 18]

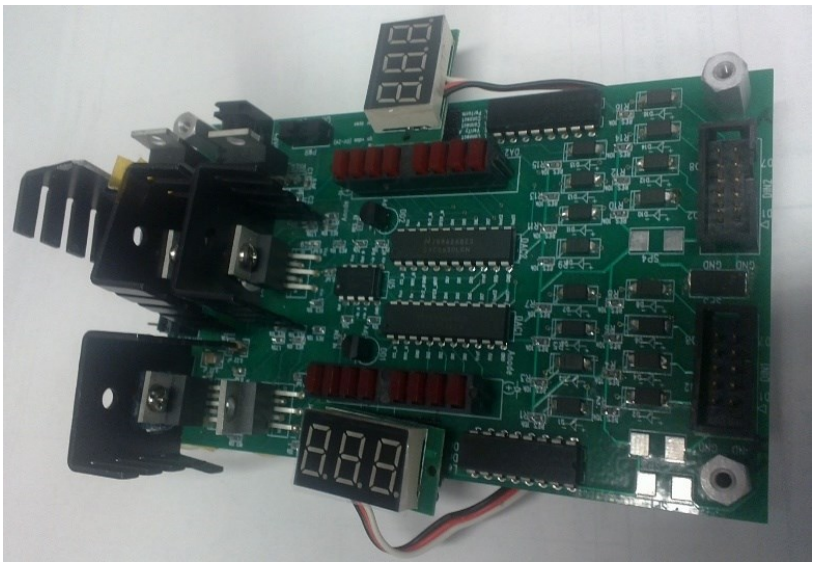

Figure 2.8. RLWA control board.

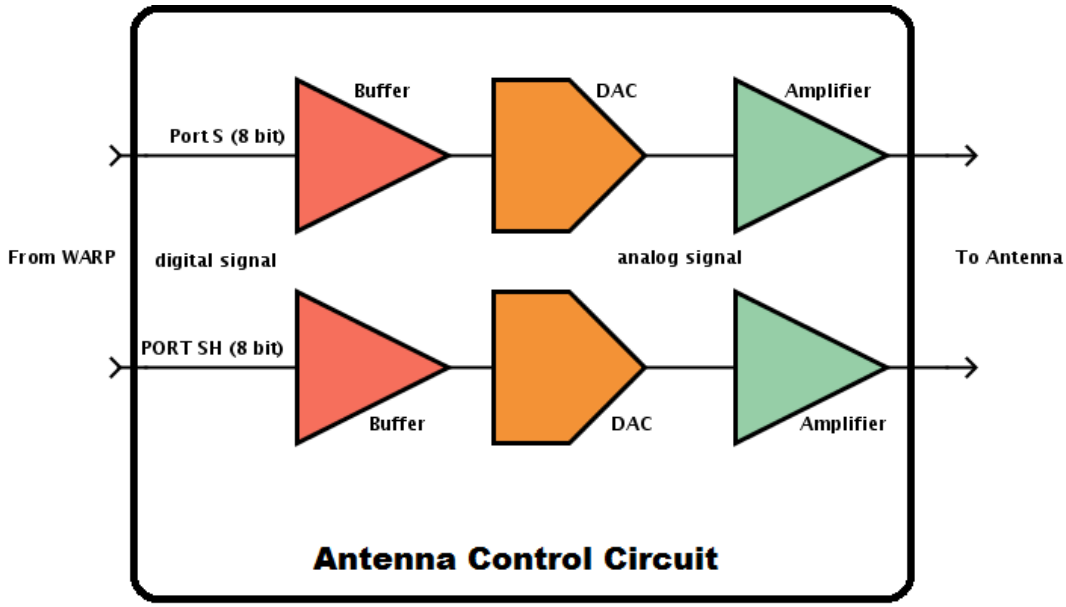

Figure 2.9. Structure of antenna control circuit.

3. ANTENNA CONTROL CIRCUIT

Main components of the design work are explained in this chapter. Focus is on the theoretical aspects of the design. Section 3.1 is describing boost converters, 3.2 focuses on operational amplifier setups and, finally, digital-to-analog converters are explained in Section 3.3.

3.1. Boost converter

Boost converter is a step up switching regulator. It means that the converter's input voltage is lower than the generated output voltage. Operation of a simplified switching converter is shown in Figure 3.1. When current flows through the switch energy is stored into the inductor. After the switch opens, the current flows through the diode in to the capacitor and to the load resistor. Inductor is shown as an additional voltage source in series with the original source, because inductor starts to discharge as time passes. Duty cycle is the fraction of time when the switch is in on-state. Duty cycle is presented as

$$D = 1 - \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}}, \tag{3.1}$$

where V_{IN} is the input voltage and V_{OUT} is the output voltage. Output current capability fades when duty cycle approaches zero. Duty cycle is proportional to the efficiency of a non-ideal switching regulator. Efficiency is

$$\eta = \frac{1}{1+\frac{R_{\mathrm{L}}}{(1-D)^2 R}}, \tag{3.2}$$

where R_{L} is parasitic resistance of the inductor and R is the load resistance. While the duty cycle is important factor, also having an inductor with low parasitic resistance assures higher efficiency. [19, 20]

As stated above, the inductor starts to discharge when the switch is in off-state. If the duty cycle is long enough, current flow through the inductor stops and the inductor is completely discharged. This phenomenon is called as Discontinuous Conduction Mode (DCM). Boost converter is in Continuous Conduction Mode (CCM), when the inductor's current ripple is small so that the inductor charge lasts through the duty cycle. DCM causes radical changes in the switching regulator system. Conversion ratio becomes depended on the load, output impedance is increased and polarity is reversed. Boost converter operates in CCM when

$$\frac{2L}{RT_{\mathrm{S}}} \geq D(1-D)^2, \tag{3.3}$$

where L is inductance, R is load resistance and T_{S} is switching period. [21]

Switching regulator is very efficient compared to the linear regulators. The power dissipated in the switching regulator circuit is minimal, because of the highly efficient Field Effective Transistor -switch (FET). Downside of the switching regulator is its

complexity. Several external components are required to program a desirable switching circuit.

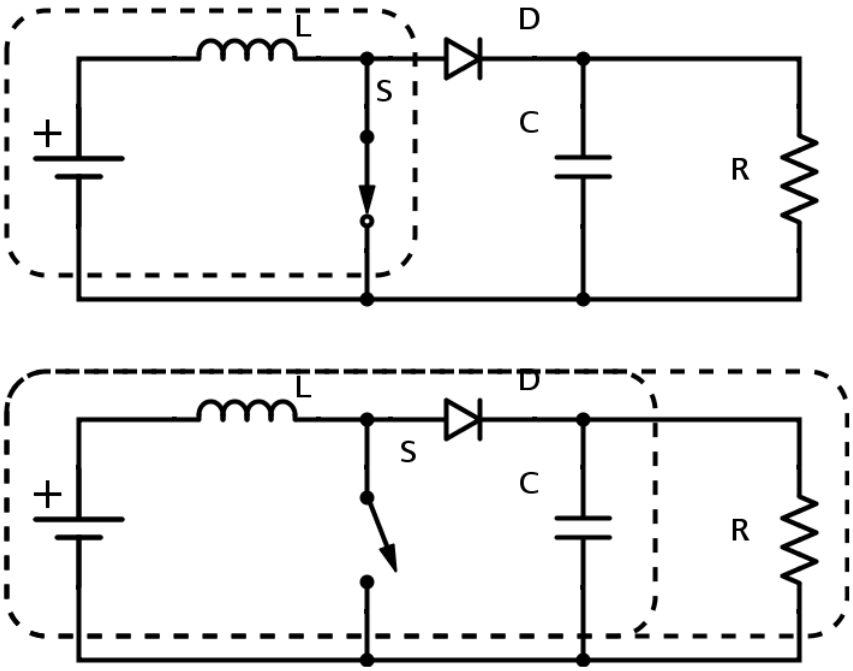

Figure 3.1. Operation principle of a boost converter.

3.1.1. External components of boost converter

Non-ideal boost converter needs a compensation network to ensure a stabile operation. Output voltage of the converter is affected by the non-linear components. A feedback loop is required for better output voltage precision. Also optimizing the transient responses will avoid possible oscillations in the output voltage.

Compensation network typically consists of an error amplifier and a passive component network. Error amplifier is connected as a feedback loop to prevent the output voltage from oscillating. Error amplifier signal is compared to the reference signal and any difference will force the output voltage back to the direction of reference voltage. External components of the boost converter is shown in Figure 3.2 [22]. As seen in the figure, the error amplifier is connected to the input voltage via an analog divider.

Resistors R_{TOP} and R_{BOT} are used to program a correct output voltage. Components R_S and C_S are used to form a soft start circuit since boost converter starts after signal level rises above threshold in the SHDN-pin. Feedback capacitor C_{FB} is used to improve transient response and reduce output perturbation due to a load step. Output voltage ripple is minimized with capacitor C_{OUT}. Individual component values are calculated according to Equations (3.4) and (3.5). Equations have been derived from the small signal model. [22]

Capacitance for the feedback capacitor can be calculated as [22]

$$C_{\mathrm{FB}} = \frac{500\mathrm{k}\Omega}{R_{\mathrm{BOT}}} \cdot 1\mathrm{pF}. \tag{3.4}$$

Output voltage V_{OUT} can be calculated according to [22]

$$V_{\mathrm{OUT}} = 1.255\mathrm{V}\left(1 + \frac{R_{\mathrm{TOP}}}{R_{\mathrm{BOT}}}\right). \tag{3.5}$$

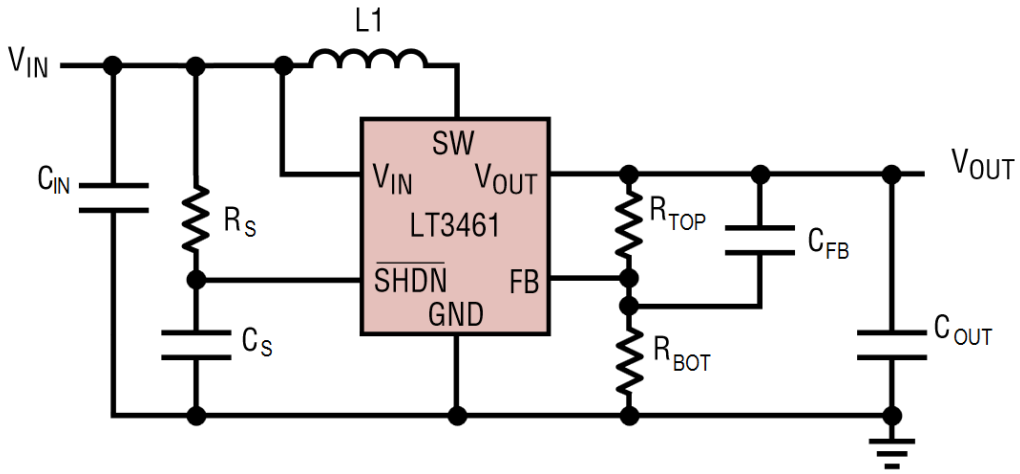

Figure 3.2. External components of the boost converter.

Inductor selection is crucial for the boost converter. The size of the inductor can be determined by deriving inductance L from Equation (3.3)

$$L \geq \frac{RT_{\mathrm{s}}D(1-D)^2}{2}. \tag{3.6}$$

3.2. Operational amplifiers

Operational amplifiers are getting more popular in electronic designs, because of their smaller physical size and lower building costs than a decade ago. A single operational amplifier can do the work of a much more complicated transistor circuitry. This section consists of a description of the main operational amplifier setups used in this thesis. Concepts of a buffer amplifier and a non-inverting voltage adder are familiarized in Sections 3.2.1 and 3.2.2.

3.2.1. Buffer amplifier

Operational amplifier connected as a buffer amplifier is shown in Figure 3.3. In this setup, the input voltage equals the output voltage. The key idea of a buffer amplifier is to separate different parts of the circuit. The buffer maintains the input voltage level in output and guaranties a stabile current flow from the supply voltage. This is

beneficial, for example, in situations where a voltage divider is used. Operational amplifier supplies the needed current and V_{in} is just a signal containing the intended voltage.

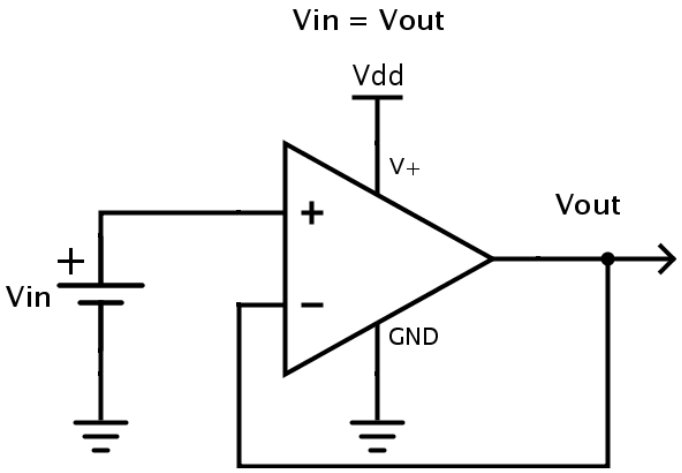

Figure 3.3. Connection of a buffer amplifier.

3.2.2. Non-inverting voltage adder

Operational amplifier, where input voltage is connected to a positive input terminal so that the output voltage has equivalent sign as the input voltage, is a non-inverting amplifier. Voltage adder is a circuit which sums up voltages of two different signals. An example circuit of a non-inverting voltage adder is shown in Figure 3.4. Output voltage is calculated as follows

$$V_{out} = \frac{R_1 + R_2}{R_1}\frac{\sum_1^n V_n}{n}, \tag{3.7}$$

where V_{out} is the output voltage, V_n is n:th input signal voltage, n is the number of input signals, R_1 and R_2 are the resistors shown in Figure 3.4. [19, 23]

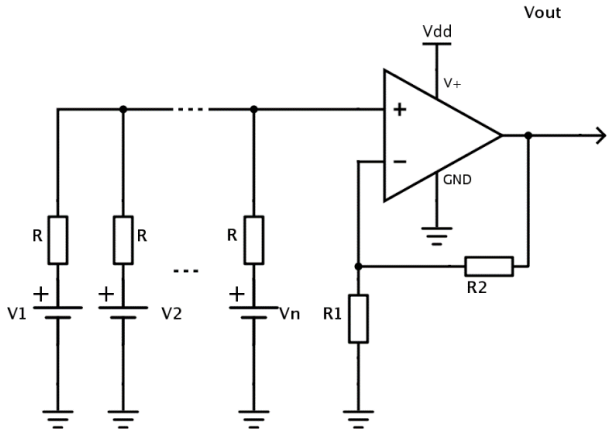

Figure 3.4. A non-inverting voltage adder.

3.3. Digital-to-analog converter

Digital signal can be transformed to an analog signal using integrated circuit called Digital-to-Analog Converter (DAC). This section focuses on a multiplying DAC and the important parameters around it like resolution, settling time and linearity error.

Reference voltage defines the range of the multiplying DAC. Multiplying DAC's internal structure is an R/2R ladder network as shown in Figure 3.5. Digital input signals control the switches. If a digital signal is in a state "1", the switch is in position 1 and the input reference signal flows through that part of the ladder network. This will increase the voltage level of the analog signal in the V_{ref} pin. Input reference voltage limits the maximum voltage level of the analog signal. To ensure the best linearity, the output should be separated from high impedances.

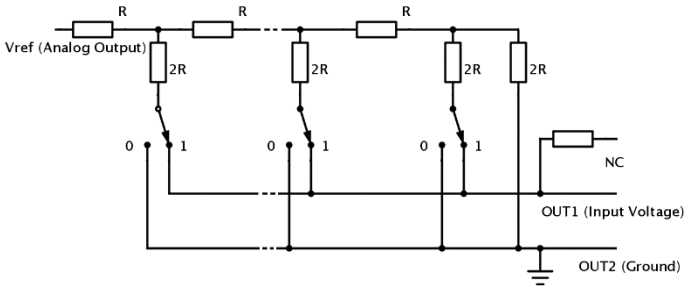

Figure 3.5. Multiplying DAC R/2R-ladder network in the voltage mode.

Resolution of the output signal is determined by the range of the input reference signal and the number of bits in digital input signal. The least significant bit resolution V_{LSB} can be calculated as

$$V_{\text{LSB}} = \frac{V_{\text{in}}}{2^k}, \tag{3.8}$$

where V_{in} is the voltage level of the input reference signal and k is the number of input bits. Another important parameter for a DAC is the settling time. It is the time required for the analog signal to reach the target voltage level. If the input keeps changing faster than the settling time, the output signal oscillates between the desired voltage levels. Linearity error is the deviation from the ideal output to the actual voltage level. This is caused by errors in offset and gain. [24]

4. DESIGN STRUCTURE AND SIMULATION RESULTS

4.1. Regulator circuit

Stabilized power source is a requirement for the designed antenna control system so designing a stable and power efficient regulator circuit is important. Regulator circuit typical setup consists of a regulator, stabilizing passive component network and buffering network.

Specifications of antenna controller circuit are +12 V power supply and +30 V output signal voltage. This means that regulator circuit must be able to produce higher voltage than the input voltage is. LT3461 DC-DC boost converter is chosen for this purpose. The key electronic characteristics are shown in Table 1. As seen from the table, LT3461 is suitable to be used in the regulator circuit of the controller design. [22]

Table 1. Electronic characteristics of a LT3461 converter

Parameter	**Value**
Input operating voltage	2.5 – 16 V
Maximum output voltage	36 V
Switching frequency	1.3 MHz
Current limit	600 mA

4.1.1. Input and output capacitors

Input capacitor is used to minimize the input voltage ripple. The manufacturer recommends ceramic capacitor with low Equivalent Series Resistance (ESR) ratio and capacitance of at least 1 µF. Input capacitor is shown in Figure 3.2 as C_{IN} and 4.7 µF ceramic capacitor is with 50 V voltage rating has been chosen. [22]

The output capacitor C_{OUT} is needed for stabilizing the output voltage. Ceramic capacitor with low ESR value is recommended by the manufacturer. 2.2 µF ceramic capacitor with 50 V voltage rating has been chosen for the output. Impedance versus frequency of typical ceramic capacitors is shown in Figure 4.1 [25]. As seen from the figure, impedance level of 2.2 µF capacitor stays under 0.1 Ω from 1 MHz to 20 MHz. Output voltage ripple can be calculated as follows

$$\Delta V_{\mathrm{P-P}} \cong I_{\mathrm{LOAD}} R_{\mathrm{ESR}} \frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}}, \tag{4.1}$$

where $\Delta V_{\mathrm{P\text{-}P}}$ is the output voltage ripple, I_{LOAD} is the load current, R_{ESR} is the ESR level, V_{OUT} is the output voltage and V_{IN} is the input voltage. In worst case scenario, the load current is approximately 50 mA so Equation (4.1) gives us

$$\Delta V_{\mathrm{P-P}} \cong 50\ \mathrm{mA} \cdot 0.1\ \Omega \frac{32\ \mathrm{V}}{12\ \mathrm{V}} = 0.0133\ \mathrm{V}. \tag{4.2}$$

In the worst case scenario, the voltage ripple is still reasonable low compared to the least significant bit resolution which is 0.078 V. [26]

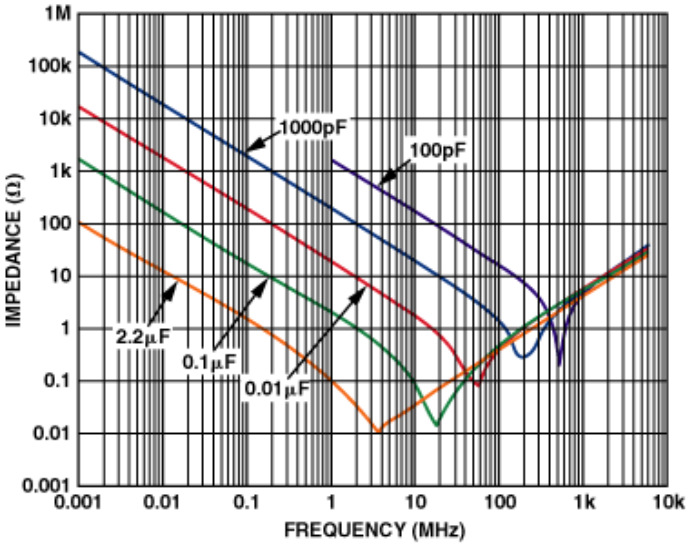

Figure 4.1. Capacitor impedance as a function of frequency.

4.1.2. Other external components

Compensation network is designed according to Chapter 3.1. First, the duty cycle is calculated from Equation (3.1)

$$D = 1 - \frac{V_{IN}}{V_{OUT}} = 1 - \frac{12\ \text{V}}{32\ \text{V}} = 0.625. \tag{4.3}$$

Load current can be estimated as 40 mA. Now, the required inductance can be calculated according to Equation (3.6) as

$$\begin{aligned} L &\geq \frac{RT_s D(1-D)^2}{2} \\ \Leftrightarrow L &\geq \frac{\frac{V_{\text{out}}}{I_{\text{load}} f_s} D(1-D)^2}{2} \\ \Leftrightarrow L &\geq \frac{\frac{32\ \text{V}}{40\ \text{mA} \cdot 1.3\ \text{MHz}} \cdot 0.625(1-0.625)^2}{2} \\ \Leftrightarrow L &\geq 27.043\ \mu\text{H}. \end{aligned} \tag{4.4}$$

This result gives the minimum amount of inductance required for stable CCM action for the boost converter. If the load current or the switching frequency or inductance falls under the estimated values, boost converter will operate in CCM. Effects of temperature changes should not be under estimated. WE-QDS 47 µH inductor is chosen and the electrical parameters are shown in Table 2 [27]. Inductor's self-resonant frequency should be over the used switching frequency, because the

inductance falls under the promised ratio in the self-resonant frequency region. Another important electrical parameter is rated current of the inductor. This should be higher than the boost converter in-rush current peak. DC resistance parameter is directly related to the efficiency of the boost converter and usually trade-off must be made between the DC resistance, inductance and physical size of the inductor. [22]

Table 2. Electronic characteristics of a WE-QDS inductor

Parameter	**Value**
Inductance	47 µH ±20 %
Rated current	1 A
Self-resonant frequency	6.7 MHz
DC resistance	272 mΩ

The output voltage is programmed according to Equation (3.5). Resistance of R_{TOP} can be calculated by fixing R_{BOT} = 10 kΩ as

$$\begin{aligned} V_{\mathrm{OUT}} &= 1.255\ \mathrm{V}\left(1+\frac{R_{\mathrm{TOP}}}{R_{\mathrm{BOT}}}\right) \\ \Leftrightarrow R_{\mathrm{TOP}} &= R_{\mathrm{BOT}}\left(\frac{V_{\mathrm{OUT}}}{1.255\ V}-1\right)= \\ 10\ \mathrm{k\Omega}&\left(\frac{32\ \mathrm{V}}{1.255\ \mathrm{V}}-1\right)=244.98\ \mathrm{k\Omega}. \end{aligned} \tag{4.5}$$

Feedback capacitance is calculated according to Equation (3.4) as

$$C_{\mathrm{FB}}=\frac{500\ \mathrm{k\Omega}}{R_{\mathrm{BOT}}}\cdot 1\ \mathrm{pF}=\frac{500\ \mathrm{k\Omega}}{10\ \mathrm{k\Omega}}\cdot 1\ \mathrm{pF}=50\ \mathrm{pF}. \tag{4.6}$$

Soft start circuit components are chosen according to the manufacturer's suggestions.

4.1.3. Voltage output

Final part of the regulator circuit is to generate different supply voltages for digital side. System requires a 5 V supply voltage for the inverter and buffer. The 5 V is also used as a reference voltage for the DAC. The 32 V power is required for the amplifier to obtain linear operation. The 10 V signal is used in summer circuit as an input signal and for DAC's supply voltage.

The main 32 V supply voltage can be divided in to the lower voltages using resistors as voltage dividers. Desired resistor values can be calculated using Ohm's law for output voltage V_{OUT} as

$$V_{\mathrm{OUT}}=\frac{R_2}{R_1+R_2}V_{\mathrm{IN}}, \tag{4.7}$$

where resistances of resistors R_1, R_2 are shown in Figure 4.2 and V_{IN} is the input voltage.

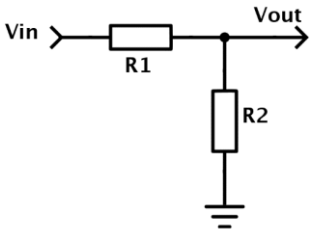

Figure 4.2. A voltage/power divider circuit.

R_1 can be calculated for voltage dividers by fixing R_2 as 10 kΩ

$$R_{1,5\text{V}} = \frac{32\ \text{V} \cdot 10\ \text{k}\Omega}{5\text{V}} - 10\ \text{k}\Omega = 54\ \text{k}\Omega \tag{4.8}$$

$$R_{1,10\text{V}} = \frac{32\ \text{V} \cdot 10\ \text{k}\Omega}{10\ \text{V}} - 10\ \text{k}\Omega = 22\ \text{k}\Omega. \tag{4.9}$$

Fixed resistor R_2 value is chosen from the standard resistor value table so that the result for Equation (4.6) gives another standard value. Voltage dividers are connected to the buffer amplifiers as shown in Figure 4.3. Now, the regulator circuit design has been completed.

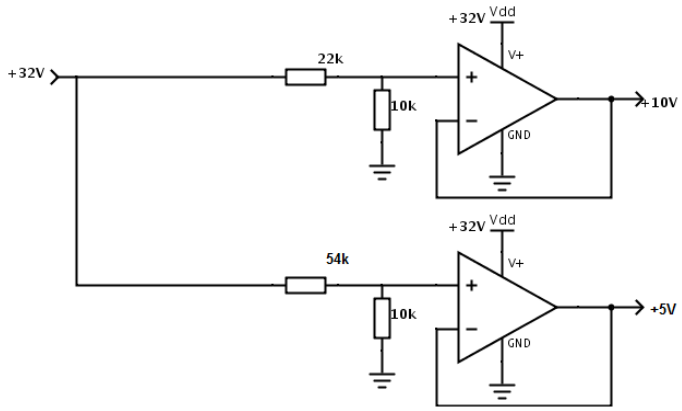

Figure 4.3. Voltage dividers and buffers.

4.2. Digital to analog conversion

The digital part of the circuit functions as a digital to analog converter. A digital signal, sent from the WARP is transformed to an analog output signal as stated in the specifications in Section 2.7. Several external components are required to guarantee a proper functioning of the DAC-circuit.

Before the conversion, it is advised to isolate the digital circuit from the WARP FPGA-circuit. This prevents any damage to the WARP-system in case of malfunction. A buffer circuit is placed right after the input terminal for the isolation and buffer output is connected to the digital analog converter.

4.2.1. D/A converter

Choosing the most optimal D/A converter requires careful considerations. An 8 bit multiplying DAC is used in this thesis to match the input digital signal to an analog antenna control signal. TLC7524 DAC is capable of transforming 8 bit 3.3 V digital input to a 0 - 5 V analog signal and is chosen for the controller [28]. Straight conversion to 20 V is not possible. If 20 V reference signal had been used, DAC would not "recognize" the digital 3.3 V input signals as "1". According to the datasheet, the digital input signal should equal the voltage of the reference signal. By using 5V DC as a reference signal, the DAC can still "recognize" the 3.3 V input signals as "1". Another requirement is that the supply voltage should be higher than the reference voltage. 10 V is used as the supply voltage since it is required in the design as stated in Section 4.2.3.

4.2.2. Delay block

Normally, the data conversion is done after handshake using data bus and control bus. In our case, however, the WARP doesn't send any control signals, so the DAC must be in receive data mode continuously. Data conversion with the handshake would require a suitable program for the WARP but this thesis is focusing on the development of the antenna control board and software development is left for further study. Since the control signal inputs are not connected to the WARP, a starting delay can be made using DAC's control signal pin. Idea of the starting delay is to compensate the handshake, because DAC is designed so that there would be a handshake signal. The starting delay is added to prevent any malfunctions at start-up. Delay block is made from a resistor, a capacitor and an inverter as shown in Figure 4.4.

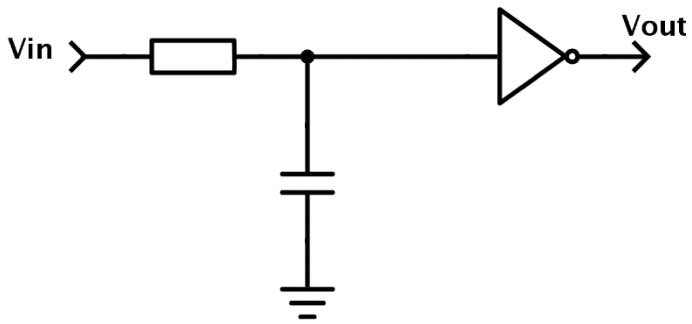

Figure 4.4. Delay circuit used in.

Delay input is connected to a 5 V digital supply voltage. When powered up, the inverter starts to send a signal to the DAC until inverters input rises over a certain threshold. Voltage level as a function of time can be calculated according to

$$V_{\mathrm{OUT}}(t) = V_{\mathrm{IN}}\left(1 - e^{-t/RC}\right), \tag{4.10}$$

where V_{IN} is the input voltage, t is time in seconds and RC is a time constant where the values of resistor and capacitor have been multiplied. The output voltages with

different time constants have been plotted in Figure 4.5 according to Equation (4.10). [29]

Sizing the passive elements can be done with the help of Figure 4.5. The inverter threshold voltage is 1.2 V. Half-second time delay is enough for the rest of the circuit to start-up so a suitable time constant value is around 2 and 3. With a resistor value of 100 kΩ and a capacitor value of 20 µF, time constant value 2 is obtained.

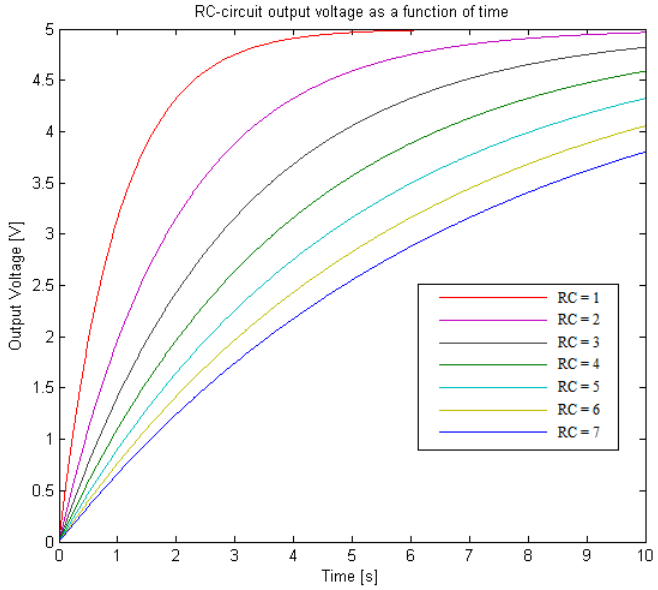

Figure 4.5. The output voltage of RC-circuit as a function of time.

4.2.3. Operational amplifier chain

Digital to analog converter connections are designed according to Section 3.3 and Section 4.2.2. DAC's amplified signal is 0 V to 5 V output voltage depending on the input signal. Since the specifications demand 10 V to 30 V output voltage, amplification is required. Chain of operational amplifiers is designed for this purpose.

Circuit diagram of the operational amplifier chain with component sizing is shown in Figure 4.6. DAC output is separated from the rest of the circuit with a buffer amplifier so the output doesn't see high impedance. This will ensure good linearity of the output voltage. Buffer amplifier is the first at the left side in Figure 4.6. Next step is to amplify the signal from 0 – 5 V to 0 – 20 V. It is done with the second operational amplifier, which is connected into non-inverting mode of operation. Lastly, a non-inverting voltage adder can be used as the summer circuit, which lifts the signal level +10 V.

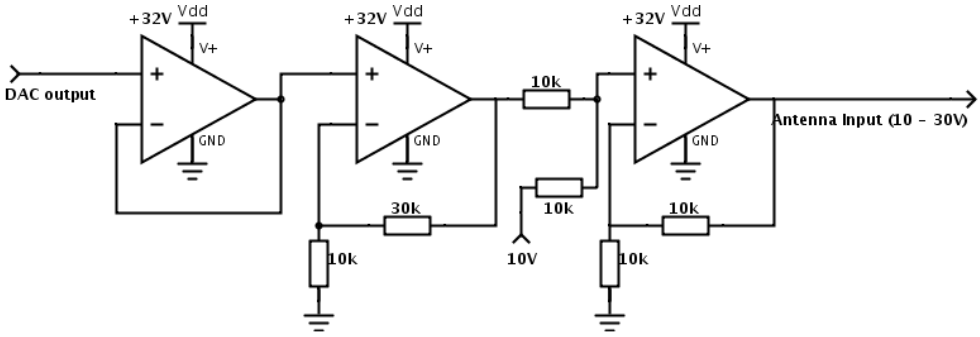

Figure 4.6. Operational amplifier chain.

4.3. Simulations

LTspice software is used to simulate the circuit design. The regulator circuit can be simulated accurately since the boost converter is modelled in the LTspice. Data conversion from digital to analog cannot be simulated since there is no model for the DAC. This section aims to verify designed analog circuits via Simulation Program with Integrated Circuit Emphasis (SPICE) process.

Regulator circuit is simulated using LT3461 boost converter component and ideal external passive components. The passive components are sized to match standard component values. Simulated regulator circuit design is shown in Figure 4.7. I_1, I_2 and I_3 represent the load, which is generated by the other parts of the board. Transient analysis is used to simulate the circuit design. Signal measurement points are at the output of the operational amplifiers U_2 and U_4. The transient analysis will plot a voltage level in a function of time and is shown in Figure 4.8. The wanted voltage levels: +10 V and +5 V are reached as seen from the figure. No major oscillations can be seen although the non-idealities of the component will add some fluctuation to the signal.

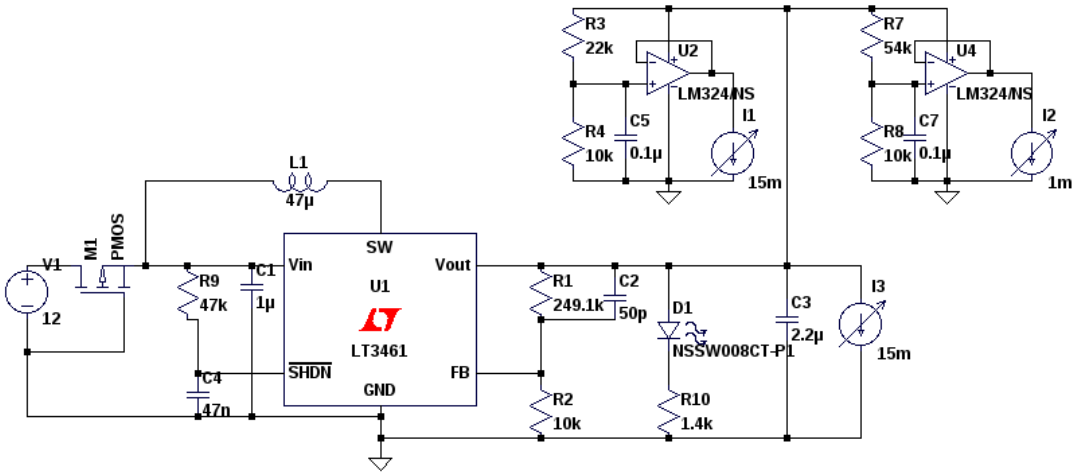

Figure 4.7. Regulator circuit design in LTspice.

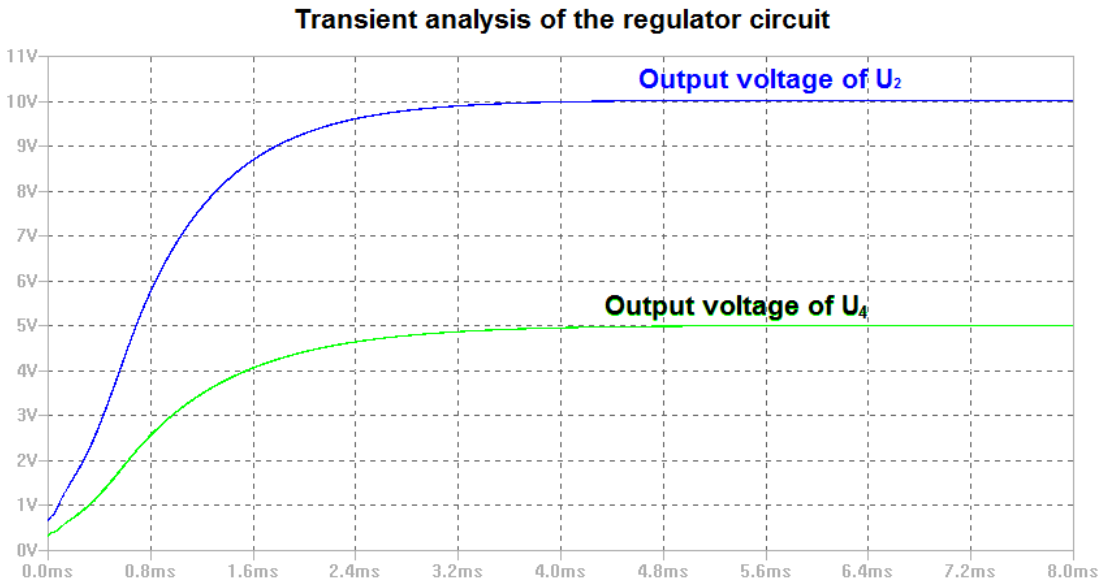

Figure 4.8. Transient analysis of the regulator circuit.

Current flown through the L_1 inductor as a function of time is presented in Figure 4.9. When the boost converter is started, inrush current is generated from the voltage difference between input and output ports of the voltage regulator. Inrush current peaks at 410 mA, so the chosen inductor WE-LQS is able to sustain such amount of current. LT3461 boost converter itself can sustain 1.5A inrush current. Current flow stabilizes to around 160 mA after 630 µs. The boost converter stays in continuous current mode, since the current flows continuously through the inductor.

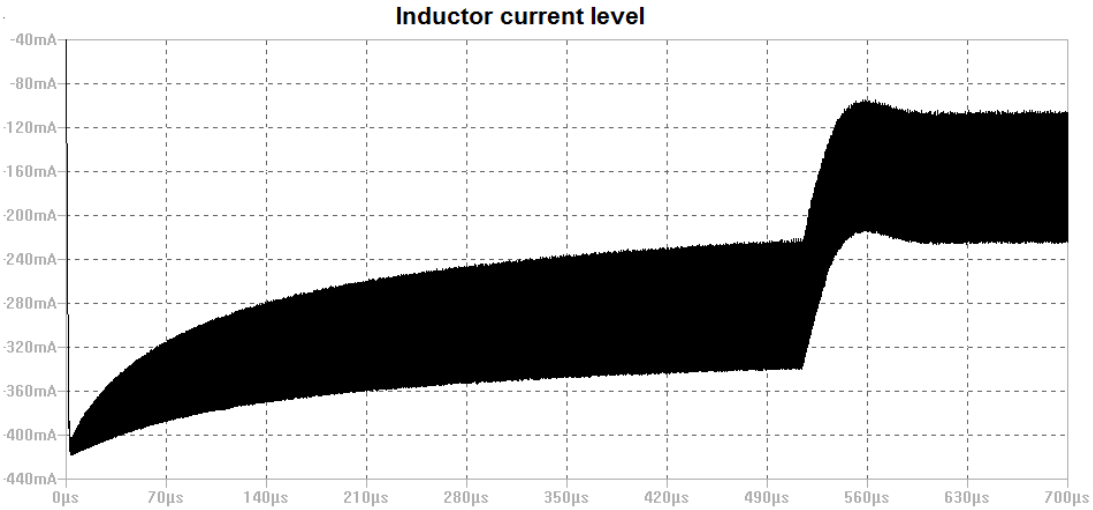

Figure 4.9. Current level through the inductor as a function of time.

LTspice simulation for the RC-circuit is used to verify the previous analytic simulations with Matlab software. Circuit design is shown in Figure 4.10 and the result of the transient analysis in Figure 4.11. The transient analysis through simulation is done with a startup option where the voltage source starts from 0 V. As seen from the transient analysis, the Matlab analytic simulation results a good matches.

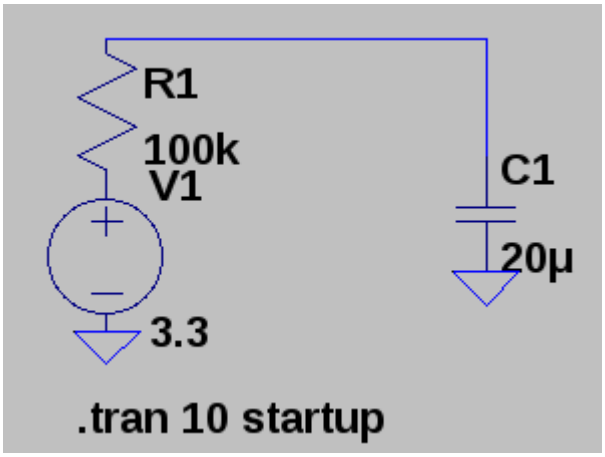

Figure 4.10. RC-circuit design.

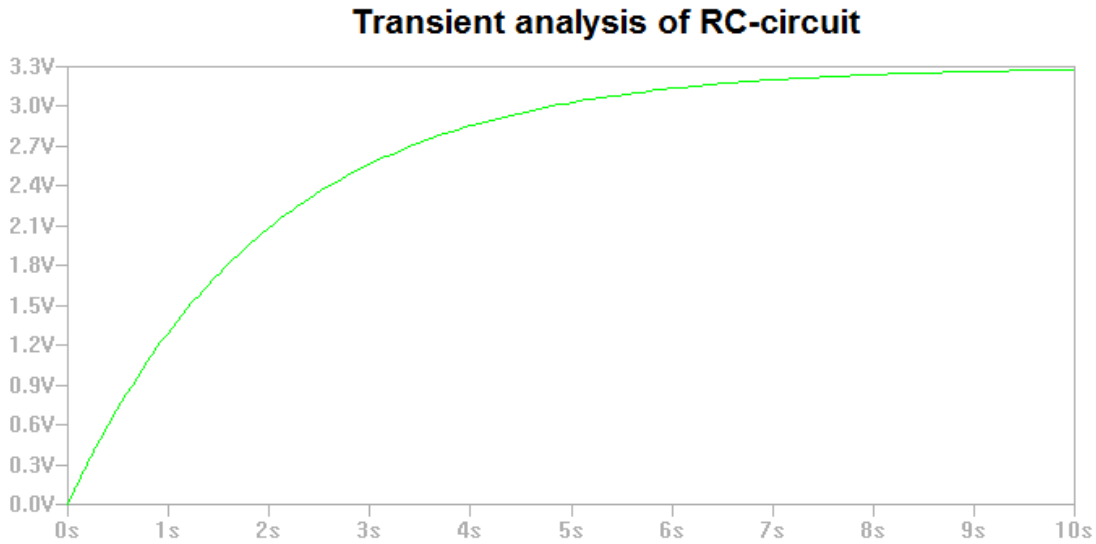

Figure 4.11. Result of transient analysis of RC-circuit.

Operational amplifier chain circuit cannot be simulated with the used operational amplifiers since the LTspice libraries do not include ISL28210. The main operation principle can still be simulated. LM324 operational amplifier is used to replace the ISL28210 in this simulation. Circuit design is shown in Figure 4.12. DAC output is modelled with a +20 V signal from the regulator circuit. Load resistance of 100 kΩ simulates the antenna.

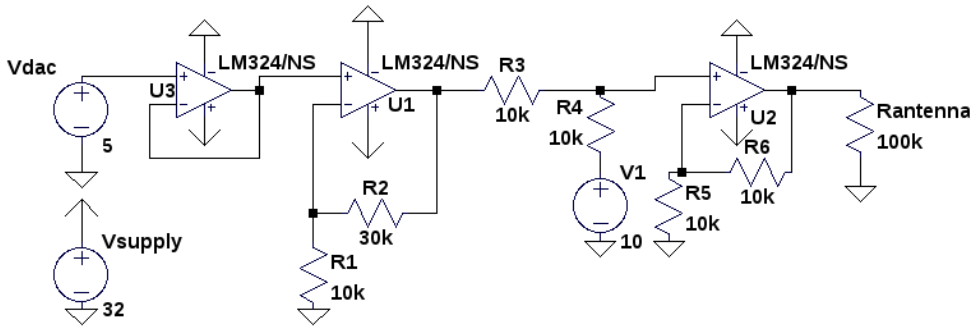

Figure 4.12. Summer circuit design in LTspice.

The result of transient analysis of the circuit is shown in Figure 4.13. Analysis consists of three measurement, which are located in output of each amplifier. The first amplifier output is marked as buffered voltage and it reaches 5 V. Amplified voltage is measured from the second amplifier output. The third amplifier output is antenna voltage. As seen from the figure, the voltage level reaches 30 V.

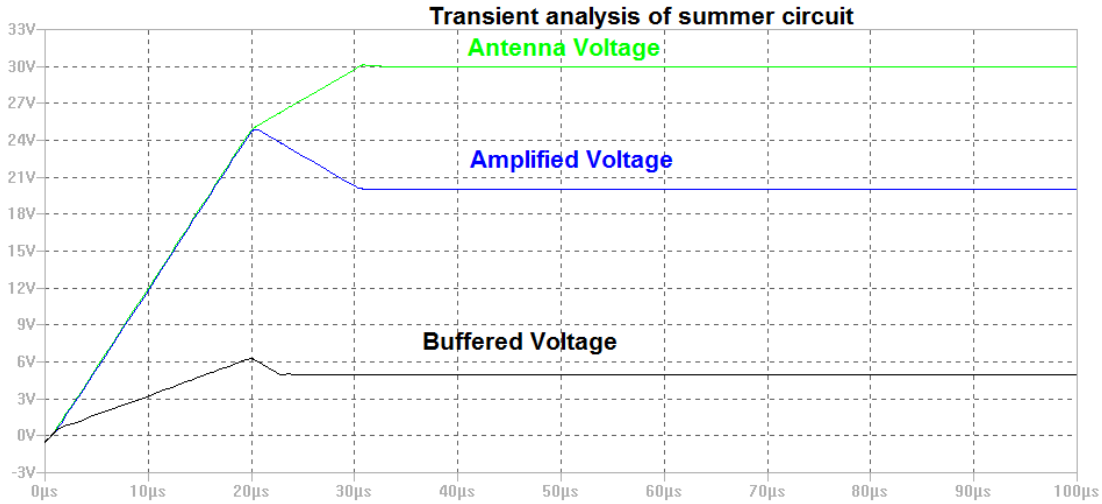

Figure 4.13. Transient analysis of the summer circuit output.

4.4. Complete schematic and board layout

After successful simulations, the schematic is constructed using Eagle Cadsoft. The schematic consists of two parts. Regulator circuit is included in the first part and digital to analog conversion is in the second part. They are shown in Figure 4.14 and in Figure 4.15 respectively. The regulator circuit has some external components, which are not introduced in the above sections. Three components from the left in Figure 4.14 are power supply connector, NMOS transistor and power switch. NMOS transistor prevents any current to flow back to the power supply in a case of failure. Transistor also protects the circuit partly from electrostatic discharge. Two green LEDs (Light Emitting Diode) are added to signal status of the control board. DAC part is isolated from input side with buffers so in case of component failure, current cannot flow back to the WARP. Floating of the input is eliminated with pull-down resistor network.

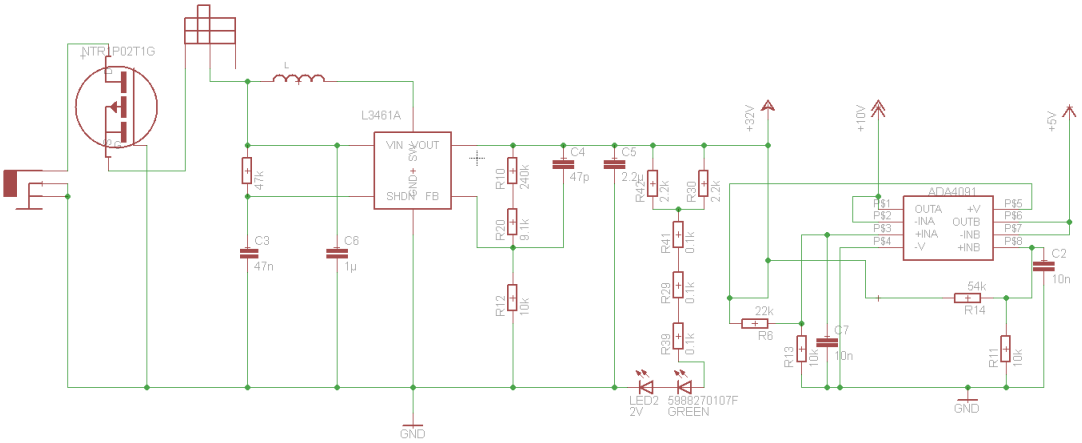

Figure 4.14. Schematic of regulator circuit part.

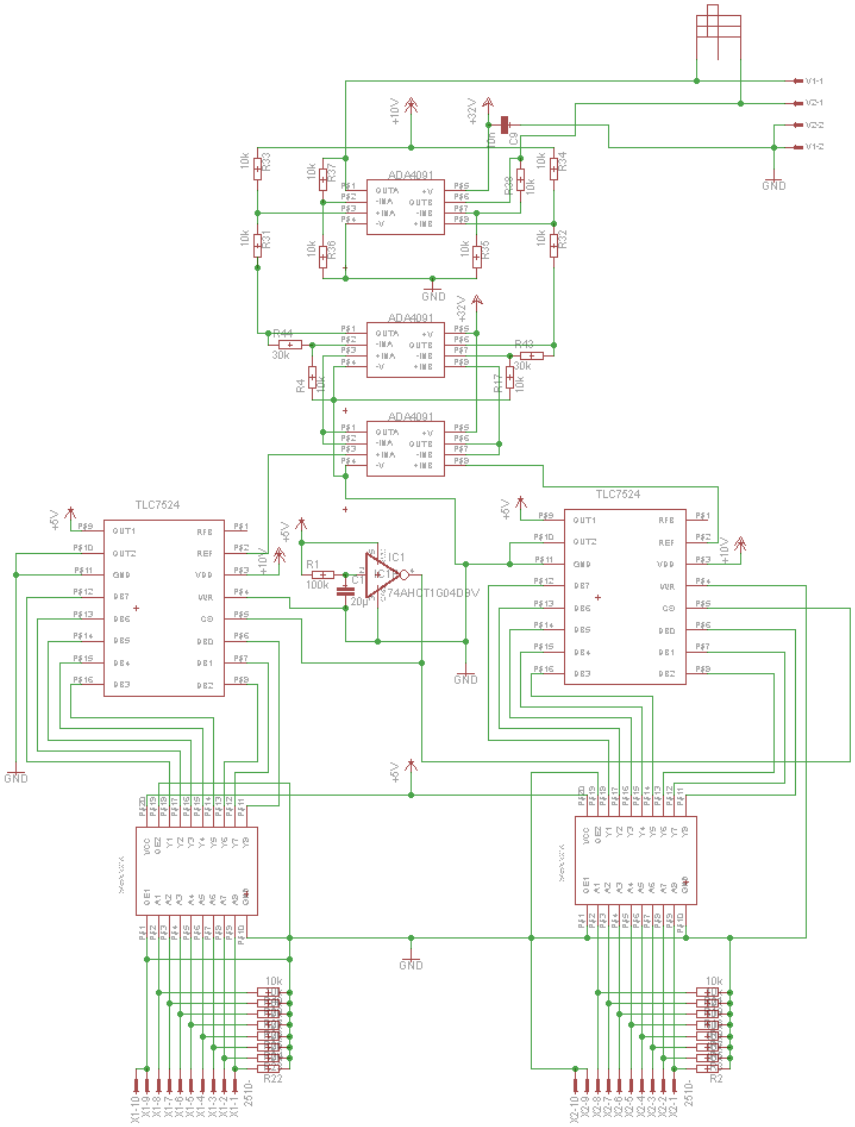

Figure 4.15. Schematic of digital to analog circuit part.

Circuit design is implemented on a printed circuit board using surface mounted components. Board layout is shown in Appendix 1. Layout design follows certain guidelines to ensure stabile operation. The boost converter is placed as close to the external component network as possible. This is done to minimize any parasitic elements such as resistance, inductance or capacitance. Boost converter's inductor path is especially vulnerable to parasitic series resistance since high amount of current with high frequency is going through the path. Capacitors C_2 and C_7 are placed as close to the operational amplifier inputs as possible. These capacitors are designed to act as energy storages so that the output ripple is minimized. [22, 23]

The board is manufactured in a workshop at the Faculty of Information Technology and Electrical Engineering. Components are attached to the control board with solder paste. First, the solder paste is applied on the component pads as seen in Figure 4.16. Components are place on the pasted pads. Finally the board is heated using reflow oven. Reflow oven temperature is controlled with a thermal profile. Few components such as header pins are surface mount components are attached afterwards to the board with soldering iron.

The finished product is shown in Figure 4.17. A voltage meter is attached to the board so that the output voltage can be seen. Board includes two switches: the right one is power switch and the left one controls the voltage meter measurement point. Board length is 7.5 cm, width is 8 cm and height is 3 cm.

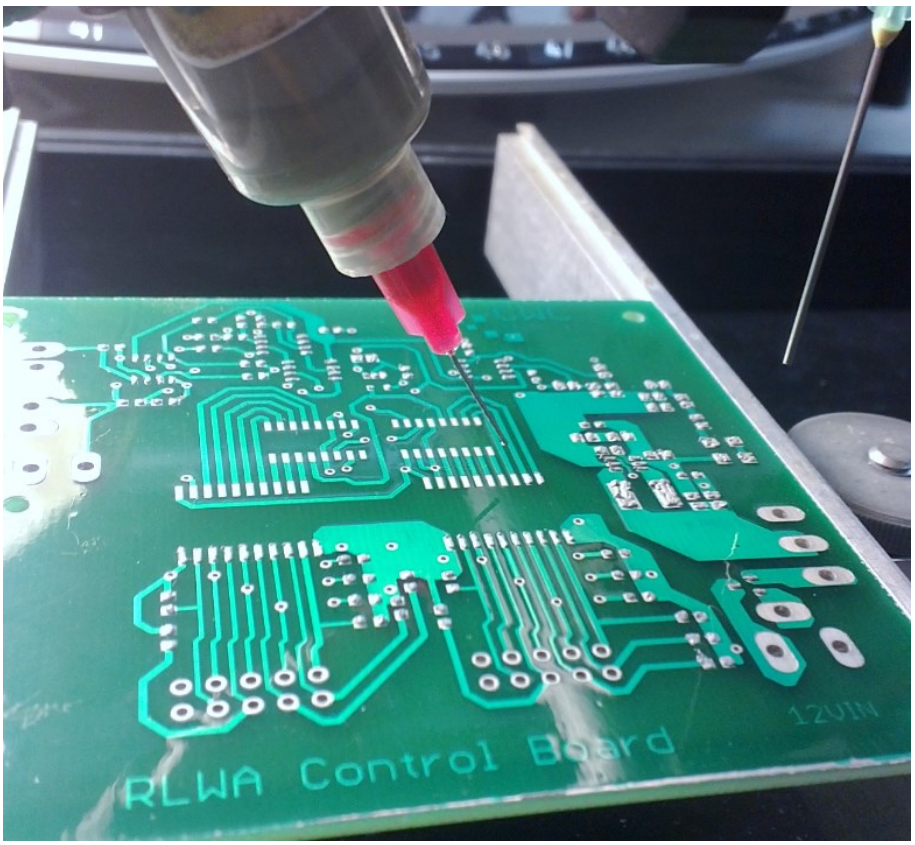

Figure 4.16. Applying solder paste on the board.

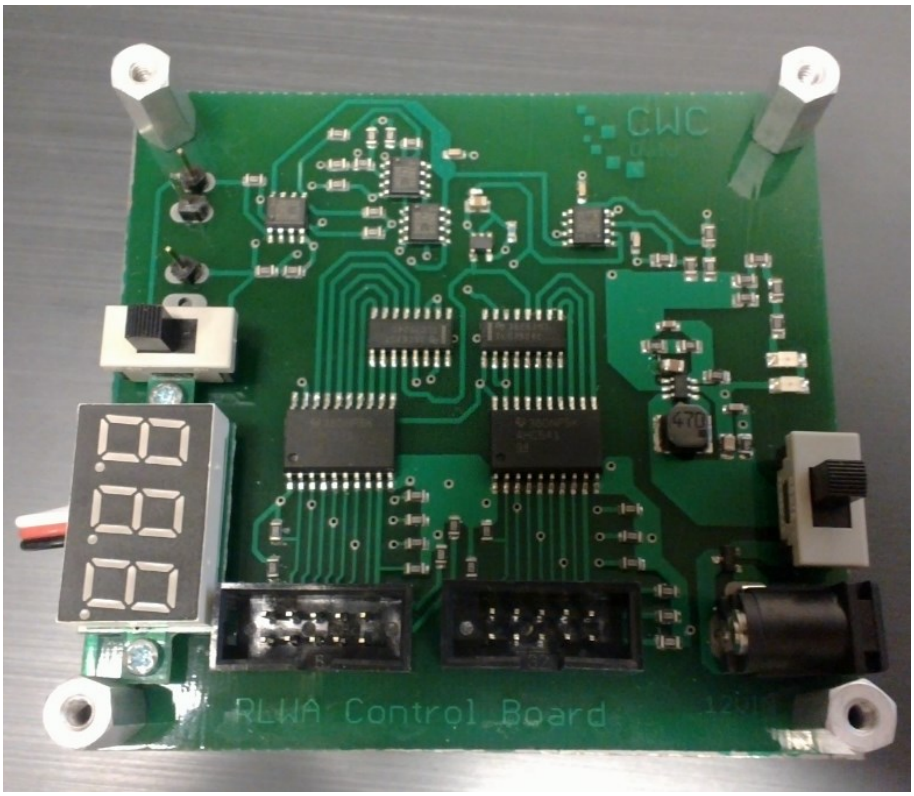

Figure 4.17. RLWA control board.

5. MEASUREMENT RESULTS

System verification requires real life measurement results. The verification are done at University of Oulu, Department of Communications Engineering. For clarity, the designed antenna control circuit is referred as new control board and the Drexel University's manufactured control board is referred as old control board. Power consumption measurements of the new designed antenna control board and the previous old version are described in Section 5.1. Antenna control board analog output voltage measurements are presented in Section 5.2 and Section 5.3. Antenna measurements are described in Section 5.4.

5.1. Power consumption

Designed new antenna control board power consumption is measured using Agilent N6705B DC power analyzer [30]. Power analyzer output is set as 12 V DC with 0.5 A current limit. Output is connected to the power supply input of the new antenna control board. Power analyzer measurement of the new antenna control board supply input is shown in Figure 5.1. Simulated current consumption is shown in Figure 5.2.

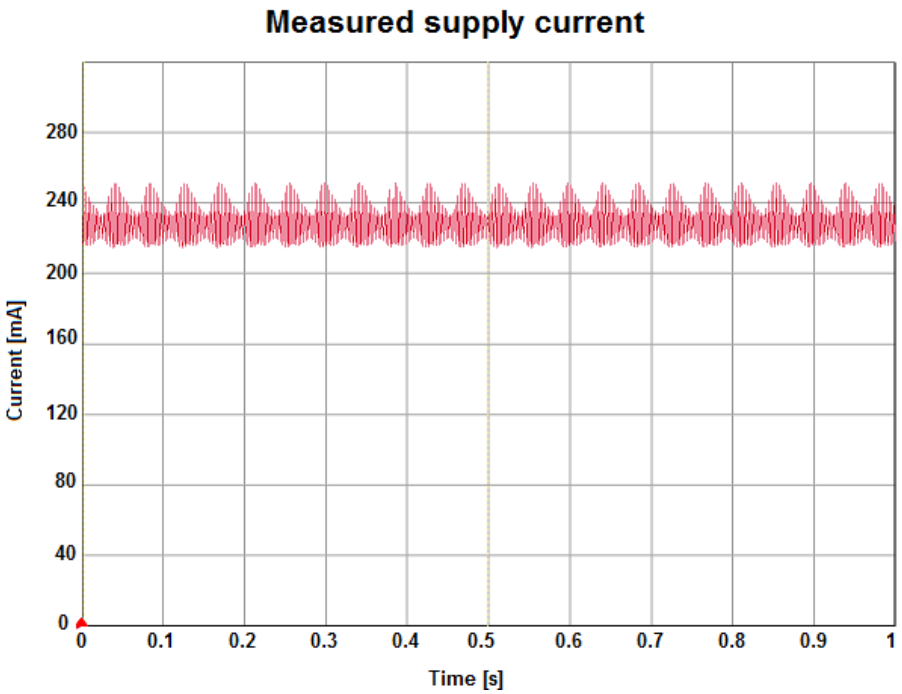

Figure 5.1. New antenna control board supply current as a function of time.

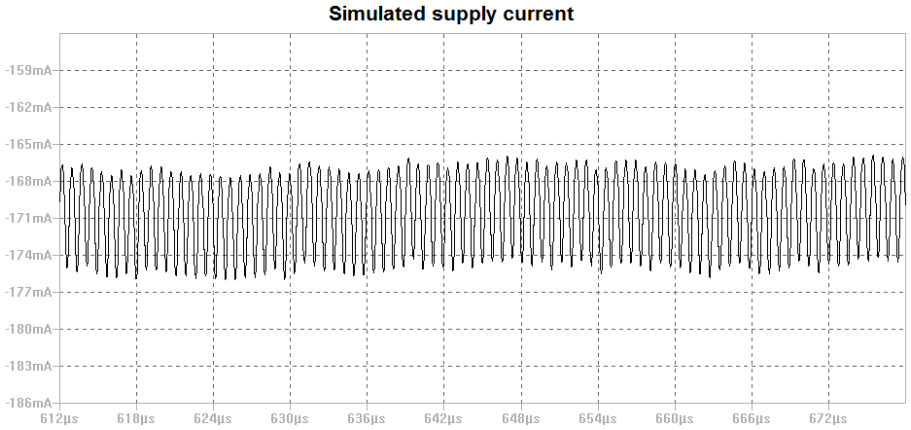

Figure 5.2. Simulated supply current as a function of time.

As can be seen from the figures, the actual current consumption is 225 mA. Simulated current is -171 mA, where the negative sign shows the direction of the current. This is around 50 mA higher than the simulation presumes. Peak-to-peak amplitude of the measurement is not as stable as in the simulated plot. The difference between these two plots can be explained by parasitic elements of components and wires of the control circuit. Current flows through the inductor of the boost converter and inductor DC resistance will increase the power consumption. Old control board current consumption is measured using multi meter. Maximum measurement voltage of the N6705B DC power analyzer is 20.7 V and the old control board requires 48 V input supply voltage. Current consumption of 112.5 mA is measured for the old control board. Total input power can be calculated from the total input current with

$$P_{\mathrm{TOT}} = V_{\mathrm{IN}} I_{\mathrm{IN}}, \tag{5.1}$$

where V_{IN} is input voltage and I_{IN} is total input current. Power consumption for the old control board is

$$P_{\mathrm{TOT}} = 48\ \mathrm{V} \cdot 0.1125\ \mathrm{A} = 5.4\ \mathrm{W}. \tag{5.2}$$

Power consumption for the new control board is

$$P_{\mathrm{TOT}} = 12\ \mathrm{V} \cdot 0.225\ \mathrm{A} = 2.7\ \mathrm{W}. \tag{5.3}$$

The new control board consumes exactly 50% less power than the old device.

5.2. Output ripple

Antenna control board analog output voltage should be as stable as possible because the antenna radiation pattern will be affected by the output ripple. The output signal is measured using Hewlett Packard 54845A oscilloscope. Old control board output signal is shown in Figure 5.3. As can be seen from the figure, the voltage has high spikes and the peak-to-peak voltage mean is 1.52 V. Signal level is not stable so the antenna

radiation pattern will be not stable as well. New control board output signal is shown in Figure 5.4. Mean of peak-to-peak voltage is only 0.079 V so the output voltage is very stable.

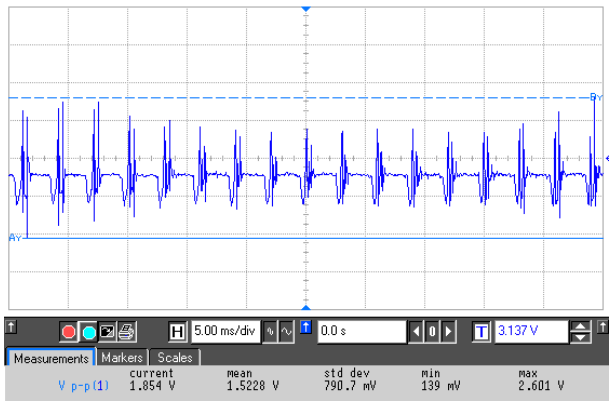

Figure 5.3. The output signal of the old antenna control board.

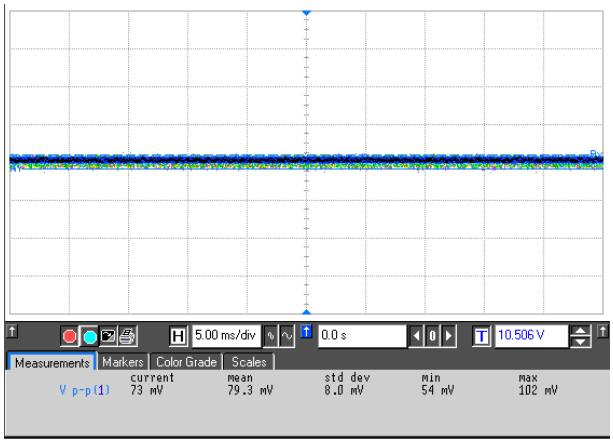

Figure 5.4. The output signal of the new antenna control board.

5.3. Linearity of the analog output signal

Linearity of the antenna control boards was measured by comparing input and output signals. System measurement setup is shown in Figure 5.5. Custom made program is used to give commands to WARP physical layer. This code first requests biasing voltage as a digital decimal value. This value is transformed to a binary value and send through Ethernet protocol to the WARP board using WARPLab reference design functions. Then the WARP board is transmitting two 8 bit digital signals to the antenna control board. Finally, an analog output of the antenna control board is measured using a voltage meter. The output voltage of the antenna control board is measured with each input signal level from 0 to 255. The measurement consists of 256 measurement points.

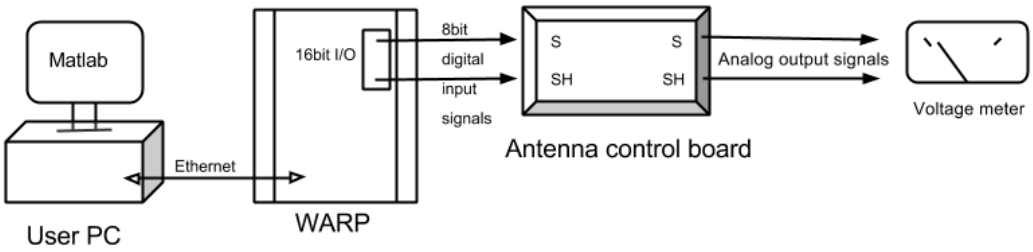

Figure 5.5. The block diagram of the measurement setup.

Old and new control board measurements are shown in Figure 5.6. As can be seen from the figure, new board input output signal is from 12 V to 30 V. Signal is very linear for input signal values 20 - 255. Old board output signal fluctuates and the analog voltage range is higher than in the new board, which makes it hard to find specific output voltages precisely. Both graphs are flat at the start. DAC output for low voltages is compromised when using voltage mode. New control board linearity is clearly better as can be seen from the figure. Every voltage level from 12.1 to 30 V can be generated with 0.1 V step size. Figure 5.6 can be used to match input decimal values with the wanted output voltage levels.

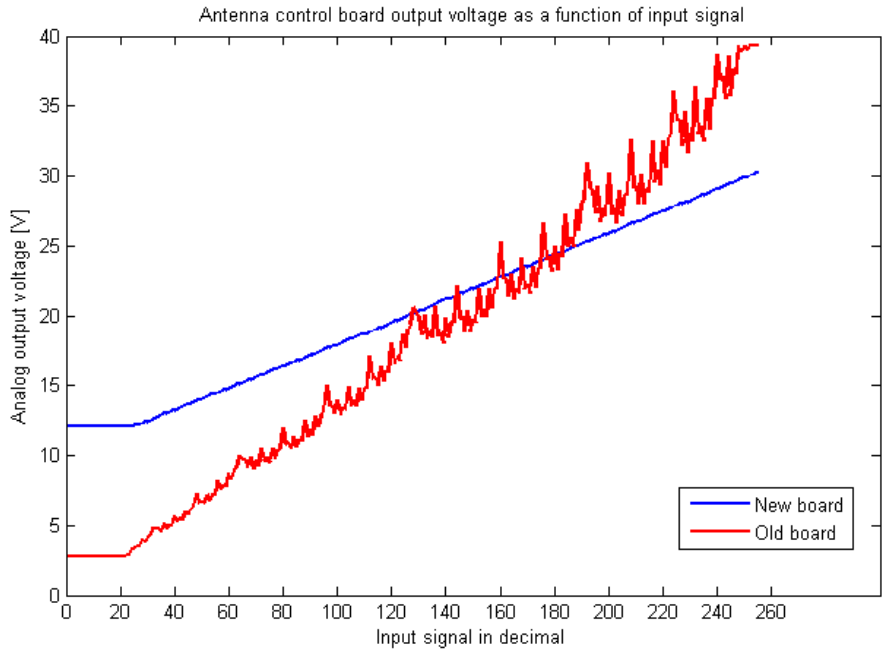

Figure 5.6. Antenna control board voltage as a function of input signal.

5.4. Antenna measurements

Operation principles of antenna control board are verified with antenna radiation pattern measurements. Antenna control board is set up in GPP-SDR system as shown in Figure 2.2. Reconfigurable leaky wave antenna is set up into the Starlab control unit. Antenna radiation pattern is controlled from the user PC via custom Matlab code. Also

physical layer code for the WARP is needed to define I/O pins and execute commands from user PC. These codes are programmed using available reference material offered by the WARP project website.

Reconfigurable leaky wave antenna is measured with Satimo Starlab multiprobe system. Satimo system antenna measurement frequency range is calibrated to perform from 0.8 GHz to 6 GHz with dynamic range of 70 dB. The Starlab control unit drives two positioning motors and an electronic scanning of the multiprobe array so that 3D antenna patterns can be measured. The Starlab is isolated with anechoic material so that the measured signals will not reflect from the environment. Vector network analyzer is used as an RF transmitter and receiver in the near field measurements. The obtained near field measurement result can then be post processed and transformed into far field results. [31]

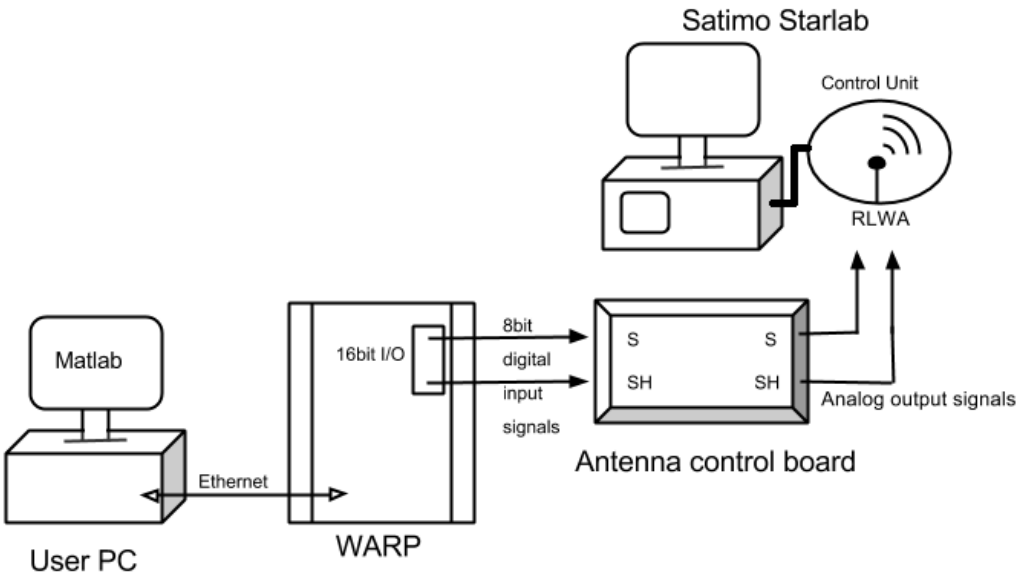

Figure 5.7. Block diagram of the antenna measurement set up.

Antenna measurement setup is shown in Figure 5.8. Starlab is on the right with RLWA inside. Laptop is used to change bias voltages by connecting it to WARP board via Ethernet cable. Antenna control board is connected to the WARP board by digital serial cable. Analog output of the control board is connected to the reconfigurable leaky wave antenna. Two sets of measurements are done using first the old antenna control board and then the new control board. Antenna is biased with different voltages to the frequency 2.44 GHz according Table 3 [18]. RLWA has two RF ports so the measurements are done using first Port 1 and repeated using Port 2.

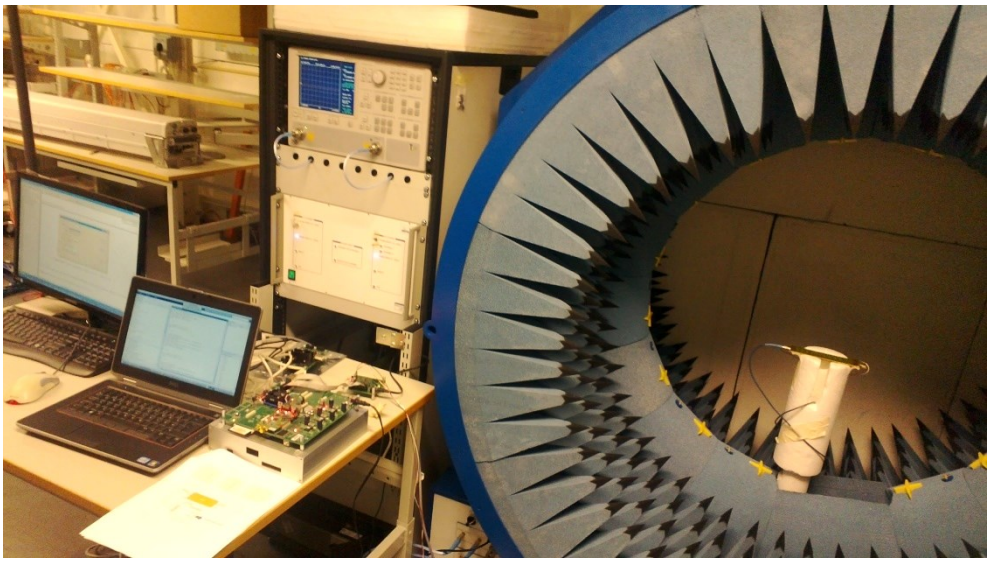

Figure 5.8. Antenna measurement setup.

Table 3. Bias voltages, respective beam angles and measured gains at 2.44 GHz

Angle [°]	**Port S voltage [V]**	**Port SH voltage [V]**	**Gain [dB]**
0	12	12	3.55
10	12.6	13.7	1.96
20	14.4	14.4	3.14
30	16.5	14.4	3.26
40	18.3	15.8	3.26
50	21.3	15.8	2.71
60	29.5	17.5	1.69

Radiation patterns can be plotted from different directions using Satimo software. Major planes are visualized in Figure 5.9 for the radiation pattern measurements. Antenna is represented in the middle of the figure. Ring outside the antenna represents the radiation pattern cutting and the red cone represents the viewer. All the following radiation pattern measurements are done in YZ-plane. It is the most informative plane since the voltage biased beam angle changes can be seen clearly.

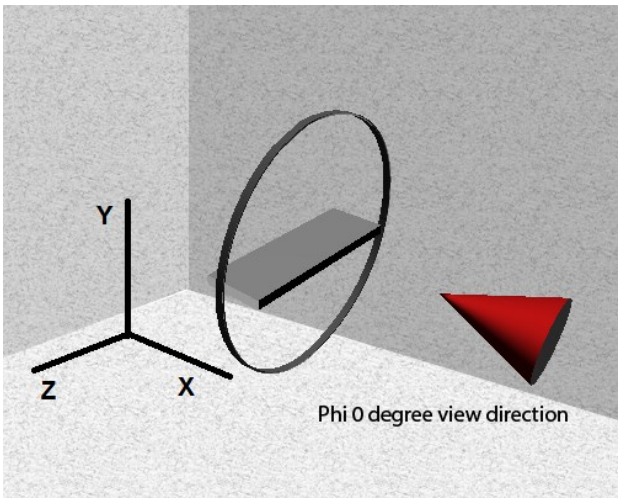

Figure 5.9. Planes for the antenna measurements.

Beam angle and gain are dependent on frequency and bias voltage. Frequency dependency can be seen in Figure 5.10 where radiation patterns are plotted as a gain function using 0° voltage biasing. Radiation patterns are from φ_{0° direction with frequencies 2.41 GHz to 2.46 GHz. Increment of frequency shifts the pattern direction from left to right and affects the gain slightly. Side lobe gains of the radiation patterns stay under -5 dB as the main lobes achieves over +2 dB gain.

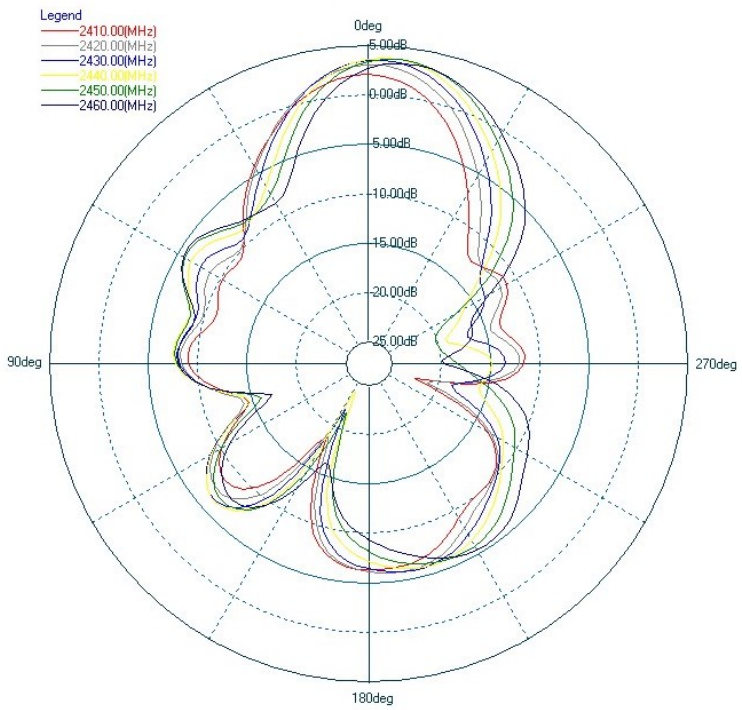

Figure 5.10. Antenna radiation pattern in YZ-plane.

Difference between the new and the old control board voltage biasing can be seen in Figure 5.11, where 60° biasing voltage is used. Radiation patterns are almost identical. This confirms that the two control boards are transmitting equal output voltages to the antenna. Marker is placed to point out where is 60° from the center. New control board radiation pattern has slightly more gain towards the 60° angle and the side lobes are smaller.

Radiation patterns for the new board in YZ-plane with 2.44 GHz frequency are shown in Figure 5.12 - Figure 5.15. Measurement from port 1 is shown in blue and port 2 in red color. Both ports are added in the same graph although the measurements where done separately. As can be seen from the figures, the voltage biasing affects the beam angle. Beam direction is towards the wanted angle, but the highest gain is not precisely directed to the wanted angle. The best results are for the 20° angle since the radiation pattern is very narrow and the highest gain is almost at the 20° angle. Higher biasing angles the gain starts to diminish and the radiation pattern becomes wider.

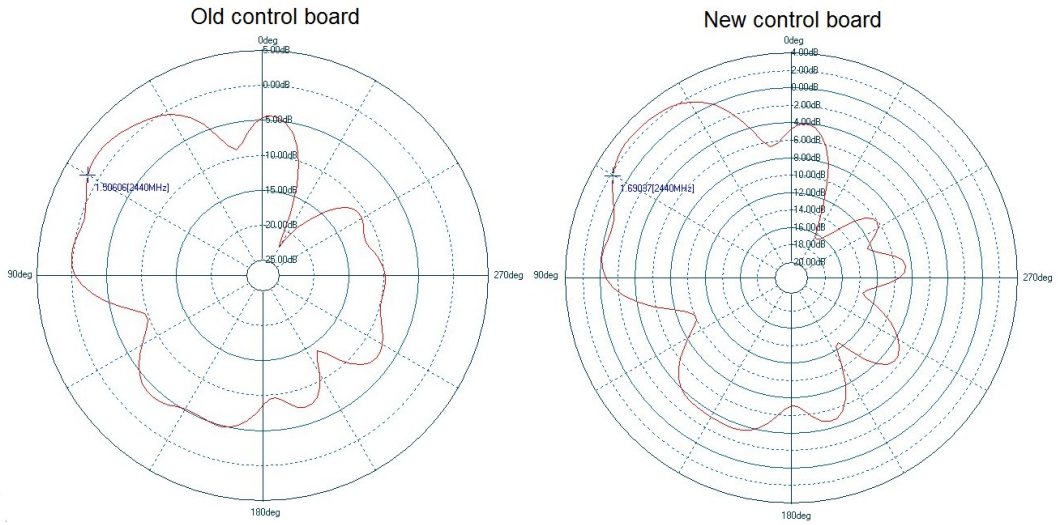

Figure 5.11. Radiation pattern comparison between new and old control board.

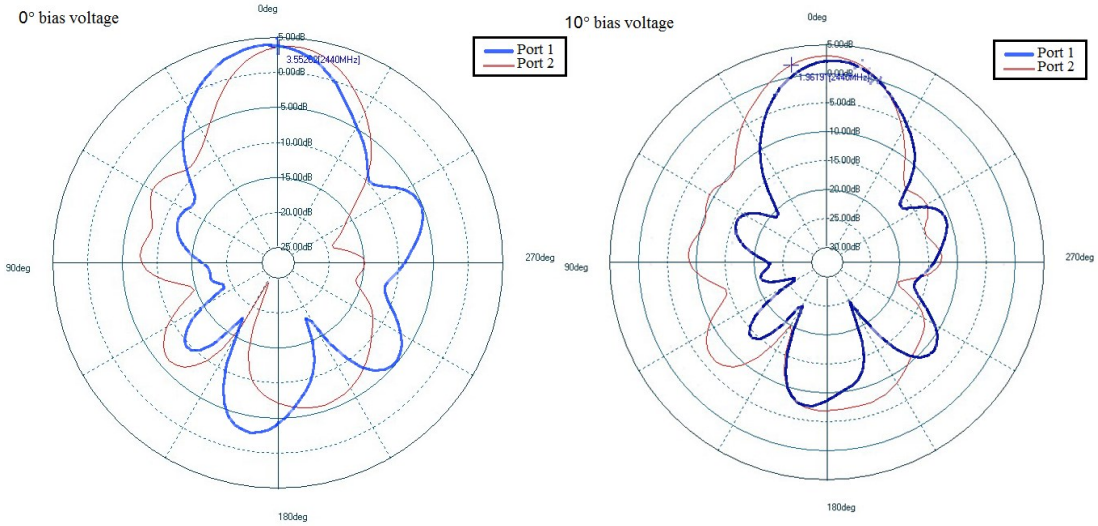

Figure 5.12. Radiation pattern with 0° and 10° angle biasing voltages.

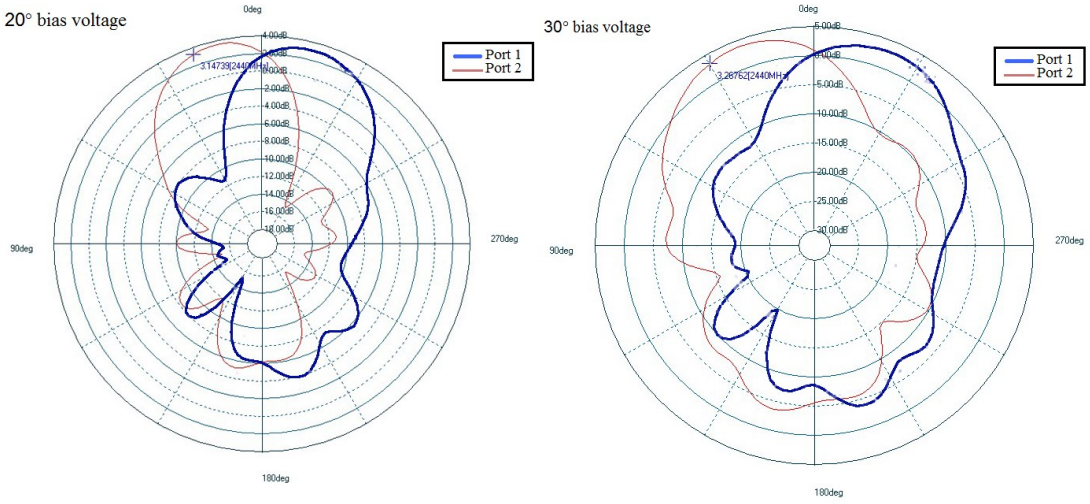

Figure 5.13. Radiation pattern with 20° and 30° angle biasing voltages.

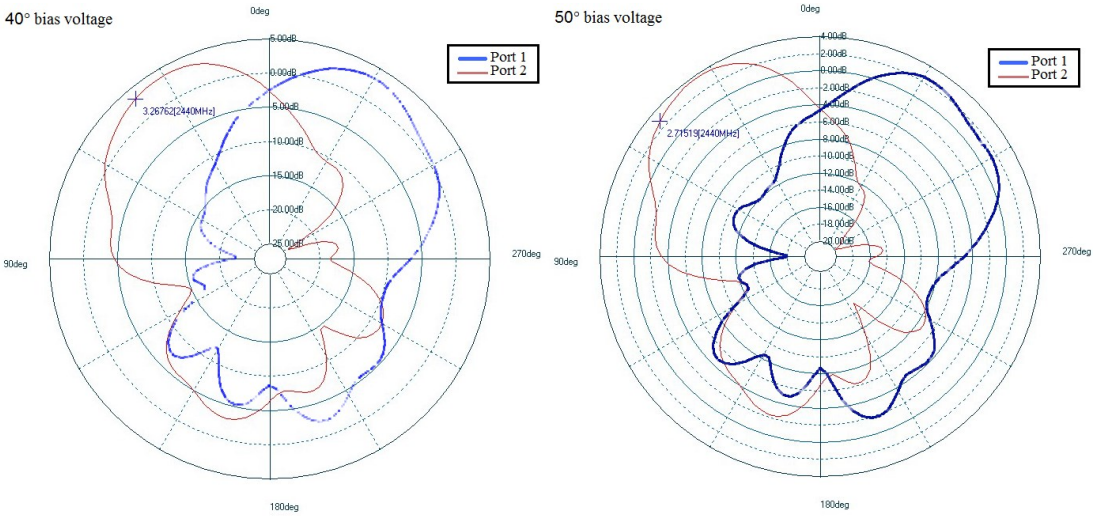

Figure 5.14. Radiation pattern with 40° and 50° angle biasing voltages.

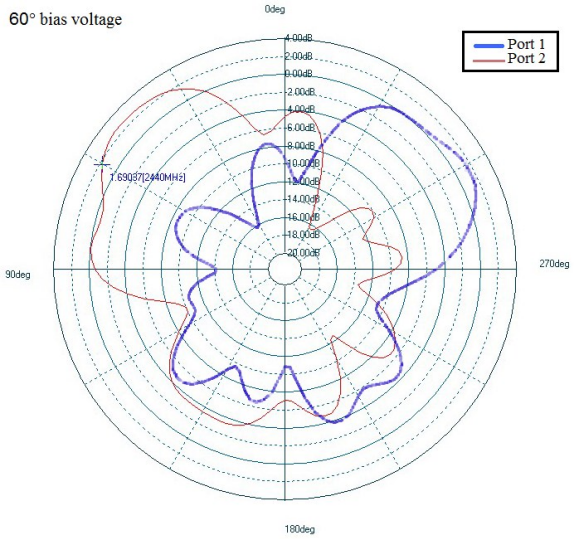

Figure 5.15. Radiation pattern with 60° angle biasing voltages.

6. DISCUSSION

Antenna control board was designed and implemented in this master thesis. Experience was gained in the subjects of circuit designing, analog and power electronics. Wireless Open Access Research Platform and especially WARPLab layer was studied in the design process. When implementing a circuit design, theoretical knowledge offers strong base for the work. Also, practical skills are needed in the manufacturing, debugging and programming phase. Choosing and finding the right components for the product requires strong background in electronics designing.

The circuit design had to be simulated and tested before the final version could be manufactured. The first versions of the antenna control board had problems with the regulator circuit and with digital to analog converter. Finding the problem could be achieved by isolating the different parts of the circuit from each other. Debugging the board was a lot of time consuming work. By applying theoretical knowledge of power electronics, the problem was identified to be a too small inductor in the regulator circuit. Inaccuracy issues with the DAC circuit was solved with an additional test board to confirm the operation of the DAC. The solution for the problem was to reroute the DAC entirely. This solution had its trade-off. Analog signal from the DAC should have been ideally from 0 V to 5 V, but the measurement showed 0.525 V to 5 V. This means that the output of the board would be 12.1 V to 30 V. Since the time was running out, decision was made to not replace the DAC.

Measurements were done for the designed antenna control board and the results were compared to the previous version of the control board to verify the operation. The designed control board is able to drive the reconfigurable leaky wave antenna with higher precision than the old version. Trade-off is that the new control board was designed just for this specific antenna type, so any other antenna with different voltage biasing might be inoperable with the designed board. The size of the control board is about 50% smaller than the previous version. Smaller size is managed to reach by using mainly surface mounted components. Power consumption of the designed circuit is reasonable for a wired device and is 50% lower compared to the old control board. The output of the new board can be set more precisely and with greater linearity than the output of the old board. Device outlook is more modern as compared to the older version and might help to attract attention in the demonstration environment. Output signal ripple of the designed control board is minimal in comparison to the old design. However, the old antenna control design acted as a reference and allowed comparative measurements to be performed throughout the design process..

Antenna pattern measurements verify the designated operation principle of the reconfigurable leaky wave antenna. Compared to the old design no great differences are found. Antenna beam direction can be reconfigured from 0° to 60° with 10° steps. Antenna radiation pattern measurements were done using the previous measurements to configure the biasing voltages. This affects greatly the results. More accurate radiation patterns could be found out by measuring the antenna with additional biasing voltage values. However this is very time consuming and there are more than 32000 combinations of antenna biasing voltages available. The best method to find out the most accurate biasing voltage value combinations would be to use the already measured biasing voltages as anchor points. Then tweaking the biasing voltage and measuring the radiation pattern would be the right way to predict the most accurate biasing voltage.

Further research towards performance of reconfigurable directional antennas can be started with integrating this GPP-SDR setup as a part of bigger reconfigurable antenna system. Testing and implementing new wireless communications applications is proposed by using the designed antenna control board. Implementing a design where novel algorithm adjusts the antenna biasing voltage with feedback from received signal strength indicator is suggested. Algorithm should scan the horizon and find the optimal beam angle. Proposed algorithm could be implemented first to the Matlab environment so the user PC would do all the calculations. Measuring the possible gains of beam scanning algorithms for reconfigurable antenna systems is advised. Additional control boards can be manufactured using this thesis as a source for instructions.

7. SUMMARY

The goal of this thesis was to design and implement a control board for a reconfigurable leaky wave antenna. The designed antenna control board allows further research towards reconfigurable antenna systems utilized with the wireless open-access research platform WARP. The implemented antenna control circuit was verified with several performance measurements.

Thesis work started with analysis of the given device specifications. The designed control board should replace an older version of the control board. Size of the control board should be smaller than the older version. Designed device should also be able to operate using 12 V DC power supply. Digital input of the control board was two 8 bit signals and output should be able to DC bias a reconfigurable leaky wave antenna. The output of the old device was measured to vary between 10 – 30 V which should be the operating range of the new design. Antenna radiation pattern should be able to be controlled between 0 - 60° with 10° steps. Linearity and precision of the antenna control board output signal were key factors in the design work. Power consumption was also taken into account in the design phase.

Regulator circuit was designed first for the antenna control board. By using boost converter to step-up 12 V power supply voltage, provided 30 V analog output signal. LT3461 boost converter was chosen as a result of SPICE circuit simulations where boost converter circuit operation were confirmed. Digital to analog conversion was done using TLC7524 DAC. Since no simulation tool was available for the DAC, a test circuit was built to verify correct operation. DAC was able to convert 8 bit digital signal to 0 – 5 V analog signal. Additional amplifiers were needed to convert the analog signal to the 10 – 30 V voltage as was required in the specifications. Multipurpose operational amplifier ISL28210 was chosen for the amplification. Amplification was also simulated using SPICE tool to verify the correct operation of the designed circuit. Power indication led, power switch and digital voltage meter were included as additional features for the designed control board. The antenna control board was implemented in PCB using mainly surface mounted components. The board layout was designed using Cadsoft Eagle PCB software. Components were attached to the board using solder paste and reflow oven. Size of the control board was only 50% of the older version.

Verification of the built device included power consumption, output ripple, output linearity and antenna measurements. Power consumption of the new device was 50% lower than consumption of the older version of the device. Output signal ripple of the designed control board was very low and the signal waveform was smooth as a function of time. Antenna measurements confirmed the correct operation of the designed board. The measurement was done using Matlab software to access WARP digital I/O which was connected to the designed control board. Reconfigurable leaky wave antenna was biased with the designed control board. The RLWA radiation pattern was measured using Satimo Starlab system. The measurements were compared to the radiation patterns produced by the old antenna control circuit. The measurements indicate that the new control board is able to DC bias the RLWA properly. Linearity and precision of the new control board were significantly better than in the old design.

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9. APPENDICES

Appendix 1. Antenna control board layout

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