MECHANICALLY FLEXIBLE INTERCONNECTS (MFIs) FOR LARGE SCALE HETEROGENEOUS SYSTEM INTEGRATION

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MECHANICALLY FLEXIBLE INTERCONNECTS (MFIs) FOR LARGE SCALE HETEROGENEOUS SYSTEM INTEGRATION

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DEDICATION

Dedicated to my wife,

Juan Sun,

my daughter,

Elsa Yunyi Zhang,

and my parents,

Zhiquan Zhang and Shuahua Li,

for their endless love and support.

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SUMMARY

In this research, wafer-level flexible input/output interconnection technologies, Mechanically Flexible Interconnects (MFIs), have been developed. First, Au-NiW MFIs with 65 μm vertical elastic range of motion are designed and fabricated. The gold passivation layer is experimentally verified to not only lower the electrical resistance but also significantly extend the life-time of the MFIs. In addition, a photoresist spray-coating based fabrication process is developed to scale the in-line pitch of MFIs from 150 μm to 50 μm. By adding a contact-tip, Au-NiW MFI could realize a rematable assembly on a substrate with uniform pads and a robust assembly on a substrate with 45 μm surface variation. Last but not least, multi-pitch multi-height MFIs (MPMH MFIs) are formed using double-lithography and double-reflow processes, which can realize an MFI array containing MFIs with various heights and various pitches.

Using these advanced MFIs, large scale heterogeneous systems which can provide high performance system-level interconnections are demonstrated. For example, the demonstrated 3D interposer stacking enabled by MPMH MFIs is promising to realize a low profile and cavity-free robust stacking system. Moreover, bridged multi-interposer system is developed to address the reticle and yield limitations of realizing a large scale system using current 2.5D integration technologies. The high-bandwidth interconnection available within interposer can be extended by using a silicon chip to bridge adjacent interposers. MFIs assisted thermal isolation is also developed to alleviate thermal coupling in a high-performance 3D stacking system.

CHAPTER 1

INTRODUCTION

With the rapid growth of portable electronics as well as high-performance computing systems, it is becoming increasing challenging to realize a large scale multi-functional system using state-of-the art CMOS and traditional packaging technologies.

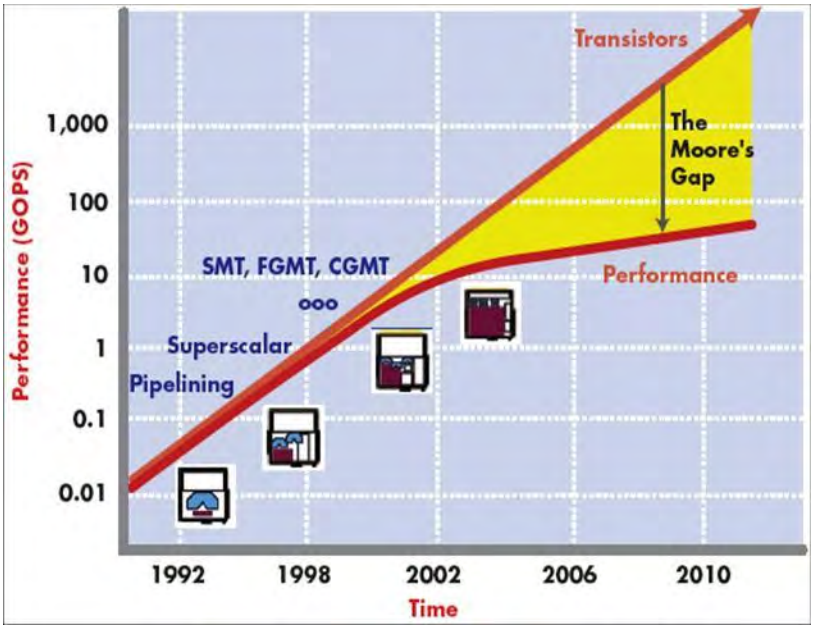


Figure 1: The performance gained from Moore's law is becoming saturated.

With respect to large scale integration using CMOS technology, as shown in Figure 1, the performance gained from node-to-node scaling is somewhat becoming saturated due to the current leakage and thermal management issues as well as other challenges [2]. In the meantime, the fabrication cost, R&D cost and design cost rise exponentially [3] because of the increasing complexity of leading edge nodes (Figure 2). Therefore, it's challenging to extend system performance and scale using traditional system on chip (SoC) approach [4]. Recently, the rapid adoption of chips with multiple cores and multiple threads per core in computing systems has sustained performance

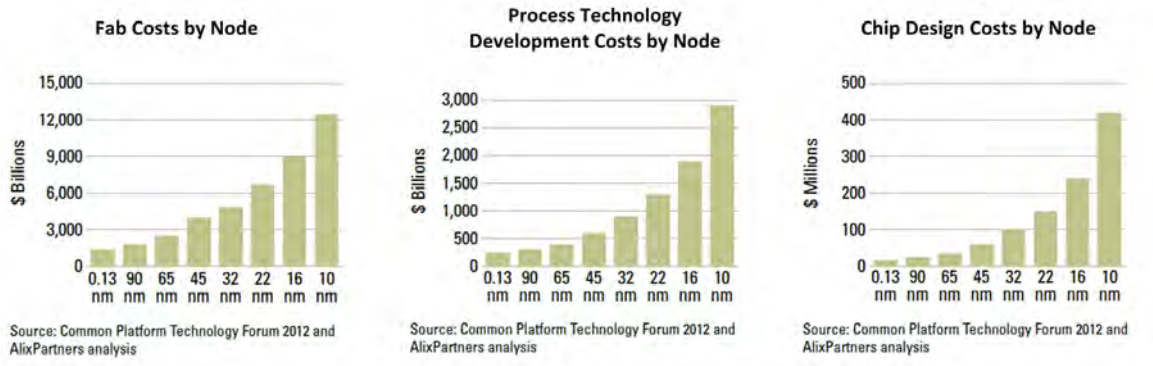


Figure 2: The fabrication cost, R&D cost and design cost rise exponentially with the technology node scaling.

scaling while keeping chip power consumption within manageable limits. While there is less need to constantly increasing on-chip clock frequency, this approach requires increasing the off-chip I/O bandwidth [5], [6], as shown in Figure 3 [6]. Therefore, a novel interconnection platform which can integrate various high-performance chips and provide high off-chip bandwidth is highly needed.

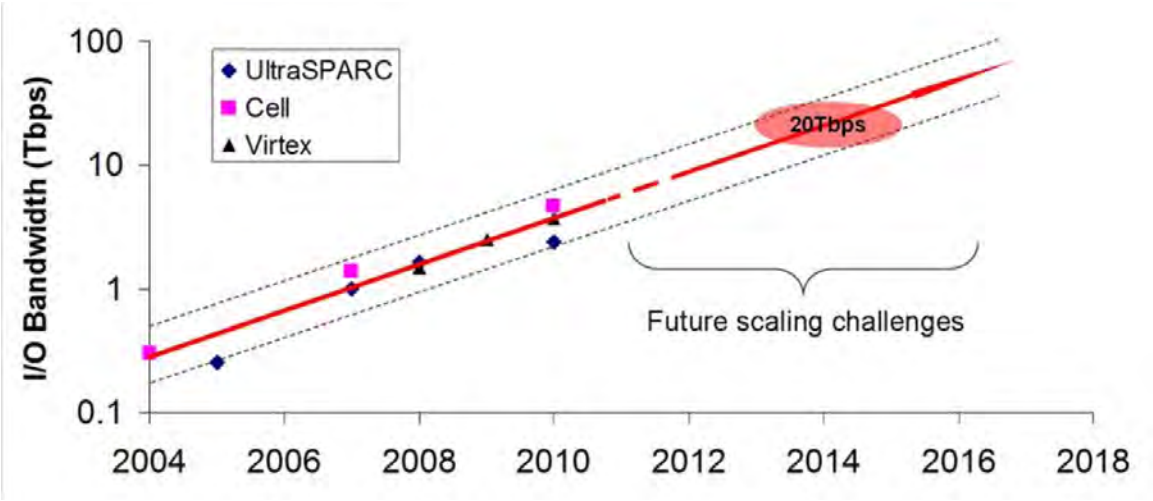


Figure 3: I/O bandwidth scaling.

With respect to traditional packaging technologies, such as package-on-package (PoP) (Figure 4) [7], it can integrate various components and materials in one package. However, the I/O pitch provided by the organic substrate, which is approximately 0.2-0.5 mm [8], is not sufficient for high-bandwidth off-chip communication. In addition,

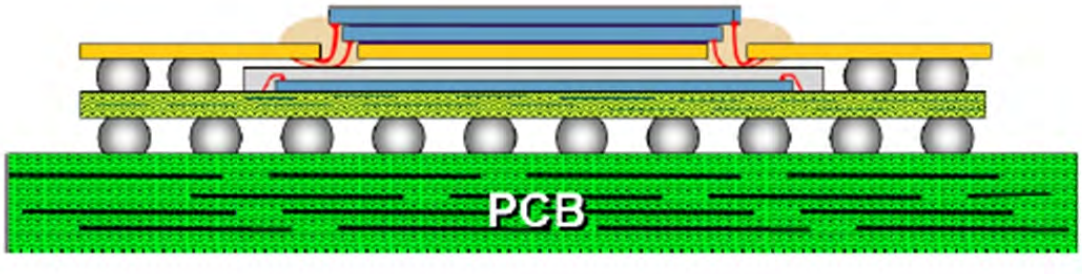


Figure 4: Package-on-package (PoP)technology.

package stacking will induce a severe thermal dissipation [9] and warpage [10], [11], which limits the number of stacking layers therefore the system scale and performance.

Therefore, the research reported in this dissertation focuses on how to demonstrate large-scale high-performance silicon systems using novel interconnect and integration technologies.

1.1 Interposer Based Large Scale Heterogeneous System

Interposer based integration platforms are discussed in this section to address the needs of large-scale high-performance heterogeneous systems. Using an interposer platform, a single large SoC chip is replaced by several integrated functional chips. By doing so, the design and fabrication complexities of realizing a large SoC are circumvented.

1.1.1 Ceramic Interposer Based Large Scale System

Interposer based heterogeneous integration has been investigated for a number of decades for a wide range of applications. Initially, ceramic and organic interposers were used to provide interconnection between the integrated chips [12]–[17]. For example, ceramic interposer is still adopted in the recently released IBM z-microprocessor using multi-chip module (MCM) technology, as shown in Figure 5 [18]. Since high-density wiring is not available on a coarse ceramic substrate, a large number of ceramic wiring planes (15 metal planes for the z-microprocessor interposer) are used to provide

Figure 5: IBM z-microprocess using MCM technology with ceramic interposer.

the large off-chip bandwidth. However, as the number of ceramic planes increases, the system bandwidth benefit gained by adding planes decreases while the cost rises significantly. Therefore, ceramic interposer based system integration is not promising as the system size expands.

1.1.2 Silicon Interposer Based Large Scale System

As shown in Figure 6 [19], thanks to state-of-the art CMOS technology, silicon interposer package can provide much larger I/O density and therefore interconnect bandwidth density relative to ceramic and organic interposer packages. Recently, Xilinx developed a microsystem platform using silicon interposers to enable high-density wiring between dice to circumvent the challenges in manufacturing large capacity FPGAs, as shown in Figure 7 [20]–[23]. Similar high performance FPGA systems using interposer with TSVs were demonstrated by Altera as well [24]–[26].

Moreover, a silicon photonic interconnection platform, called the 'macrochip', has been investigated by Oracle to realize a system with an ultra-low energy-per-bit and large-system bandwidth, as shown in 8 [27]–[31]. In the macrochip, the electrical die

and silicon photonic die are integrated using rematable interconnects, and the high-performance off-chip communication is achieved using optical waveguides on a large silicon interposer.

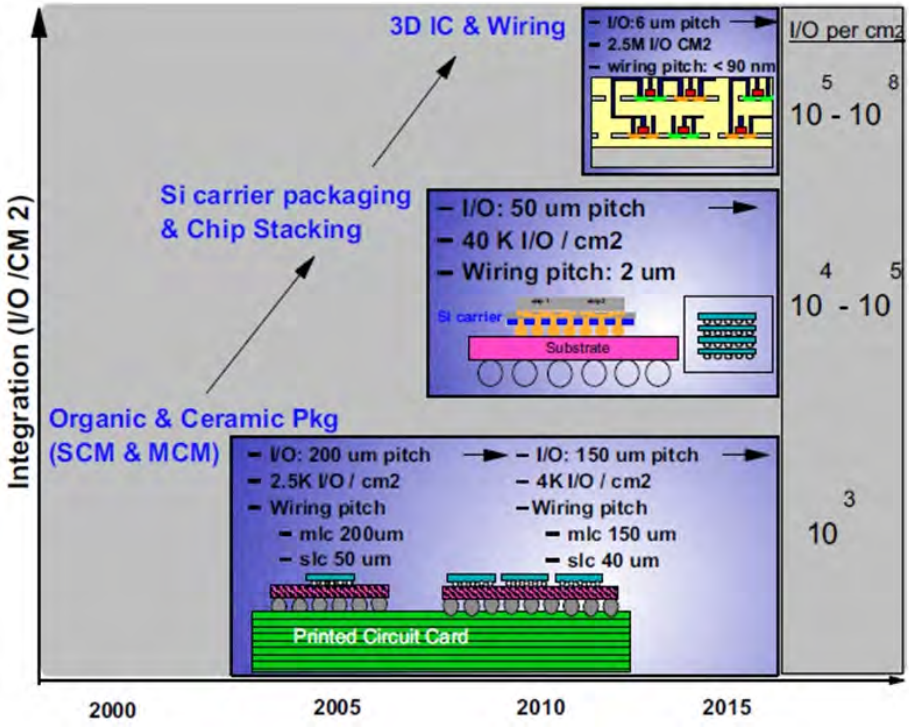


Figure 6: I/O density comparison: Ceramic/organic interposer, silicon interposer and 3D IC.

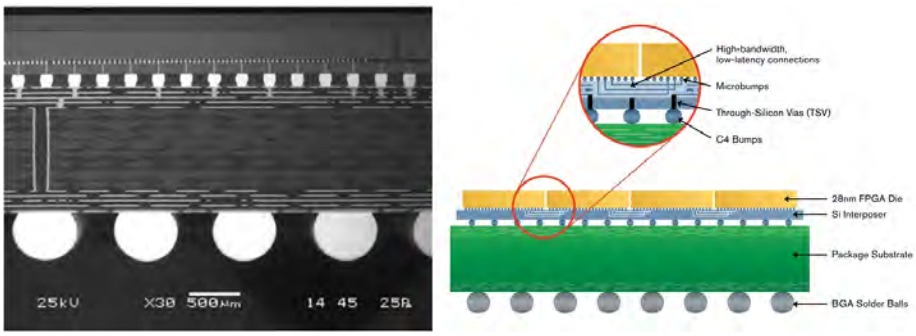


Figure 7: Advanced FPGA from Xilinx using silicon interposer based 2.5D integration.

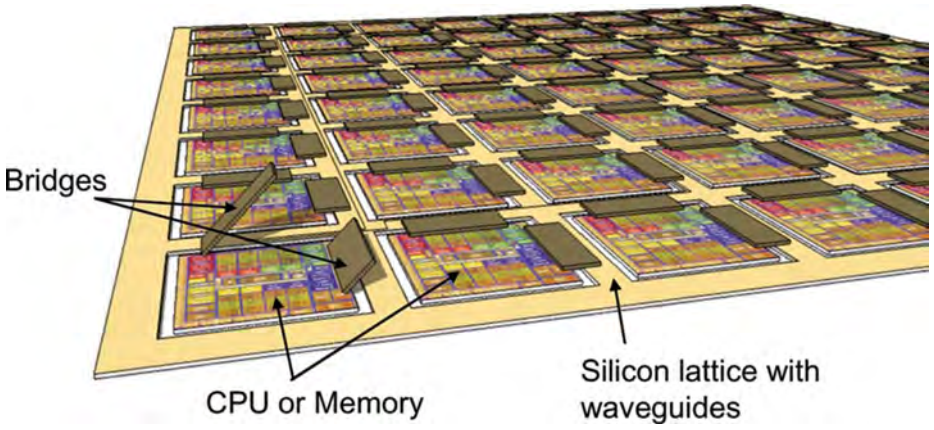


Figure 8: Oracle macrochip leverages 2.5D integration and silicon photonics technology.

1.1.3 Proposed Multi-interposer System

As discussed above, silicon interposer based 2.5D integration provides a promising high-performance off-chip interconnection. However, the performance and cost of 2.5D integration systems are limited by the following factors:

1. As shown in Figure 9 (a), when silicon interposers are used, a secondary package substrate is typically inserted to fan out the high density I/Os (C4 bumps) on the interposer to the low density BGA I/Os on the motherboard. Another reason for this need is due to the challenges associated with the coefficient of thermal expansion (CTE) mismatch between a large silicon interposer and an even larger organic motherboard. However, the insertion of the package substrate increases the system form factor and also degrades electrical performance.

2. The high-performance interposer interconnections are only available for chips mounted on a single interposer. Given that the size of interposers is limited by the reticle size as well as cost, there exists a limit on the number of chips that can be integrated. Therefore, an innovative interconnection platform between interposers is needed to extend interconnect benefits over a large-scale system.

3. As the number and diversity of integrated chips increases, the cost and yield

of a heterogeneous system suffers from the increased complexity of system-level testability.

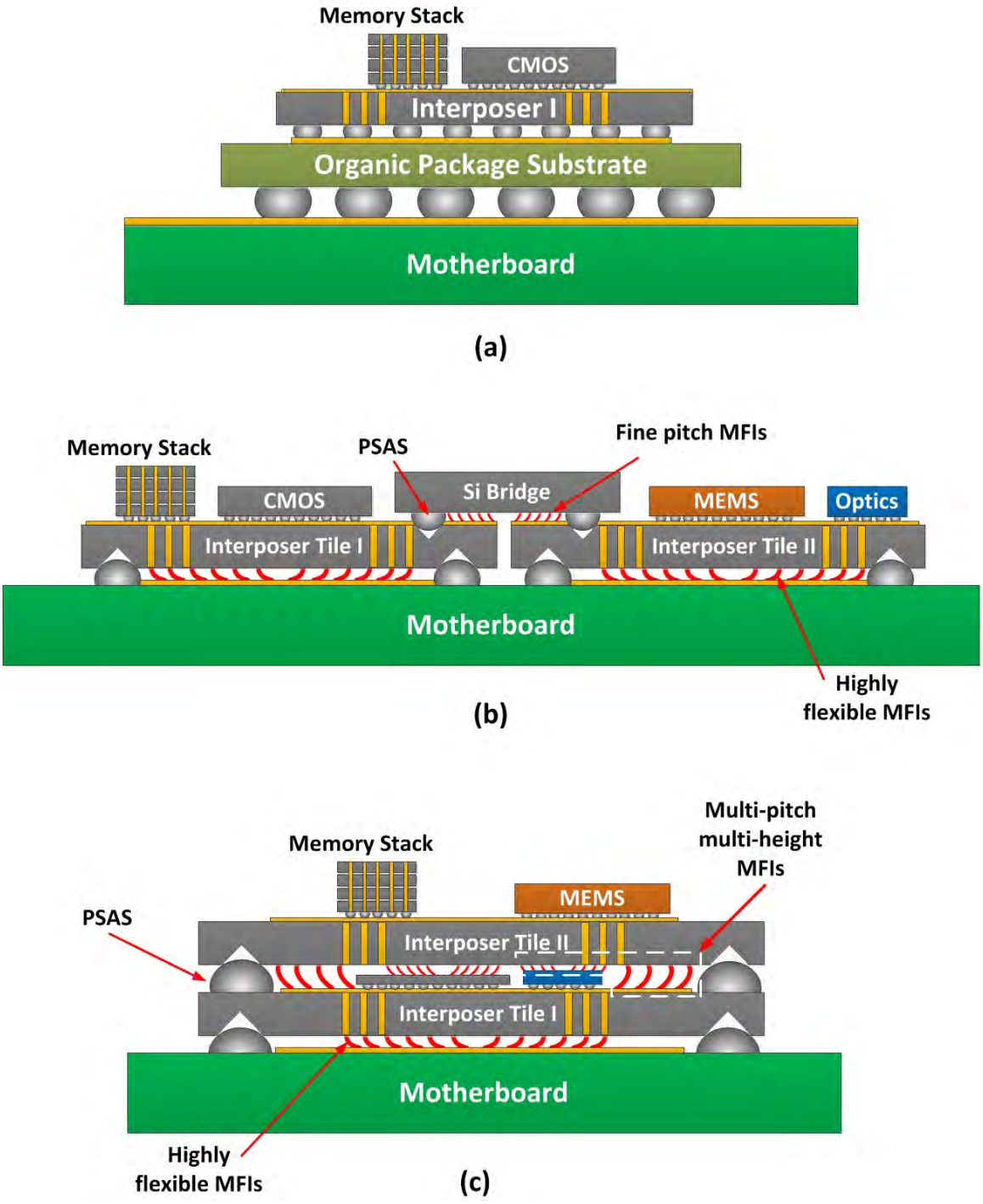


Figure 9: Based on the traditional 2.5D interposer technology (a), large scale heterogeneous systems can be realized by MFIs based interconnection technology : (b) laterally expanded silicon interposer tiles and bridges and (c) 3D interposer stacking.

4. Since chips are typically permanently soldered, there is a lack of repairability, which can increase system cost.

5. All chips are thermally coupled with each other through the solder joints and underfill layer, which could aggravate thermal management challenges in high performance system.

Therefore, novel multi-interposer platforms enabled by various flexible interconnect technologies are proposed in this thesis to enable the large-scale high-performance heterogeneous system, as shown in Figure 9 (b) and (c).

Figure 9 (b) illustrates the bridged multi-interposer system, which connects multiple side-by-side interposer tiles using silicon bridge chips to form a large-scale system. The key features of this system are: 1) low-cost and high-accuracy self-alignment assembly of the components is obtained using Positive Selft Alignment Structures (PSAS) and pyramid pit pairs [32]; 2) using the flexible I/Os between the silicon interposer tile and organic substrate, the silicon interposer tile may be directly mounted on the motherboard, which not only shortens the interconnect length, increases interconnect density, and minimizes impedance discontinuities, but also lowers the package thickness; 3) the flexible I/Os between the silicon interposer tile and bridge can overcome the die thickness variation and CTE mismatch induced warpage, therefore ensure a reliable fine pitch tile/bridge interconnection; 4) the system level electrical interconnects enabled by MFIs and PSAS are rematable, therefore system-level testing can be accomplished before the permanent integration of all silicon interposer tiles and bridges; and 5) the underfill-free packaging could thermally decouple the integrated chips, which is helpful in system thermal management.

Figure 9 (c) illustrates a 3D interposer stacking approach in which multiple stacked interposers are interconnected using flexible I/Os with various heights and pitches. The flexible I/Os and self-alignment structures used in the bridged multi-interposer system are adopted for this 3D interposer stacking system, which enables

self-alignment, direct bonding, system-level testing, and enhanced thermal management capabilities as discussed earlier. Besides those, similar to 3D IC integration, interposer stacking shortens the interconnect length between integrated chips and interposers and lowers the system profile by embedding chips between interposers.

As discussed above, self-alignment features and flexible I/Os are the two key technologies to enable the envisioned system in Figure 9. Since self-alignment assembly using PSAS was previously demonstrated in [32], this dissertation focuses on the flexible interconnects. In order to develop flexible I/Os that can be effective in the various systems listed above, four key requirements must be fulfilled: 1) fine-pitch high-density interconnects, 2) large elastic vertical deformation for sufficient flexibility and reusability, 3) high-contact force for low-contact resistance temporary interconnection, and 4) long lifetime (for usefulness and reliability).

1.2 Flexible Interconnects Technologies

Various flexible interconnect technologies have been investigated over the past decades that were initially used to address the challenges in assembling a silicon chip onto an organic substrate. The previously reported flexible interconnect technologies are summarized as follows:

1. Flexible interconnects formed on or within a low-modulus polymer substrate, such as the WAVE Package [33], Floating Pads Technology [34] , and Sea of Leads (SoL) [35] as shown in Figure 10. The compliances of these flexible interconnects are dominated by the young's modulus of the polymer and thus, cannot be adjusted in a wide range.

2. Modified wire-bond based technology, such as MicroSpring Technology [36]. These microsprings could be mass manufactured in low-cost by modifying the bonding process of wedge wire bonder. The drawbacks are relatively large I/O pitch and low adjustable compliance range.

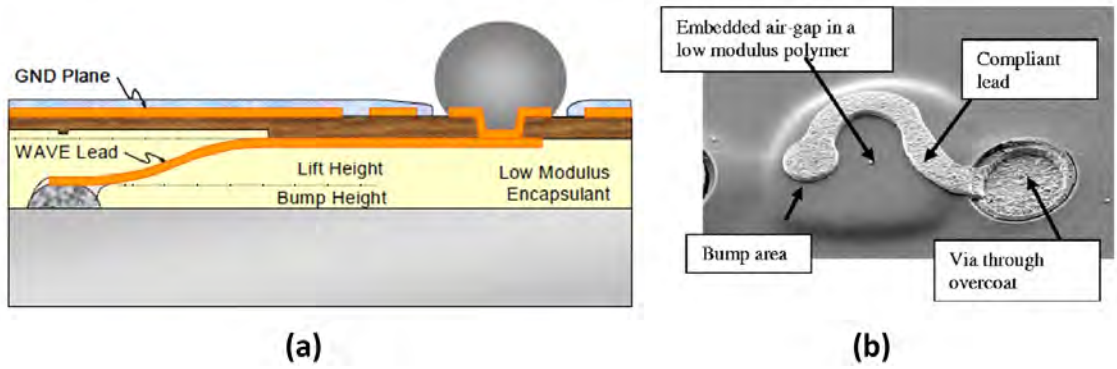


Figure 10: Flexible interconnects formed on polymer substrate: (a) Wave Package and (b) Sea of Leads.

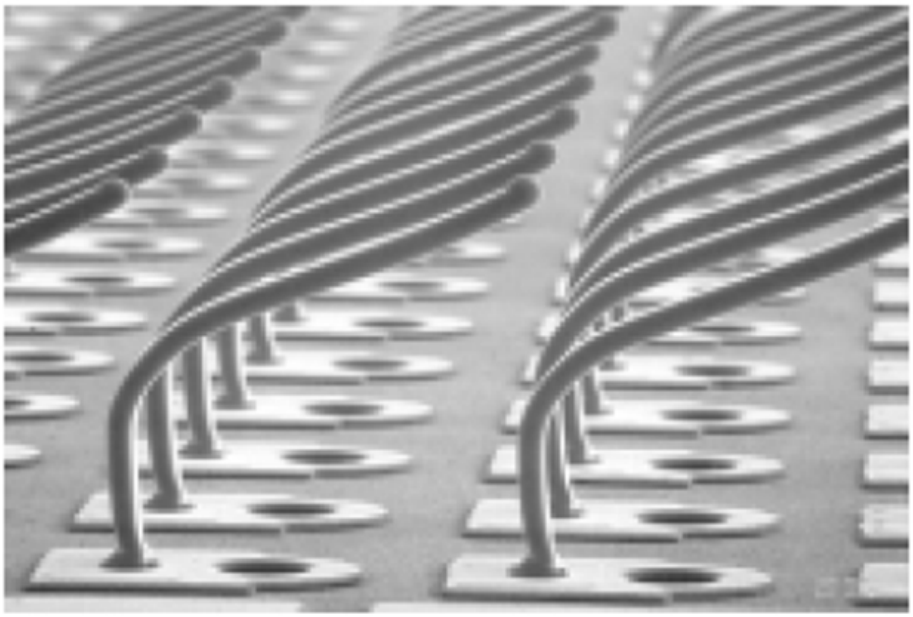


Figure 11: MicroSpring Technology.

3. Stress engineered metal interconnects, such as rematable spring interconnect [31], [37], [38], J-spring [39] and coiled micro-spring [40]. The fairly complex fabrication process limits the throughput and density of these stress engineered metal interconnects.

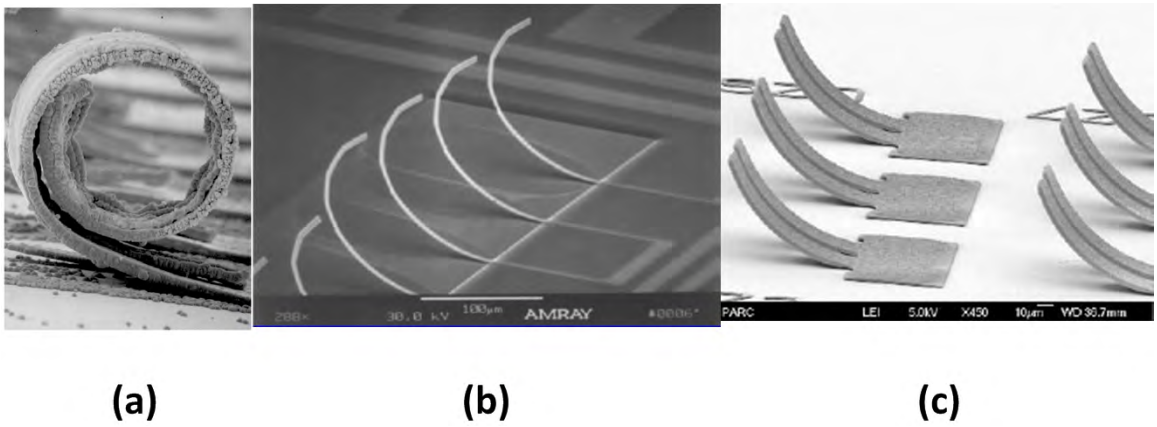


Figure 12: Stress engineered metal interconnects: (a) coiled micro-spring, (b) J-spring and (c) rematable spring.

4. 3D free standing micro-spring technology, such as β-Helix [41], G-Helix [42]–[44], Flex-Connects [45]–[47], multi-path interconnects [48]–[50], nickel tungsten (NiW) micro-springs [51] and curved copper compliant die-package interconnects [52]. These 3D free standing micro-springs are fabricated by lithography processes, therefore a relatively fine pitch array can be obtained using wafer-level low cost fabrication. In addition, the compliance of micro-spring structure can be easily adjusted in a wide range by tuning the thickness of the free standing structures.

Concerning the four requirements listed in Section 1.1.3, it is very challenging to realize the proposed system using these previously reported flexible interconnect technologies. A novel copper-based 3D curved mechanically flexible interconnect (MFI) technology was previously reported by Yang et al. [53], [54]. Despite using a tapered and curved geometrical profile to uniformly distribute and reduce the maximum stress

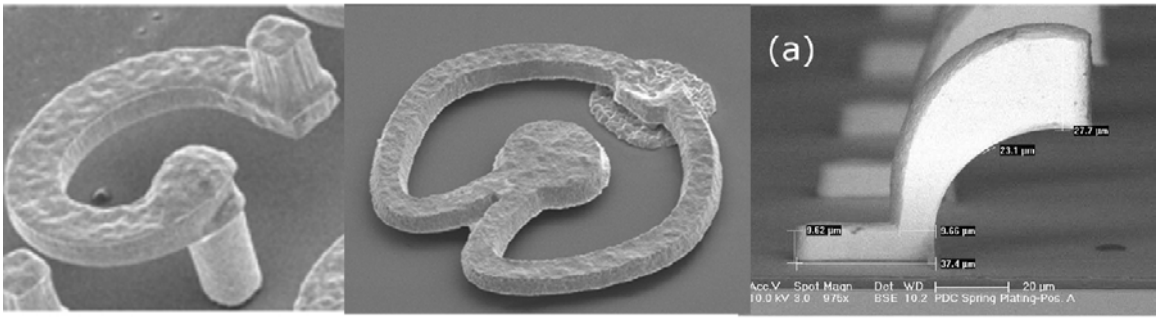


Figure 13: 3D free standing micro-spring: (a) G-helix, (b)β-Helix and (c) curved copper compliant die-package interconnects .

during deformation, the low-yield strength of the material used, Cu (yield strength of 200 MPa [55]), makes it difficult to extend the vertical elastic range of deformation beyond 20 μm. This material limitation was overcome recently by the use of NiW, which has a significantly higher yield strength (as high as 1.9 GPa [56]). The usefulness of the material was demonstrated in [51], [56], where flexible interconnects with a larger vertical elastic range of deformation (up to 40 μm) were developed and demonstrated. However, due to the readily oxidizing nature of Cu as well as NiW, it has not yet been shown that it can be used in real applications with a reasonable reliability, especially in applications where the interconnect structures are not encapsulated in an inert environment.

1.3 Research Statement

The objective of this research is to develop a set of advanced flexible interconnect technologies and apply them to various large-scale high-performance heterogeneous systems. Specifically, the flexible I/O technologies developed in this thesis have the following key features:

1. Wafer-level batch fabricated, have a large contact force, long life-time, and large vertical elastic range of motion to enable silicon interposer and organic (or other

substrate with large surface variation) interconnection.

2. Fine pitch to enable dense I/O array for high-bandwidth communication.

3. Can be fabricated with various heights and pitches, which can form a high-performance and low-profile stacking system.

4. Are used for the demonstration of two proposed novel high-performance heterogeneous systems (i.e. bridged multi-interposer system, Figure 9 (b), and 3D interposer stacking system), Figure 9 (c)).

5. Enable innovative thermal management benefits from underfill elimination.

1.4 Organization

The organization of the research reported in this dissertation is listed as follows:

- Chapter 2: Development of a Au-NiW MFIs with large contact force, vertical range of motion and enhanced life-time. FEM modeling, fabrication and characterization of mechanical and electrical properties are included.

- Chapter 3: Novel photoresist spray-coating based fabrication process is developed to form fine pitch MFIs with a large vertical height.

- Chapter 4: Au-NiW MFIs with contact tip are developed to enhance the temporary assembly capability and charaterized by various assembly tests.

- Chapter 5: MFIs with multi-height and multi-pitch are developed using double-lithography and double-reflow processes.

- Chapter 6: 3D interposer stacking system is demonstrated using the MPMH MFIs technology.

- Chapter 7: Bridged multi-interposer system and the related key enabling technologies are reported.

- Chapter 8*: A novel surface tension assisted ball-in-pit self population is demonstrated, which is critical to enable a large scale high accurate self-alignment.
- Chapter 9: An MFI assisted thermal isolation technology is developed to mitigate the thermal coupling between stacked dice, which is critical for 3D integration.
- Chapter 10: Conclusion and possible extensions of the thesis are described.

* The work presented in Chapter 8 was completed when the author was a 2012 visiting summer intern in the Photonics, Interconnects and Packaging group in Oracle Labs in San Diego and was published in the ECTC 2013 proceedings [1] and is reported as-is in this thesis as Chapter 8 with permission from Oracle.

CHAPTER 2

HIGHLY ELASTIC GOLD PASSIVATED MFIs

2.1 Introduction

In order to develop mechanical flexible interconnects (MFIs) to enable direct silicon interposer mounting on an organic substrate as discussed in Chapter 1, three key requirements must be fulfilled: 1) large elastic vertical range of motion for sufficient flexibility and reusability, 2) high-contact force for low resistance temporary interconnection, and 3) long lifetime for practical usefulness and reliability. However, due to limitations stemming from either material property, design, and/or fabrication processes, it is challenging for the traditional compliant I/O technologies [33]–[36], [39]–[42], [45], [51], [52] to fulfill all these requirements. In this chapter, a novel flexible interconnect technology, Au-NiW MFIs, are reported to address these issues.

This chapter will first describe the design methodology of Au-NiW MFI, which is based on the analysis of material selection and mechanical FEM simulation. In addition, a wafer-level batch fabrication process of Au-NiW MFIs is developed. The key steps of the fabrication process are: 1) high sacrificial polymer dome formation, 2) NiW electroplating, and 3) electroless gold passivation layer deposition. The tall sacrificial dome helps to extend the vertical gap of the MFI up to 65 μm, the NiW with high yield strength ensures the full depth deformation of the MFI is elastic, and the gold passivation layer preserves the mechanical and electrical characteristics of the MFI during their field use. At last, the outstanding mechanical and electrical properties of Au-NiW MFI are verified by various indentation and resistance measurements.

2.2 Design Methodology and FEM Analysis on MFIs with Tapered Geometry

In order to operate within the elastic deformation range and therefore enable reusability of MFIs, the maximum local internal stress of MFIs during deformation should not exceed the material yield strength, which is defined as the stress beyond which the material starts to deform plastically and cannot recover the original profile. However, given that a relatively large contact force is necessary for temporary interconnection to ensure reliable electrical interconnection, the maximum local internal stress is expected to be relatively large, which might cause plastic deformation. Therefore, fabricating MFIs using a material with high yield strength is a cornerstone to the design of MFIs.

An optimized geometry should also be considered to maximize the range of elastic deformation. As discussed in the previous work of Yang et al. [53], [54], [57], thinner and longer MFIs help in decreasing the internal stress and maintaining a maximum stress value that is below the yield strength of the MFIs material for a given deformation range. However, both the thickness and length of the MFIs cannot be manipulated easily as they will be constrained by practical, electrical, and mechanical performance requirements. Thinner MFIs lead to lower contact force, and given that a relatively large contact force is necessary for applications that require temporary interconnection, thicker MFIs are required to ensure reliable electrical interconnection (i.e., low contact resistance). In addition, in order to achieve high bandwidth interconnections, a high I/O density is desirable in many applications, which implies that shorter MFIs are needed. Therefore, instead of thinning and elongating the MFIs, an optimized width profile is adopted to lower the maximum internal stress while maintaining a large contact force.

Considering the two main factors of MFIs design as discussed above (material property and geometry optimization), the following is a brief design strategy adopted

for the proposed MFIs:

1. Form the MFIs by choosing a material with high yield strength, which affords the MFIs to have a large internal stress for a desired contact force while maintaining elastic deformation. This issue is reported in [51], [56].

2. Follow the design strategy developed in previous work of Yang et al. [53], [54], [57] to optimize the 3D tapered and curved geometry of the MFIs to attain a maximum internal stress below the yield strength of the material.

3. MFIs must be passivated in order to ensure the reliability in many practical applications. Electroless gold plating is adopted in this work to form the passivation layer.

Below, we elaborate on the two key points above.

2.2.1 High Yield Strength Metal Alloy-NiW

Cu has been used extensively for various flexible interconnect technologies [34], [40]–[42], [45] because of the high conductivity, high electromigration resistance and established low-cost electroplating techniques. However, the yield strength of Cu is relatively low (less than 200 MPa [55]). Thus, it limits the range of elastic deformation. Tungsten, on the other hand, has a yield strength of up to 1.37 GPa [58]. However, it cannot be efficiently deposited using electroplating, which is the most convenient low-cost method to deposit thick metal film (few microns and above) at room temperature. NiW, a Ni alloy with nano-crystal structure developed in [51], [56], is an ideal material for MFIs due to its high yield strength of up to 1.9 GPa and its ability to be deposited using electroplating. Besides the high yield strength, which is critical for large elastic deformation, the latter is also particularly important for low-cost manufacturing since a thick metal layer is typically needed.

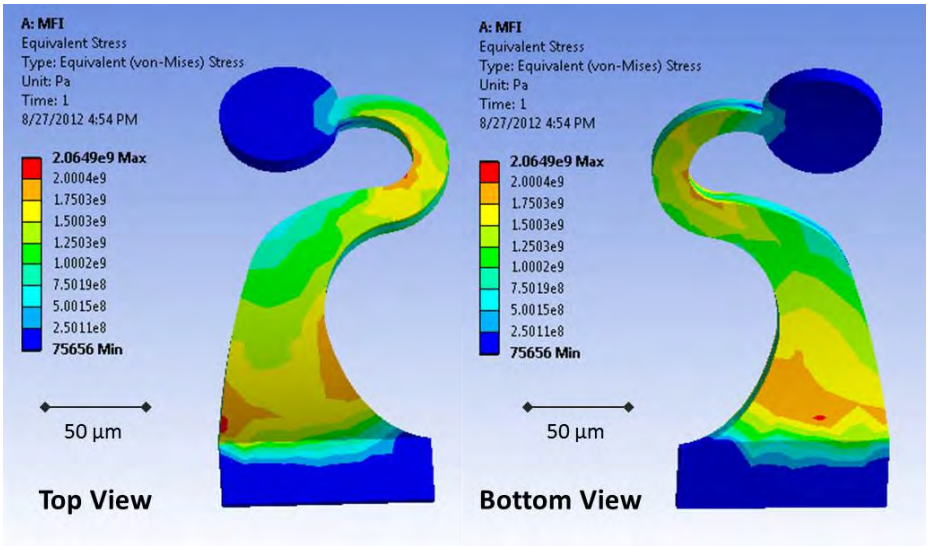


Figure 14: von Mises stress FEM simulation of 50 μm vertically deformed NiW MFI. The inner stress is uniformly distributed.

2.2.2 FEM Analysis of MFI with Tapered Geometry

A tapered MFI width design based on the principles developed by Yang et al. [53], [54], [57] is used here to distribute the stress uniformly and provide larger vertical range of motion. FEM simulations of the stress distribution within a tapered NiW MFI with 50 μm vertical deformation are shown in Figure 14. The simulated MFI is 9 μm thick and occupies a footprint of 120 μm by 200 μm. The FEM simulations performed by ANSYS Workbench software package show that at 50 μm vertical deformation, the maximum local von Mises stress is 2.06 GPa, which is close to the yield strength of NiW. The simulated reaction force at this value of deformation is 6.0 mN.

Since the gold passivation layer is very thin (0.5μm) and soft compared to NiW, the impact of the gold passivation layer on the mechanical deformation of the MFI is neglected in the simulations, which is verified experimentally in Section 2.4.

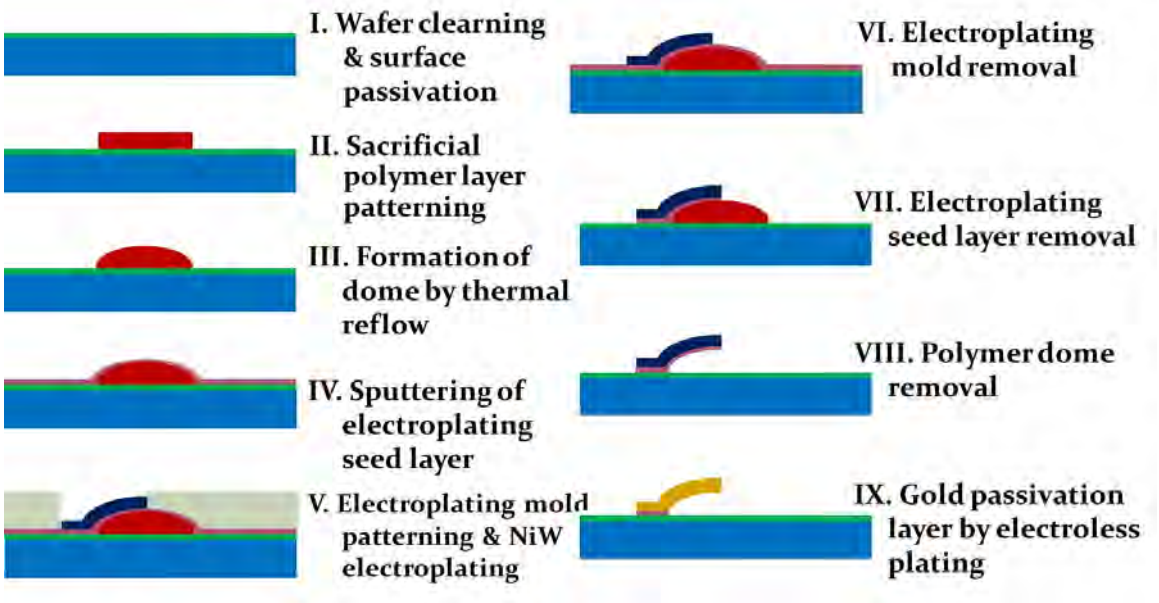
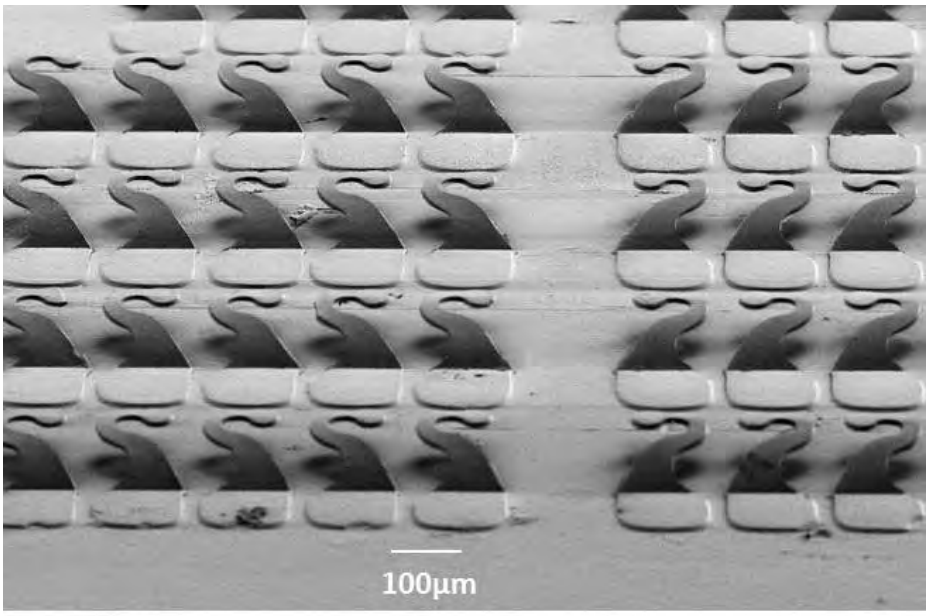


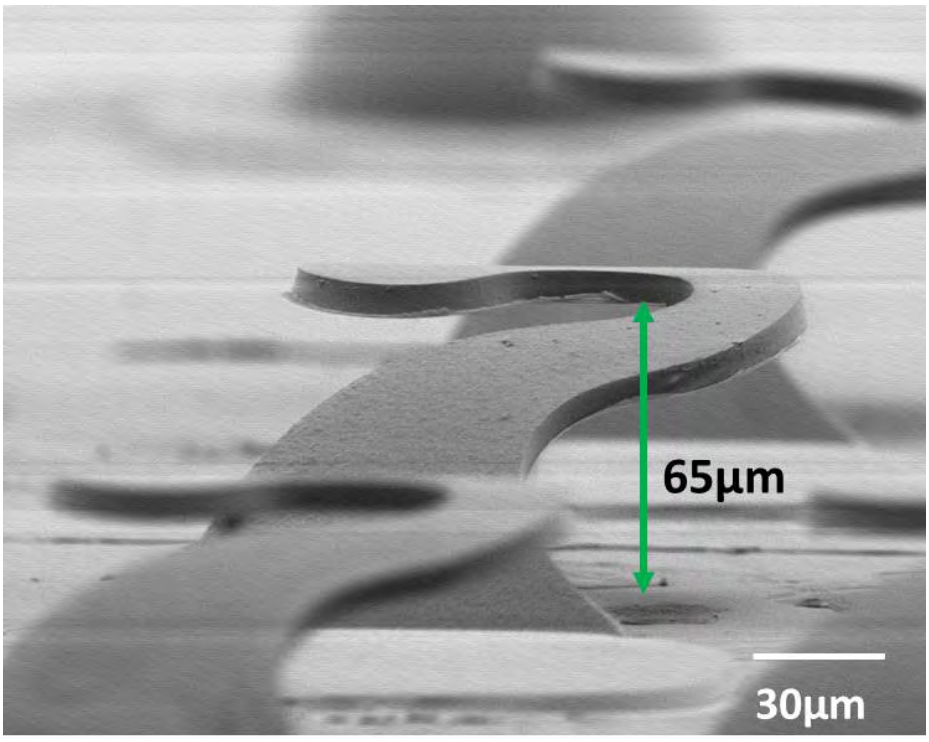
Figure 15: Process flow for Au-NiW MFIs

2.3 Spin-coating Based MFIs Fabrication

The fabrication of the flexible interconnects, as shown in Figure 15, is similar to the Cu based MFI process described in [53], [54], [57], and similarly, this process requires only two photolithography steps. The first photolithography step is used to pattern a sacrificial polymer layer on the substrate, which transforms into a dome following a thermal reflow process. The second photolithography step is used to pattern a photoresist electroplating mold on the surface of a Ti/Cu/Ti seed layer, which covers the sacrificial polymer. After the electroplating of the NiW MFIs, the electroplating mold, the seed layer and sacrificial polymer dome are removed subsequently leaving behind free-standing MFIs with a 120 μm by 200 μm footprint and 65 μm Z-axis gap, as shown in Figure 16. Finally, a gold passivation layer is deposited on the free-standing MFIs using electroless plating, as shown in Figure 17. Below, we elaborate on the key process steps.



(a)



(b)

Figure 16: Gold passivated NiW MFIs with 65 μm vertical gap

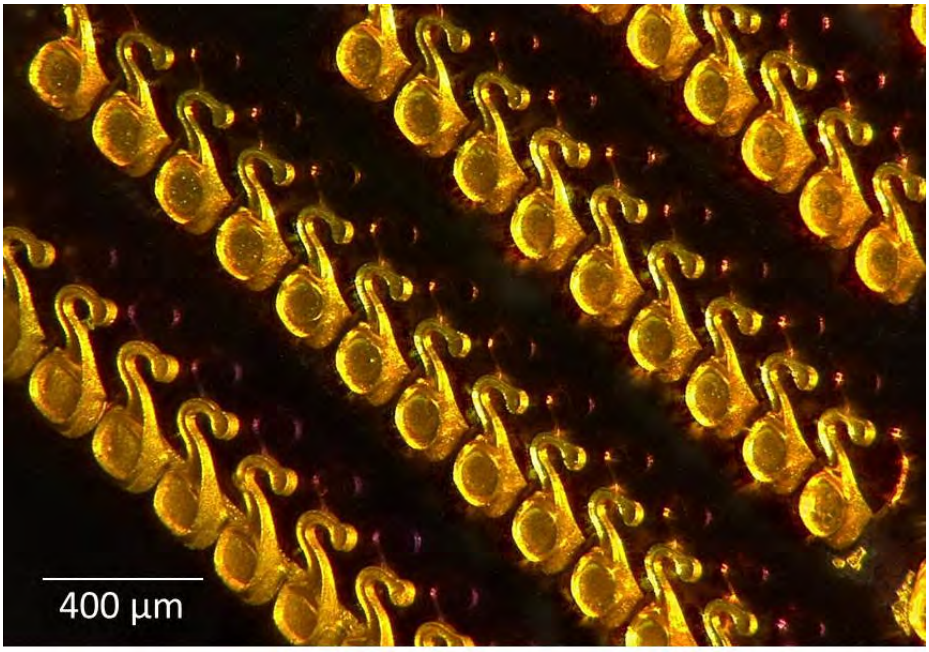


Figure 17: Optical micrograph images of MFIs with 65 μm vertical gap after electroless gold passivation

2.3.1 Sacrificial Polymer Dome

The height of the polymer dome determines the maximum vertical deformation range. Depending on the polymer dome thickness, single or multiple polymer spin-coating steps may be needed. A single spin coat of the polymer layer was sufficient to attain the 20 μm vertical gap for the Cu MFIs in prior work [57]. In order to reach higher vertical gap, multiple coatings were used to obtain a 45 μm thick polymer layer, which after reflow, transforms into a polymer dome with a height of 65 μm. Since the sacrificial polymer dome is very thick, gradual post bake followed by natural cool down must be used to avoid solvent out-gassing and polymer dome cracking.

2.3.2 Electroplating Mold

In order to form MFIs by electroplating, more than 50 μm thick conformal photoresist film needs to be coated and patterned on the Ti/Cu/Ti seed layer covering the substrate with polymer domes. Note that the polymer domes result in 65 μm surface

variation. The main challenge in the formation of the electroplating mold is dose control. This is true because after spin-coating, the thickness of the photoresist layer on the peak of the domes is thinner than the photoresist thickness in the valley between the domes. Thus, the variation of photoresist thickness leads to different dose requirements for exposure across the wafer. Since the photoresist is very sensitive to under exposure, which typically occurs in the valley since it is the thickest photoresist region, the exposure dose for the whole wafer is tuned based on the requirement of the valley.

2.3.3 Electroplating and Release

Since the yield strength of Cu is too low to afford the large vertical range of motion, NiW is used to form the MFIs using electroplating, which is a fast, low-cost, and CMOS compatible approach. Traditional Ni sulphate based NiW electroplating electrolytes require high electroplating temperature (approximately 90°C) and harsh alkaline solution (pH8), which may not be compatible with some Si processing. In addition, the internal stress of NiW eletrodeposited by a Ni-sulphate based bath is high and can easily lead to cracks. Therefore, Ni sulfamate based electrolytes are used in our work. The components of NiW MFIs with gold passivation layer are verified by X-Ray Fluorescence (XRF), as shown in Figure 18.

For a given bath temperature and pH value, the thickness of MFIs is mainly controlled by the electroplating time. Since MFIs with various thickness values were formed in different batches for testing, the MFIs thickness will be clearly noted along all data reported in the following sections. After electroplating, the polymer dome and seed layer are removed to yield 3D free standing NiW MFI with a footprint of 200 μm by 120 μm and vertical gap of 65 μm (Figure 16).

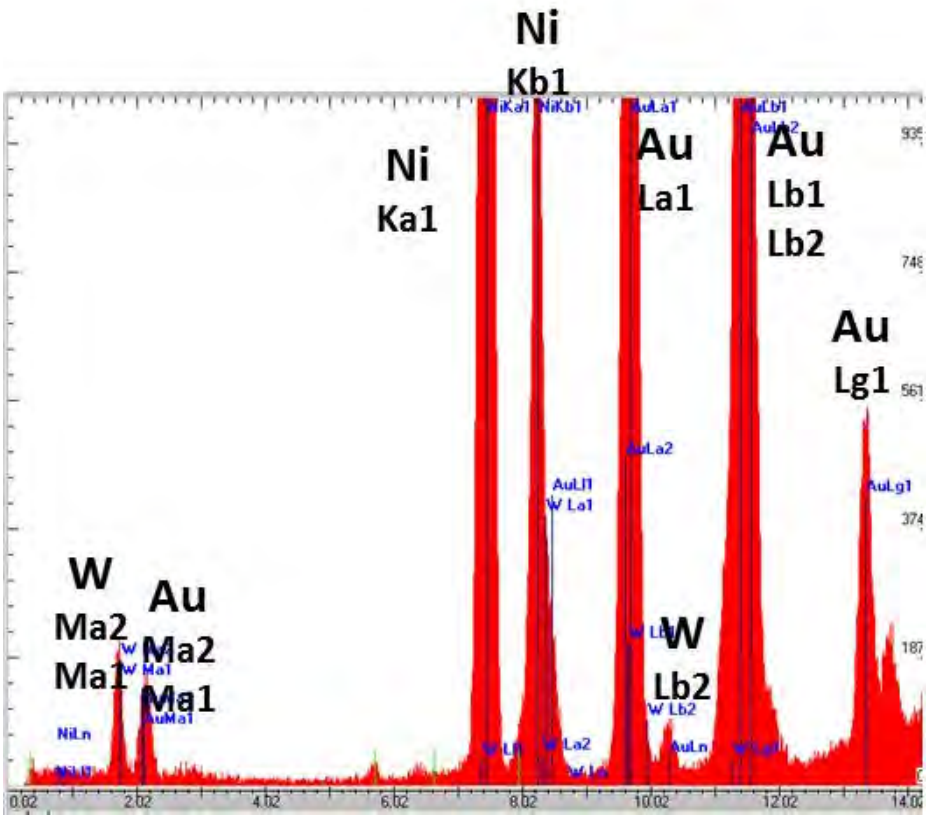


Figure 18: Au-NiW MFIs components verification by x-ray fluorensence (XRF)

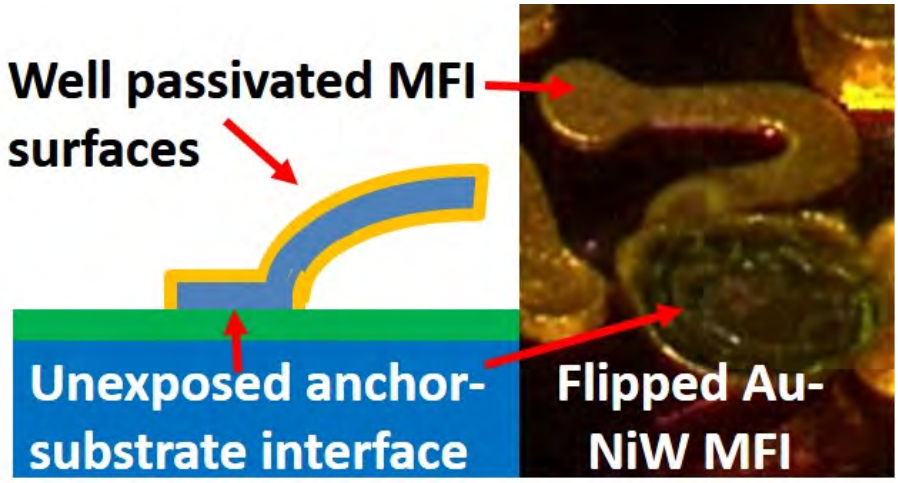


Figure 19: A gold passivation layer is deposited on all exposed surface of the NiW MFIs by electroless plating

2.3.4 Electroless Gold Passivation Layer

The passivation layer, which determines the durability of the lead, is critical for flexible interconnects. For both Cu and NiW MFIs, oxidation and corrosion of the exposed metal to the ambient will significantly shorten the MFIs' lifetime. Therefore, a passivation layer is mandatory for MFIs exposed to the ambient in order to preserve the mechanical and electrical properties during their lifetime. As shown in Figure 19, a gold passivation layer is deposited on the surface of the NiW MFIs by electroless plating. Since the deposited gold results from a chemical reaction on all conductive surfaces, all exposed MFI surfaces are passivated as required in this application. One of the gold passivated NiW MFIs was flipped using tweezers (large force was applied to detach the MFI) to illustrate the passivation layer uniformity (Figure 19). The only uncoated part of the MFI, as expected, is the unexposed interface between the anchor of the MFI and the substrate. Compared with other methods for passivation (for example, polymer coating) there are significant benefits: 1) simple and low-cost processing since photolithography is not needed, 2) high conductance, which is important in lowering the MFI resistance, especially for NiW MFI, and 3) longer lifetime.

2.4 Mechanical and Electrical Characterization of MFIs

2.4.1 Mechanical Characterization

Multiple indentations were employed to determine the mechanical properties of Au-NiW MFIs, including the maximum elastic deformation range and the corresponding contact force and compliance. The results of the mechanical characterization of the MFIs are reported in this section.

Indentation testing of the MFIs was carried out using a Hysitron TriboIndenter, as shown in Figure 20 (a). Each indentation cycle includes a forward and a backward step. In the forward step, a predefined forced is applied on top of a free standing MFI

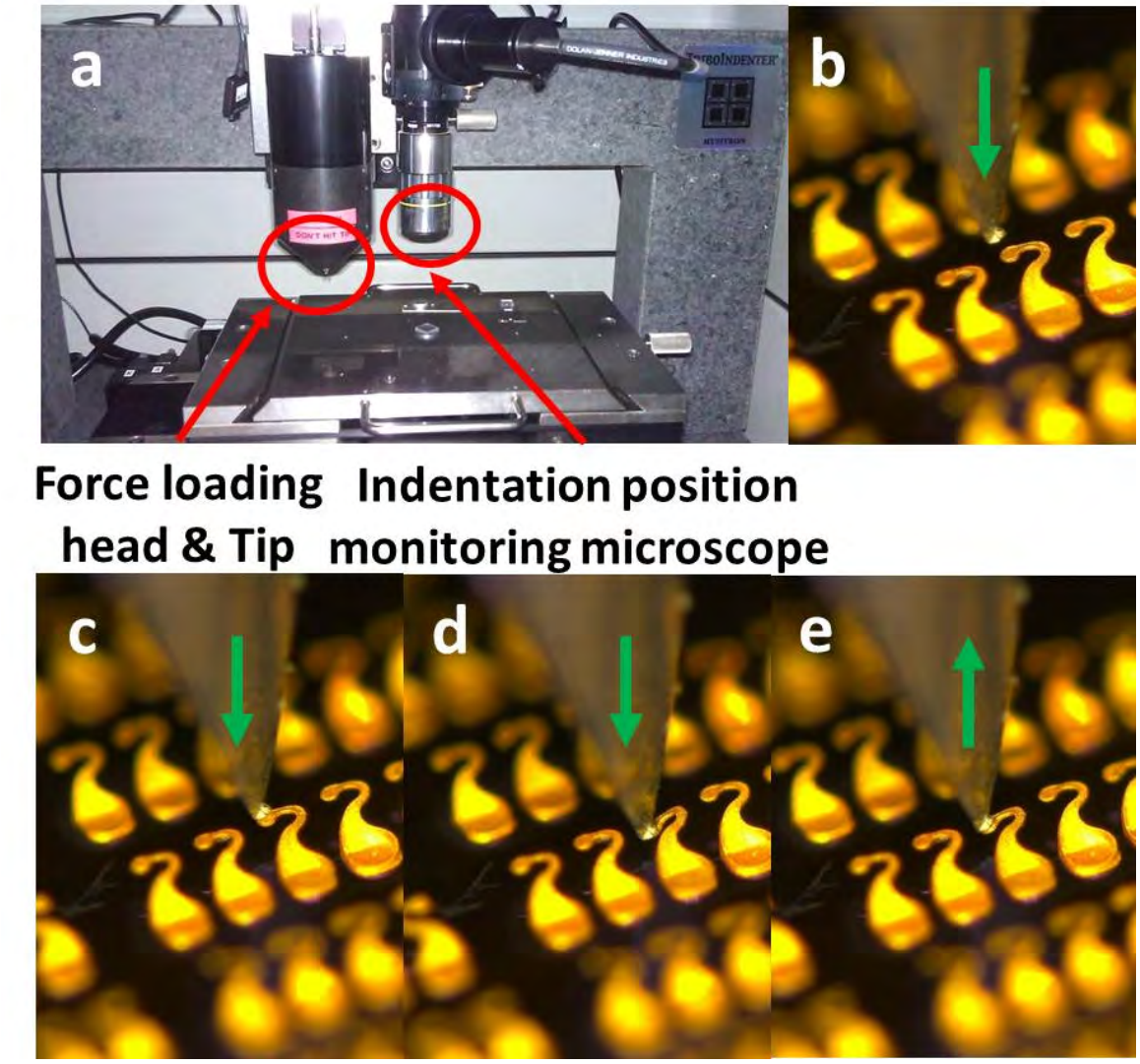
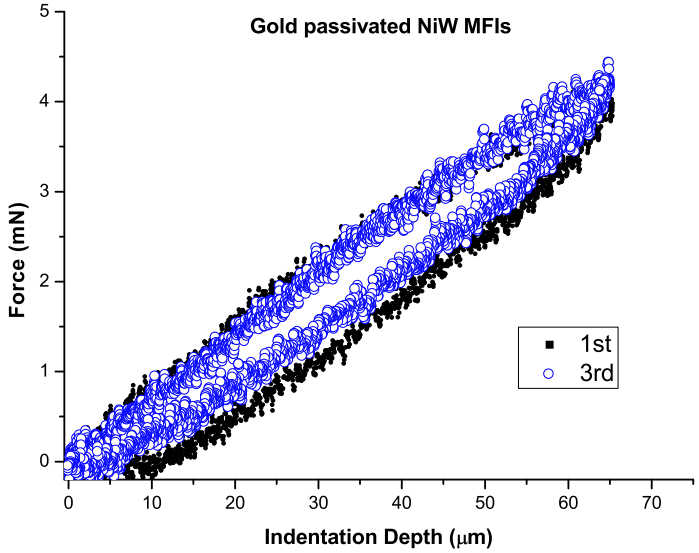


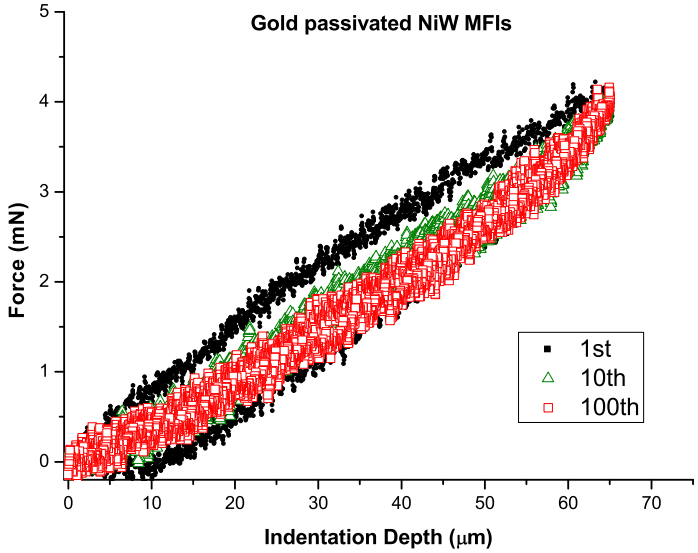
Figure 20: Indentation tests of MFIs are performed by Hysitron Triboindenter. For each indentation cycle, the free standing MFI is deformed downward to a preset depth (b, c, d) under a predefined force profile applied by a piezo-driven tip followed by a force release (e).

by a piezo-driven indentation head, which bends the MFI to a specific depth (Figure 20 b, c, d). In the backward step, the MFI is released to recover its pre-indentation profile (Figure 20 e). The real-time position and the corresponding reaction force of the piezo-driven tip, which has the same value as that of the MFI, are recorded.

The results recorded in Figure 21 verify that the 65 μm vertical deformation is elastic (the MFI thickness is 6.85 μm). Figure 21 (a) illustrates that the first few



(a)



(b)

Figure 21: Results from 100 indentations of a single gold passivated NiW MFI. The plots illustrate elastic deformation up to 65μm.

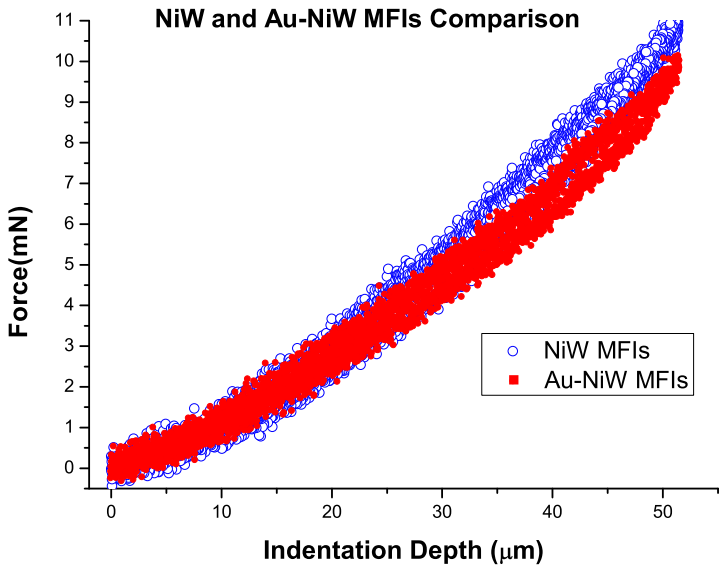


Figure 22: Comparison between NiW MFI and Au-NiW MFI shows that the gold electroless passivation layer does not degrade the elastic deformation of the NiW MFIs.

indentation cycles do not overlap with each other. This is believed to be caused by some plastic deformation that occurs in the first several indentation cycles. These might be caused by minor defects generated during the fabrication process, especially during NiW electroplating. Once these defects are recovered after the first several indentations, subsequent indentation profiles shown in Figure 21(b) are almost identical (roughly, from the 10^{th} cycle to the 100^{th}). As discussed in the previous section, in order to increase the contact force, thicker NiW MFIs should be used, which can be easily accomplished by increasing the electroplating time of NiW film.

As discussed in the previous section, since the MFI design was optimized without the gold layer, MFIs before and after gold passivation were indented to verify that the electroless gold film does not degrade the elastic deformation of the NiW MFIs. The results of 100 indentation test cycles on NiW MFIs before and after gold passivation are compared in Figure 22. The anchor thickness of the indented NiW MFI in this

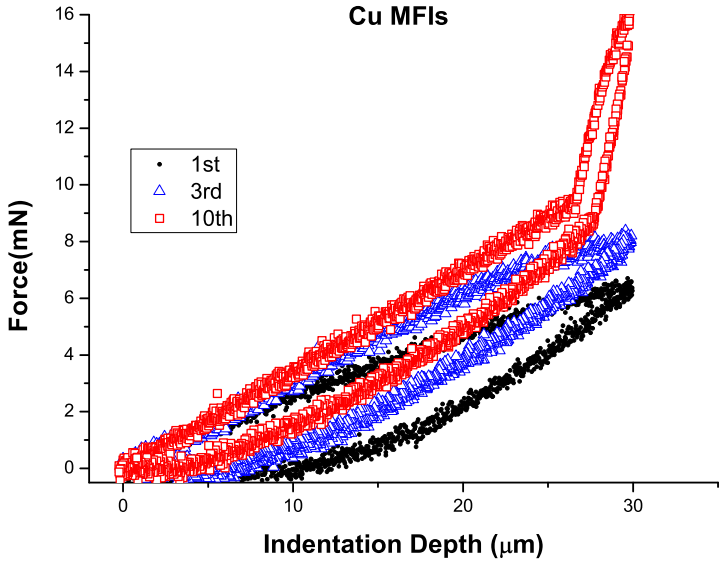


Figure 23: Cu MFI with similar thickness (11μm) cannot provide 30μm elastic deformation.

experiment is 10.12μm, and the corresponding contact force for 50 μm deformation is 10.8 mN (i.e., compliance of 4.63 mm/N). Before deposition of the gold passivation layer, the NiW MFIs were first cleaned with diluted HCl to remove the native oxide from the NiW layer. The anchor thickness of the HCl cleaned MFI is 9.43 μm and 9.73 μm before and after electroless gold plating, respectively. This indicates that 0.3 μm of electroless gold was deposited. Since both sides of the free-standing MFI are coated with gold, the total thickness of MFI is approximately 10.03μm (i.e., 0.3 μm of gold on both the top and bottom sides of the MFI). Based on the measured indentation results in Figure 22, the corresponding contact force for 50 μm deformation is 10 mN (i.e., compliance of 5 mm/N). Comparison of the two indentation results shown in Figure 22 confirms the assumption that the impact of the electroless gold passivation layer/process appears to be negligible.

In order to compare the Au-NiW MFIs with Cu-based MFIs, 100 indentation test cycles were also performed on Cu MFIs of the same design. In this case, the copper

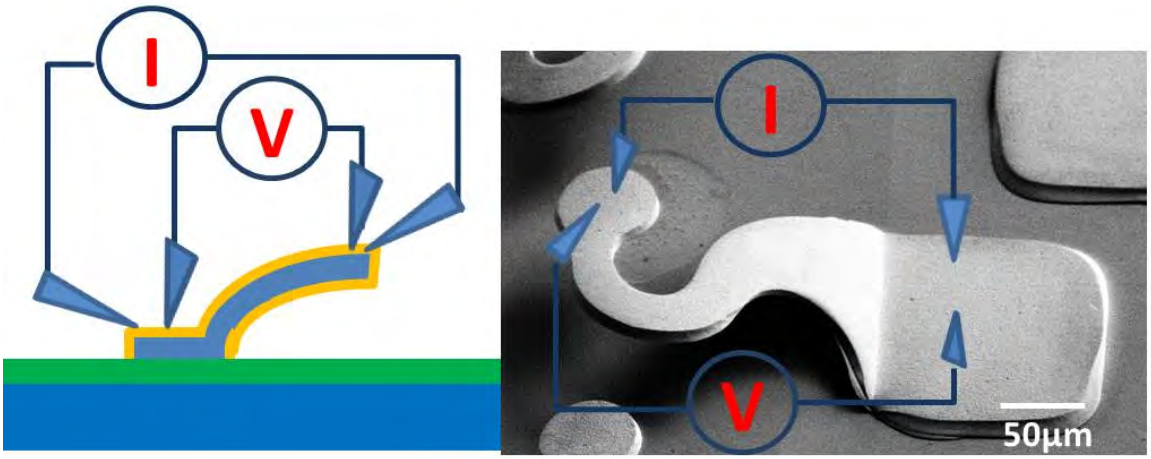


Figure 24: Four-point resistance measurement of MFIs.

MFI was 11 μm thick. However, the Cu MFIs were plastically deformed within 30 μm deformation. As shown in Figure 23, the forward and backward plots are not overlapping, and the contact force is not linear with indentation depth. In addition, there are clear indentation depth intercepts shown in the 1st and 3rd indentation plots in Figure 23, which illustrate that the MFI end position is lower than the starting position of each indentation cycle. For example, in the 1st indentation cycle, the contact force becomes zero when the indentation depth is 10 μm, which means that when the piezo-driven tip does not contact the MFI any more, the MFI is approximately 10 μm lower than the starting position. Therefore, the vertical gap of the MFI continues to shrink due to plastic deformation. At the end of the 10th indentation cycle, the tip of the MFI touches the substrate surface resulting in the contact force increasing at a much larger slope than prior experiments.

2.4.2 Electrical Characterization

Four point probing was used to perform MFI electrical resistance measurements, as shown in Figure 24. During the measurements, the tested MFIs are partially bent to attain a stable resistance reading. The average resistance of 10.25 μm thick NiW MFI

is 101.62 mΩd. This value is higher than the FEM simulated electrical resistance in ANSYS, which was 78.1 mΩ. This difference is believed to be caused by the contact resistance since the partially deformed MFI cannot provide large enough contact force to sufficiently break the thin native oxidation layer on the MFI surface.

The measured resistance of the gold passivated MFIs (0.3 μm gold layer thickness on each side of the MFI) is 67.8 mΩ. The gold passivation layer reduces the resistance due to: 1) the high conductivity gold layer is in parallel to the NiW film, and 2) provides a non-oxidized contact surface between the probe tip and the MFI. Of course, forming a thicker MFI is another approach to lowering the electrical resistance of the MFI. Given a target deformation depth, the larger contact force provided by thicker MFI is also desirable. However, as discussed in Section 3.1.1, additional design effort is needed to ensure that the maximum internal stress is lower than the yield strength of the material.

2.4.3 Enhanced lifetime

As mentioned earlier, without the passivation layer protecting NiW from oxidation, the performance of flexible interconnects degrades significantly with time. In order to verify the lifetime improvement due to the electroless gold passivation layer, 100 indentation test cycles were carried out on NiW MFIs with and without gold passivation. The indentations were performed on the same samples after two months of storage in room temperature with relative humidity of 42%. Figure 25 (a, b) illustrate that after two months, the Au-NiW MFIs maintain elastic deformation. However, the original 50 μm elastic deformation capability of NiW MFIs without a gold passivation layer cannot be maintained, as shown in Figure 25 (c,d). Obvious plastic deformation is observed from the indentation results of the NiW MFIs shown in Figure 25 (d). In addition, the intercept on the indentation depth axis of the backward plot shows that the tip of the deformed MFI does not return to the starting position of each cycle.

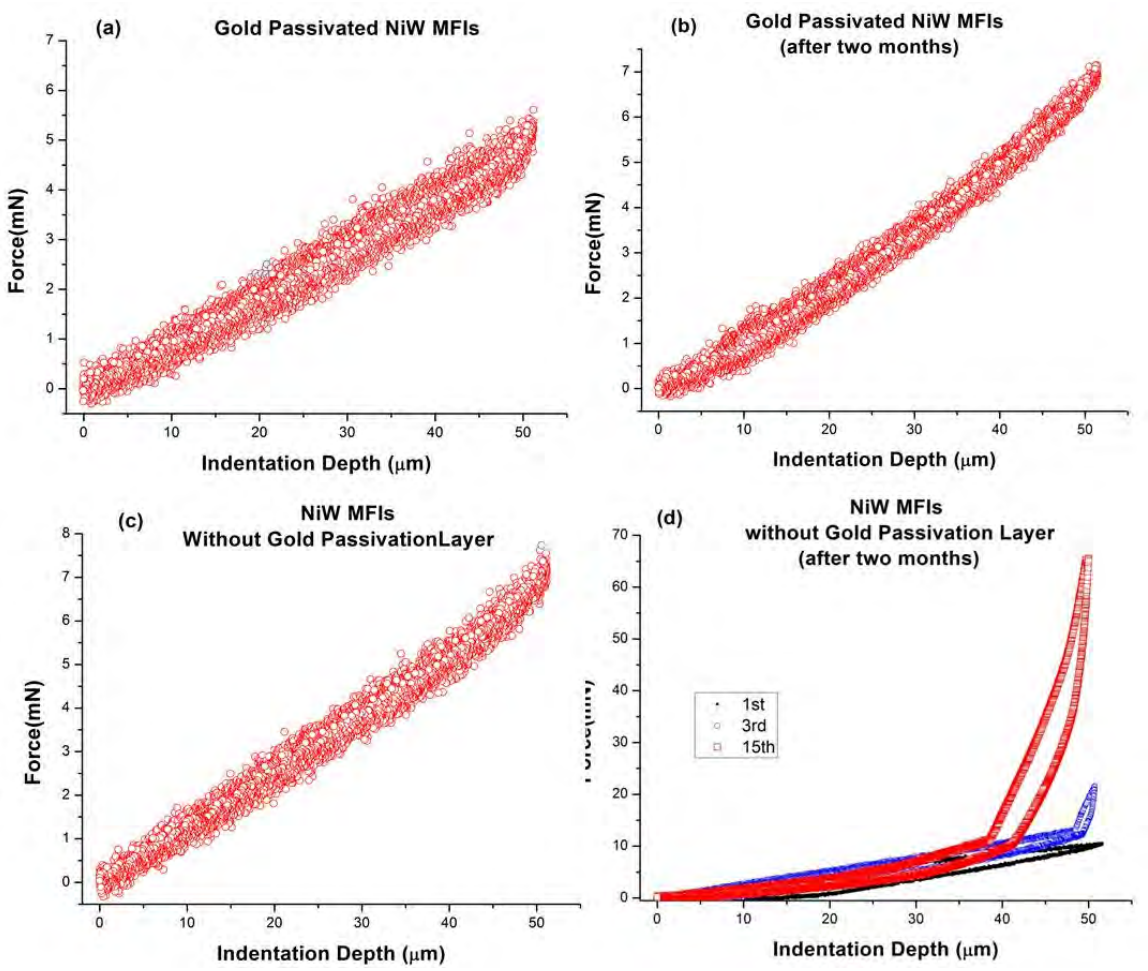


Figure 25: Life-time verification of NiW MFIs with gold passivation layer. NiW MFIs with gold passivation layer maintain the 50 μm elastic deformation capability after two months, unlike the non-passivated NiW MFIs.

The vertical gap was shrunk to less than 50 μm (from 65 μm initial gap) after the first two cycles and the tip began to touch the substrate at the end of third cycle.

Similar to the lifetime testing reported in the last section, four point probing was carried out over a two month period to compare the electrical resistance of the MFIs. As shown in Figure 26, the whole wafer was separated into three zones, and each zone was divided into two subzones (one with and one without gold passivation). Six MFIs, numbered 1-to-6 in Figure 26, were measured by four point probing method and then stored in room temperature with relative humidity of 42%. After two

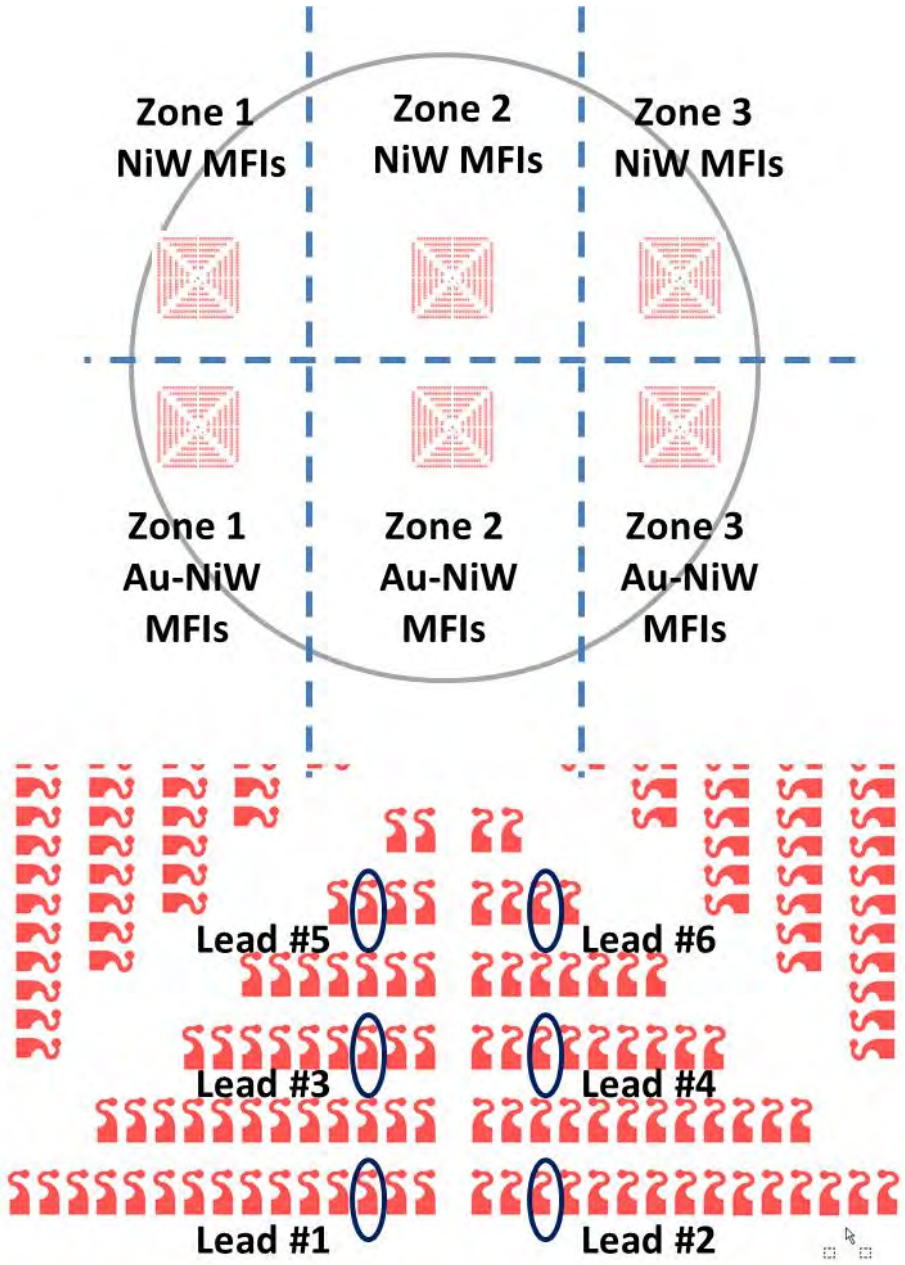


Figure 26: Electrical resistance measurement test over the whole wafer

months, another set of measurements was performed for comparison. All the electrical resistance measurements of the NiW and Au-NiW MFIs are summarized in Table 1 and Figure 27. The average resistance of 9.12 μm thick NiW MFIs increased from a range of 117.7-to-119.6 mΩ to a range of 152.3-to-163.3 mΩ. Thus, there is on average a 39.15 mΩ change in resistance. For the gold passivated MFI, the change of average

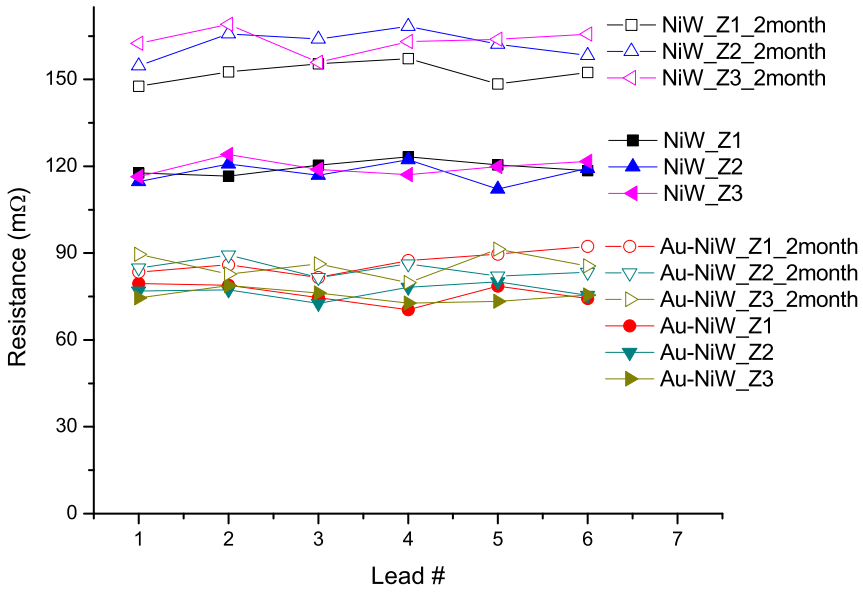


Figure 27: Electrical resistance measurements of NiW and Au-NiW MFIs. As can be seen, the gold passivated MFIs preserved their electrical resistance over a two-month period.

resistance is less than 10 mΩ.

Table 1: Electrical resistance measurements for NiW and Au-NiW MFIs

	Zone 1(mΩ)		Zone 2(mΩ)		Zone 3(mΩ)	
	NiW	Au-NiW	NiW	Au-NiW	NiW	Au-NiW
t=0	119.5	76.1	117.7	76.7	119.6	75.2
t=2 months	152.3	86.7	162.2	84.6	163.3	85.8

2.5 Conclusion

Wafer-level batch fabricated gold passivated NiW MFIs are experimentally demonstrated with 65 μm vertical elastic range-of-motion. The electroplated NiW material with very high yield strength makes it promising to realize rematable MFI. The enhanced geometrical design of the MFIs ensures stress is distributed uniformly during

deformation, and at the same time, maintains an inner stress that is lower than the yield strength of NiW during vertical deformation. High yield strength material along with the optimized geometry design ensure the NiW MFI has 50 μm+ vertical range-of-motion while providing a large contact force. In addition, the electroless gold passivation layer not only lowers the resistance but was also critical to protecting the MFIs from oxidation to preserve their mechanical and electrical characteristics, which was experimentally verified by the results of 100 indentations and four-point electrical resistance measurements, respectively, performed over a period of two months.

CHAPTER 3

MFIs WITH HIGHLY SCALABLE PITCH

3.1 Introduction

The pitch of the Au-NiW MFIs discussed in Chapter 1 is larger than 150 μm, which is only suitable for the interconnection between silicon interposer and organic substrate. However, for the fine pitch flexible I/Os, for example the I/Os used to connect interposer and bridge, as shown in Figure 9, further footprint scaling of MFI while keeping a large vertical gap needs to be addressed. The critical fabrication step to enable such scaling is how to form a fine pitch electroplating pattern on a substrate with large surface variation. The photoresist spin-coating approach adopted in Chapter 1 is not feasible here due to fabrication challenges such as exposure dose optimization and dome cracking during photoresist pre-bake. Spray-coating approach has been widely used for the photoresist formation on a substrate with large surface variation [59]–[62]. In this chapter, a photoresist spray-coating based fabrication process for MFIs is developed to address the footprint scaling issue and enables a large MFI array with highly scalable pitch.

This chapter is organized as following, 1) finite element method (FEM) analysis is conducted to investigate the electrical and mechanical properties of MFIs with various pitch and size in Section 3.2; 2) the wafer-level batch fabrication process of MFIs with wide range of dimensions and pitch is discussed in Section 3.3; 3) Finally in Section 3.4, mechanical and electrical test results of the MFIs with highly scalable pitch are reported.

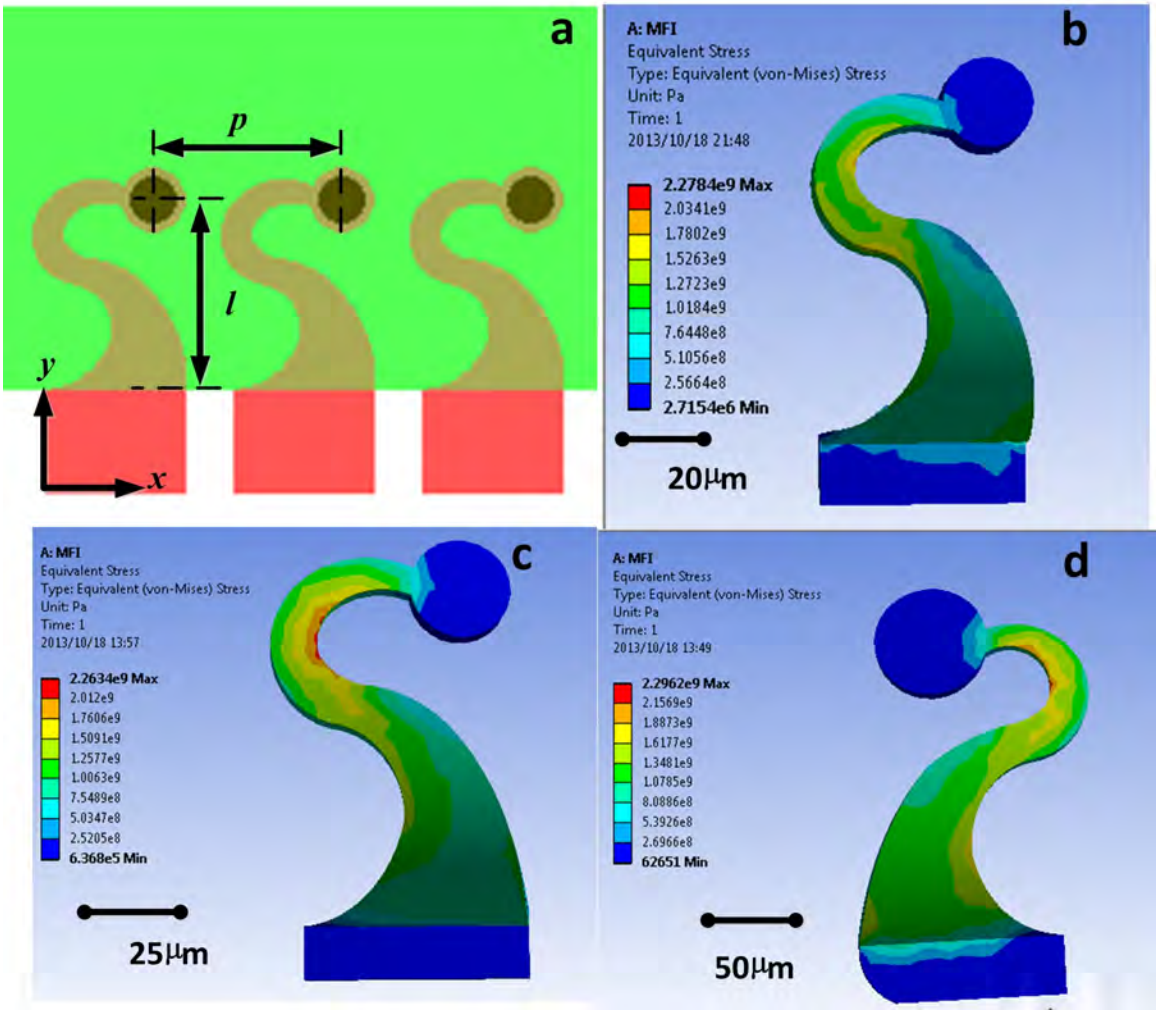


Figure 28: Pitch definition (a) and von Mises stress simulations of NiW MFIs on 50 μm pitch (b), 75 μm pitch (c), 150 μm pitch (d).

3.2 FEM Analysis on MFIs with Highly Scalable Pitch

In this section, we report FEM analysis of the mechanical compliance and electrical resistance of MFIs with various geometries. As shown in Figure 28 (a), the pitch, p, of an MFI array is the distance between two nearby MFI tips; the length, l, of MFIs is the projected distance between the tip and anchor of the MFI. When the pitch and the length of an MFI are specified, the tapered shape of the MFI is optimized based on the design rules reported previously [53], [54]. Since both the vertical gap and the thickness of the MFI are uniform, they are considered as constant in the analysis reported in this section. The NiW MFI is assumed to be stress-free before deformation because the internal stress induced in the NiW electroplating process [56] is negligible compared to the stress caused by the external bending force. Moreover, the internal stress-free assumption is verified by the fact that the simulated and experimental compliance match as reported in Section 3.4.

Table 2: FEM simulation results of MFIs with various pitches

	Pitch		
	50 μm	75 μm	150 μm
Length (μm)	50	75	150
Vertical gap (μm)	65	65	65
Thickness (μm)	7.2	7.2	7.2
Compliance (mm/N)	1.26	2.93	5.57
Resistance (mΩ)	110.63	125.72	122.48

The mechanical properties of NiW MFIs with various sizes are simulated using ANSYS Workbench 13.0. NiW MFIs designs on 50 μm, 75 μm, and 150 μm pitches are shown in Figure 28 (b), (c), and (d). The MFI thickness and vertical gap are selected as 7.2 μm and 65 μm, respectively. As shown in Figure 28, the inner stress of MFI is uniformly distributed to decrease the maximum inner stress that helps alleviate the mechanical fatigue. The compliance of each simulated MFI is summarized in

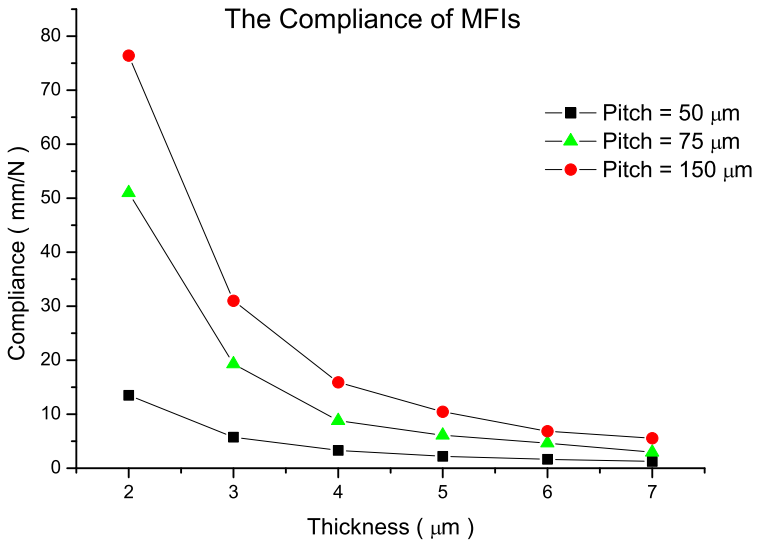


Figure 29: FEM simulation results indicate the compliance of MFIs on 50 μm, 75 μm, and 150 μm pitches increases as the thickness decrease.

Table 1. The thickness, 7.2 μm, is selected here to optimize the compliance of MFIs on 150 μm pitch. Of course, the thickness of an MFI should be based on a specific MFI geometrical design, which again, in this case was performed for the MFI design with 150 μm pitch. As such, the compliance of the MFIs on 50 μm pitch is lower than that on 150 μm pitch. To increase the compliance of the MFIs on 50 μm pitch, the thickness of the MFIs can be reduced, as shown in 29. To maintain the tapered design of MFIs, in this work, the size of the MFIs is scaled down in both the x and y directions with the same scaling factor, as shown in Figure 28 (a). Therefore under such scaling, at a given thickness, the resistance, R, of the MFIs on different pitches does not vary appreciably as demonstrated by the FEM simulation results summarized in Table 2.

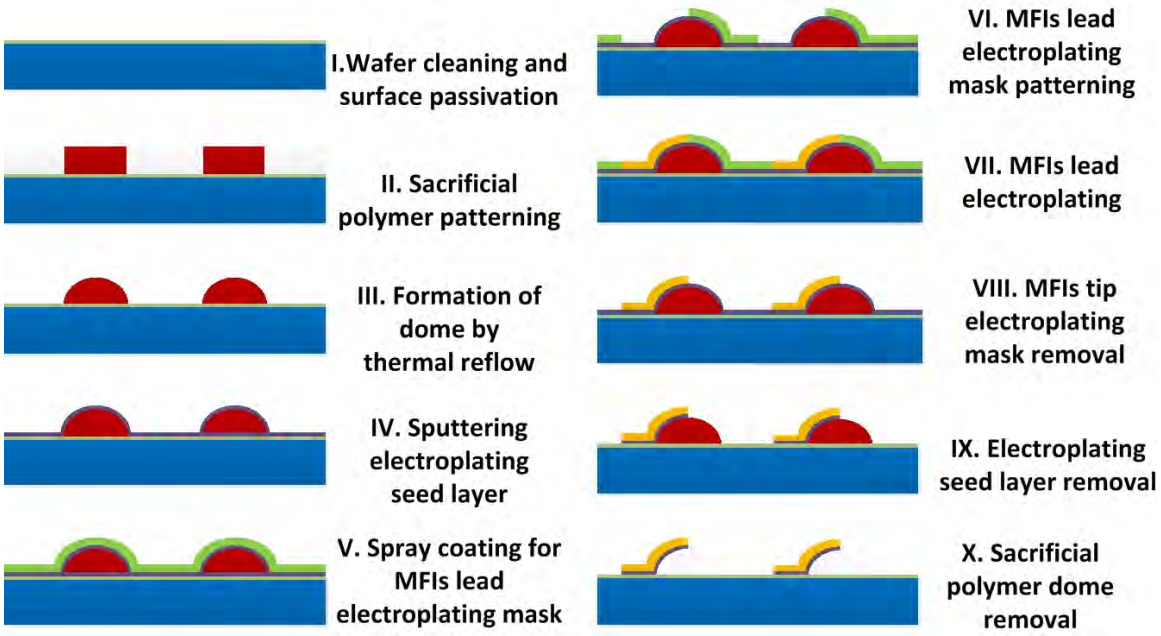


Figure 30: Fabrication process of the MFIs with highly scalable pitch.

3.3 Fabrication of MFIs with Highly Scalable Pitch

The fabrication process of MFIs under consideration is illustrated in Figure 30. Conventionally, a spin-coating approach is adopted in the fabrication of flexible I/Os with either small pitch (down to 100 μm) or large vertical gap (up to 40 μm), such as the work reported in [35], [41], [42], [45], [51], [52]. However, due to two main issues, difficulty to achieve proper exposure of the photoresist and non-uniform evaporation of the solvent (details will be discussed later in this section), spin-coating is not feasible to realize flexible I/Os with both fine pitch and larger vertical gap. In this paper, we utilize conformal photoresist spray-coating for the first time, which is the key enabler to scaling MFI pitch to 50 μm, while maintaining a 65 μm high vertical gap. The fabrication process of the MFIs begins with a sacrificial polymer spin-coating on a silicon wafer with a nitride passivation layer. This process step is followed by a thermal reflow process to form 65 μm tall sacrificial polymer domes. Next, a Ti/Cu/Ti film is sputter coated on top of the polymer domes as an electroplating seed layer. Above the

seed layer, instead of photoresist spin-coating, photoresist spray-coating is adopted to realize a 10 μm thick conformal negative photoresist layer (over the 65 μm high domes). This conformal photoresist layer is patterned and used as the NiW electroplating mold for the MFIs. After electroplating of the MFIs, the photoresist plating mold, the seed layer and the polymer dome are removed leaving behind fine-pitch MFIs with a vertical gap of 65 μm above the substrate. Details of the spray-coating process and its advantages over the spin-coating for the MFI fabrication process are described next.

3.3.1 Spray-coating vs. Spin-coating

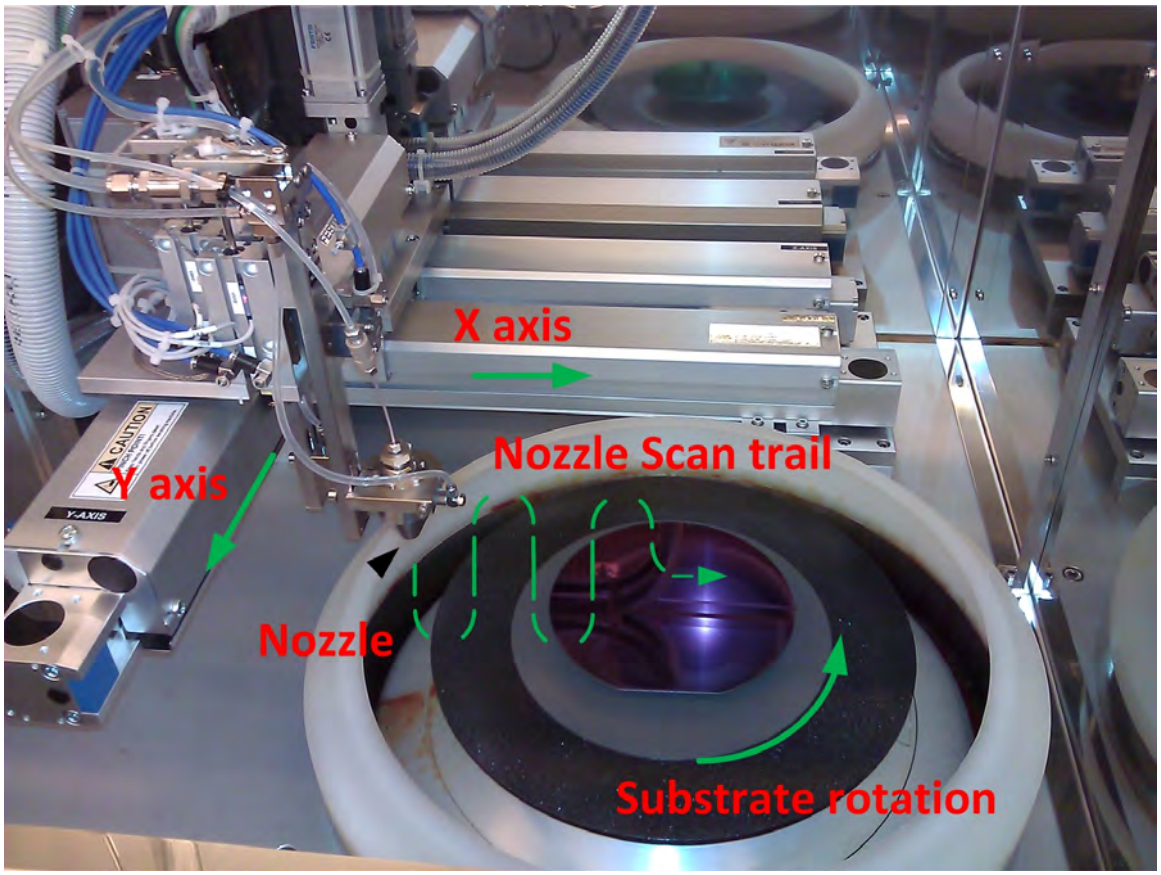
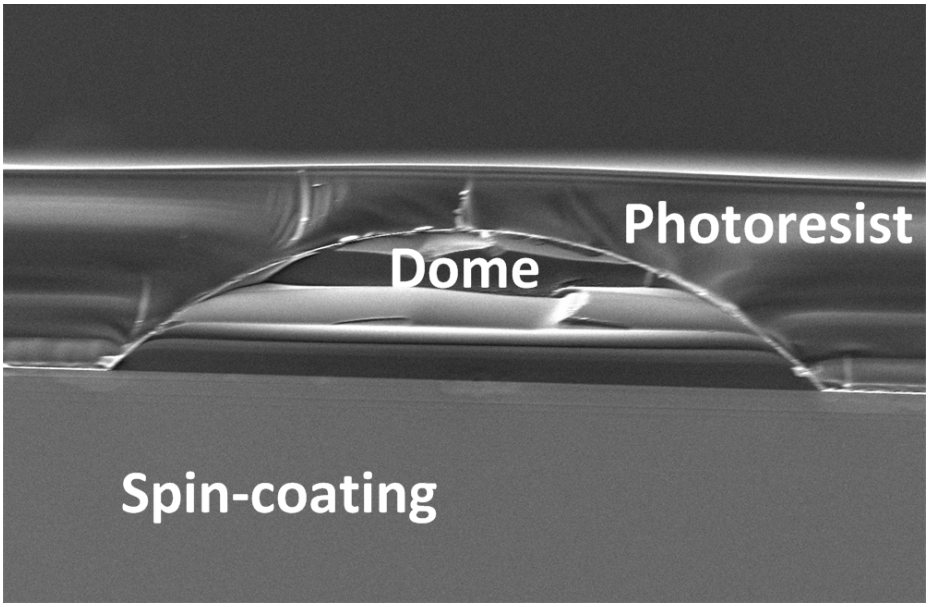


Figure 31: Uniform and conformal photoresist film can be obtained by Suss Alta spray-coating System.

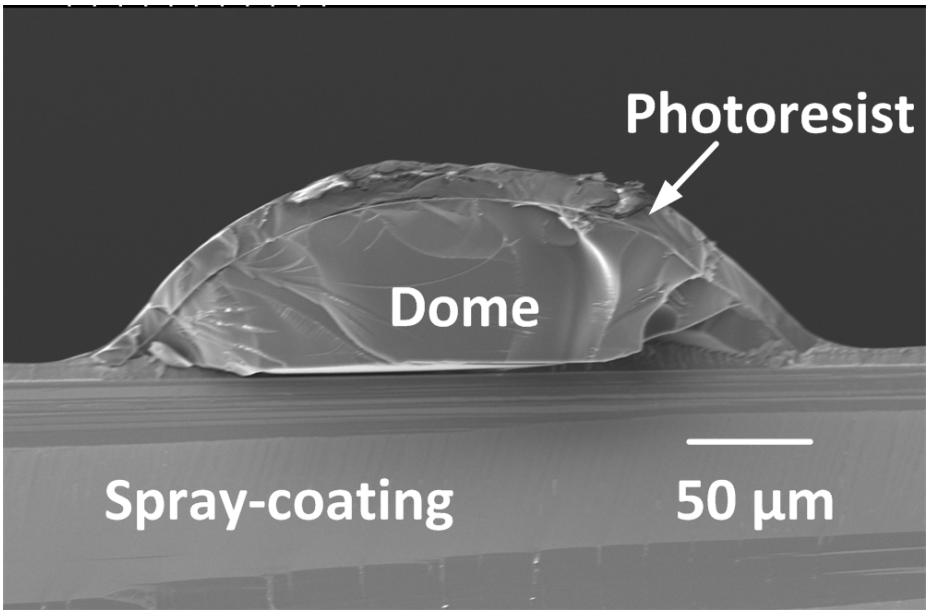
Spray-coating is performed using a Suss Alta Spray Coater, as shown in Figure 31

to yield a uniform and conformal photoresist film above the polymer domes. During the spray-coating process, the diluted photoresist is pumped to a spray nozzle and subsequently pulverized into tiny droplets. These tiny droplets in turn are sprayed out of the nozzle and onto the wafer surface. During the flight from the nozzle to the wafer, most of the solvent in the droplets is evaporated and only the polymer clusters are deposited on the wafer surface to form a conformal film. The spray coater nozzle is scanned in the X- and Y-axes while the wafer is continuously rotated to ensure uniform deposition. The thickness of the deposited film depends on the nozzle scanning speed, the pumping rate, and the photoresist concentration. For example, about 10 μm thick photoresist can be obtained by spray-coating diluted negative photoresist with a nozzle speed of 350 mm/s and a pump flow rate of 0.8 ml/min.

In order to highlight the key benefits of the spray coated photoresist layer, a cross-section of the sacrificial polymer domes (covered by an electroplating seed layer) coated with a spin-coated and a spray-coated photoresist layers are shown in Figure 32. The spin-coated photoresist layer produces a planar surface profile resulting in a non-uniform photoresist layer. Since the photoresist thickness in the spin-coating scenario is non-uniform, two main challenges are introduced that make photoresist spin-coating not applicable for fine-pitch MFIs fabrication: 1) exposure dose control and 2) non-uniform solvent evaporation. However, the surface profile of the spray-coated photoresist layer perfectly follows the wafer surface topology leading to a uniform photoresist layer. In addition, since most of solvent evaporates during the spray-coating process, low temperature soft bake is sufficient for the subsequent photolithography step. Therefore, the two spin-coating induced issues can be perfectly resolved. The challenges induced by spin-coating approach and how they are resolved by the spray-coating approach are discussed next.



(a)



(b)

Figure 32: Compared to spin-coating (a), photoresist spray-coating (b) can form a uniform photoresist layer on top of sacrificial domes.

3.3.2 Fabricaton Challenges Using Spin-coating

As shown in Figure 32, after spin-coating, the photoresist layer on top of the polymer domes is thin while the region in the valley between two domes is thick. The large

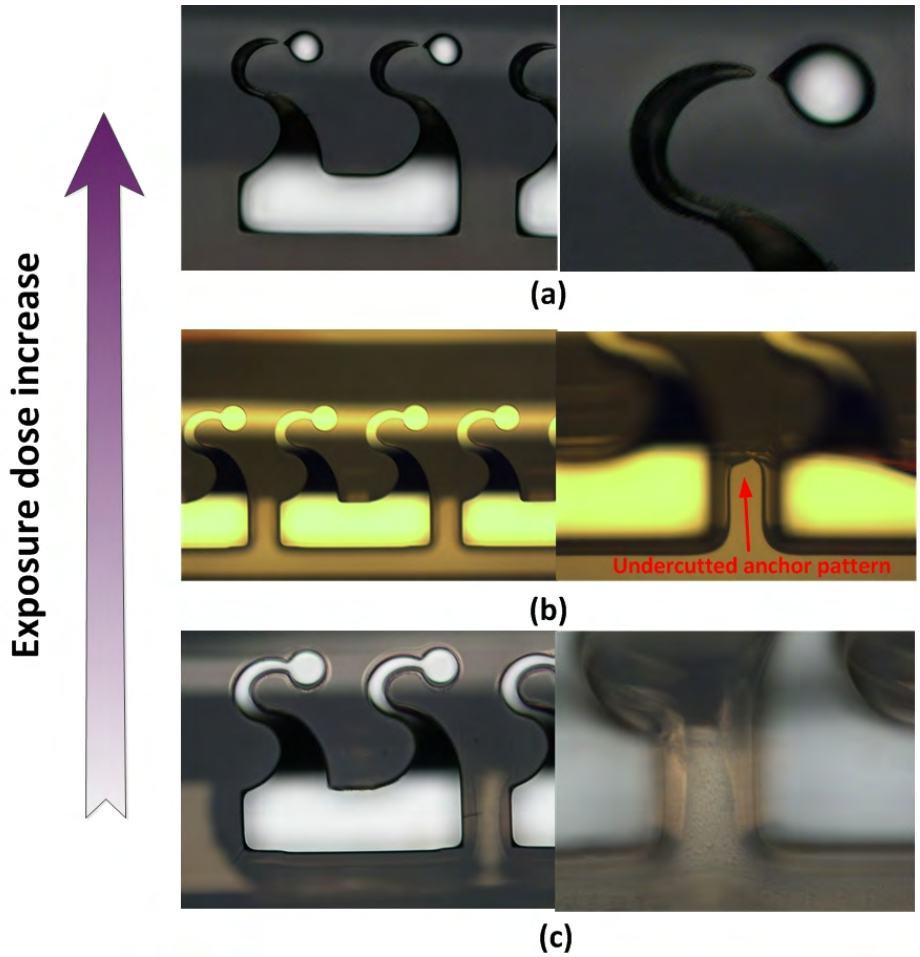


Figure 33: An over exposure of photoresist results in the loss of fine pattern on top of the dome (a); the photoresist undercut cannot be eliminated by a fine-tuned exposure (b); under exposure results in severe undercut on valley (c).

photoresist thickness difference makes it difficult to achieve proper exposure of the photoresist on both the top of the domes and in the valley between the domes. Either over exposure on top (resulting in loss of fine patterns) or under exposure in the valley (resulting in severe undercut of MFIs anchor) will render the MFI fabrication as null, as shown in Figure 33. The other main issue, as shown in Figure 34(a), is the non-uniform evaporation of the solvent in photoresist. During the soft bake step, most of the solvent evaporates from the photoresist, which leads to volume shrinkage of the photoresist layer. Due to the thickness variation, the evaporation and the volume shrink are non-uniform, which leads to an inner stress variation around the dome.

In addition, the partially melted polymer dome during the high temperature soft bake process step makes the dome prone to distortion. Consequently, the seed layer covering the polymer dome can be broken, which leads to photoresist leakage at the dome edge (Figure 34 (b)) and seed layer cracking on the top of the dome (Figure 34 (c)). The photoresist leakage will prevent the subsequent electroplating process and yield broken MFIs, as shown in Figure 34 (d). Moreover, the photoresist plating mold cracking can also be induced by the non-uniform evaporation, as shown in Figure 34 (e).

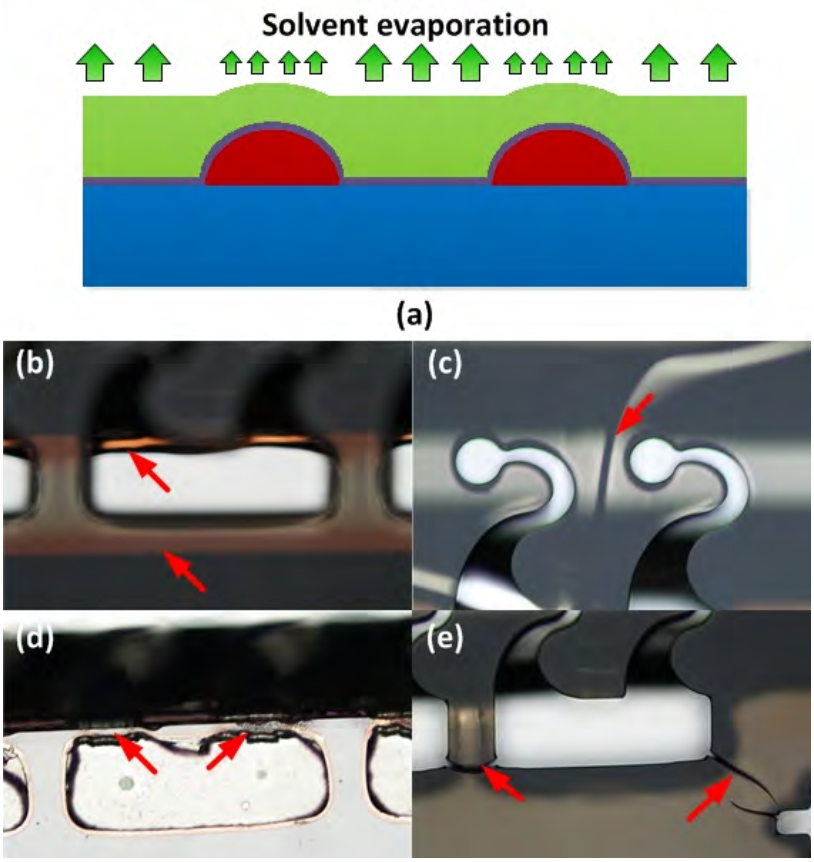


Figure 34: Fabrication issues caused by non-uniform solvent evaporation (a) are: (b) polymer dome leakage, (c) seed layer cracking, (d) MFIs breaking, and (e) electroplating mask cracking.

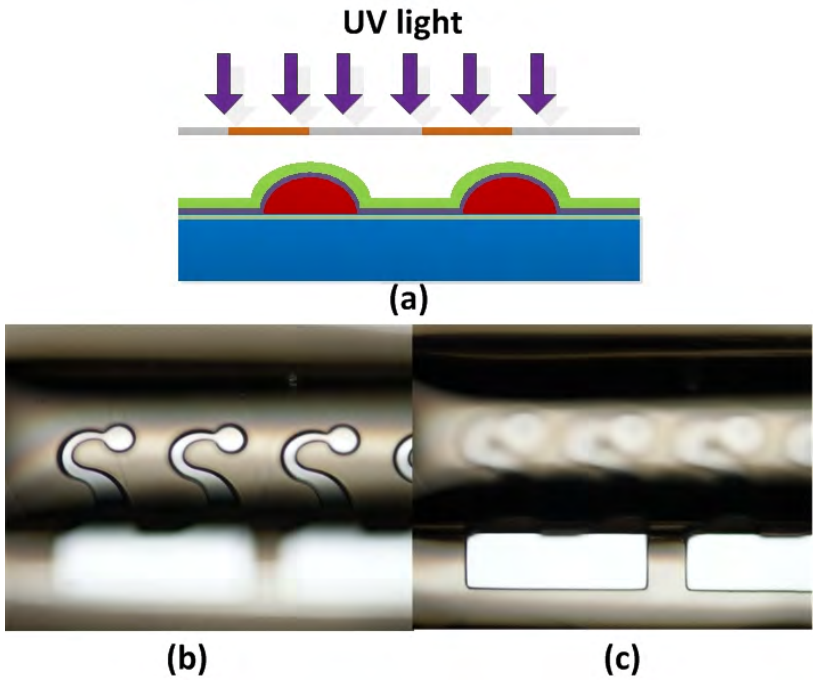


Figure 35: A proper exposure can be conducted on the conformal spray coated photoresist layer (a). After the development, clear pattern can be obtained both on the top of the domes (b) and in the valley between the domes (c).

3.3.3 Fabrication Using Spray-coating

Using spray-coating, a uniform and conformal photoresist film can be formed across the wafer and thus eliminating the two challenges introduced by spin-coating. As shown in Figure 35, patterns on top and in the valley of the domes are fully developed with good critical dimension control. Since there is no undercut or breakage in the electroplating mask, shorting is prevented between nearby MFIs after electroplating. Compared with the spin-coated sample, the MFIs fabricated using spray-coating avoid the high temperature soft baking therefore the non-uniform solvent evaporation issue and produces MFIs with high yield, as shown in Figure 36.

After the removal of the plating mold, seed layer, and sacrificial domes, Figure 37 (a) illustrates the remaining free standing MFI array with various pitches (150 μm, 75 μm and 50 μm). High magnification images of MFIs with various pitches are

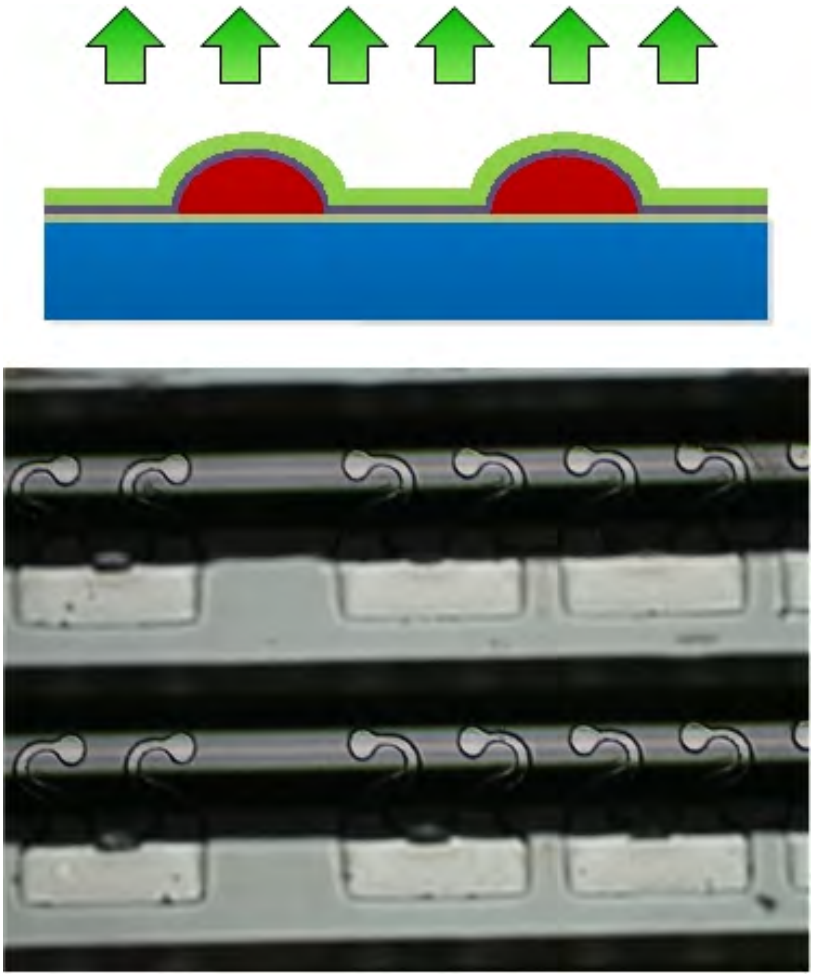
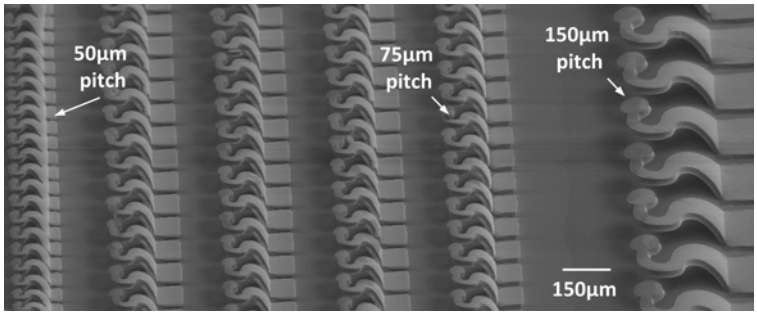


Figure 36: The solvent evaporation of a spray coated sample is uniform and no high temperature soft baking process needed which yields MFIs consistent to design geometry on the dome surface with no cracks.

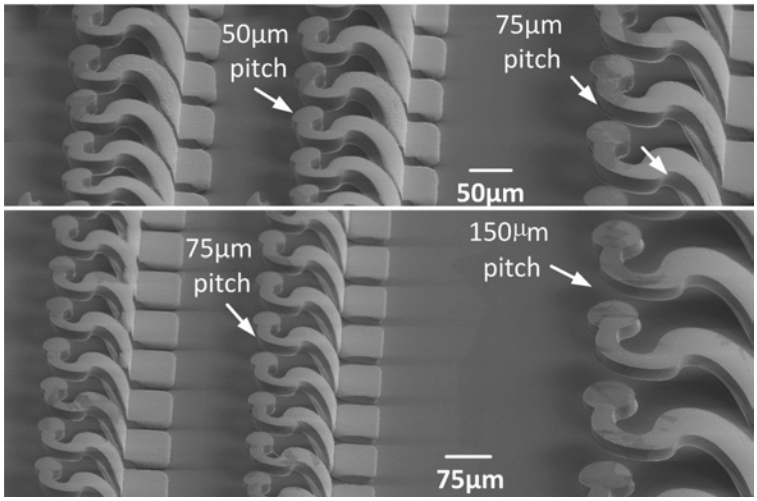
illustrated in Figure 37 (b). The 65 μm vertical gap of the MFI is verified by the side view, as shown in Figure 37 (c). All MFIs have the same vertical gap (65 μm) and thickness (7.2 μm).

3.4 Mechanical and Electical Characterization

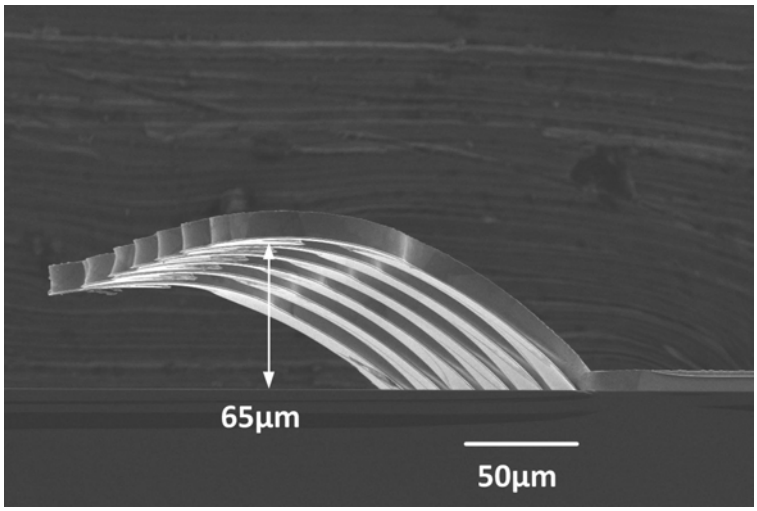
Indentation testing and four-point resistance testing of the MFIs were carried out in similar approach as described in Section 3.1.3.1, and the results are summarized in Table 3. For four-point resistance testing, seven MFIs were randomly picked from each of three designs with different pitches.The resistance is slightly larger than the



(a)



(b)



(c)

Figure 37: Overall view (a,b) and side view (c) of free standing MFIs array on 150 μm, 75 μm and 50 μm pitch with 65 μm vertical gap.

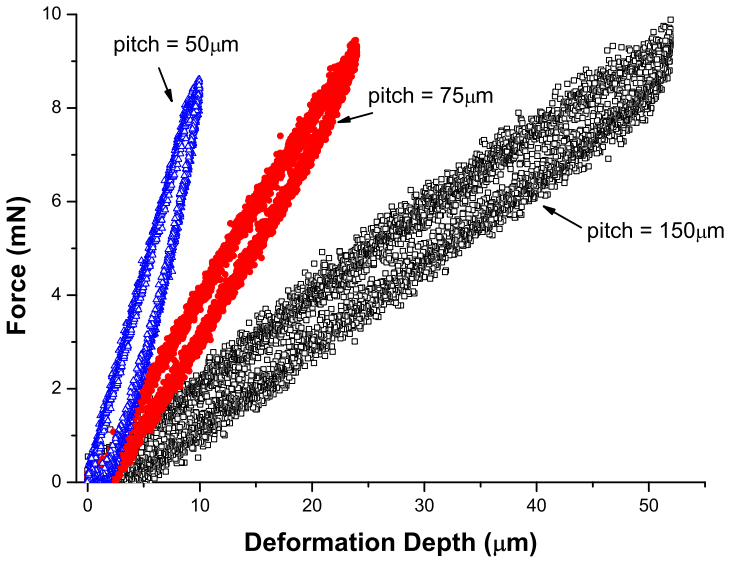


Figure 38: Indentation results of MFIs with pitches of 150 μm, 75 μm, and 50 μm.

Table 3: Comparison between FEM simulation and experimental data for MFIs with various pitches

			Pitch		
			50 μm	75 μm	150 μm
Compliance (mm/N)	FEM Simulation		1.26	2.93	5.57
	Indentation measurement		1.2	2.72	5.32
Resistance (mΩ)	FEM Simulation		110.63	125.72	122.48
	Four point measurement	Average	119.1	134.3	133.2
		Standard deviation	3.87	4.02	3.79

results from FEM simulations, which is believed to be due to the fact the resistivity of the electroplated metal film is higher than that of bulk material, which is used in the simulation. In addition, indentation testing details of each MFI design with various pitches are plotted in Figure 38. These results are consistent with our FEM simulations in Section 3.1.4.1. Again, to increase the compliance of the MFIs on the smaller pitch, a thinner metal film should be electroplated, as shown in Figure 29.

3.5 Conclusion

Mechanically flexible interconnects (MFIs) with highly scalable pitch (from 150 μm to 50 μm) and large vertical gap (65 μm) are reported in this chapter. The wafer-level batch fabrication of the reported MFIs is enabled by performing photolithography on a highly non-uniform surface (65 μm high sacrificial domes) covered with a spray-coated photoresist. Compared with the spin-coating assisted process, the benefits of spray-coating assisted process are demonstrated in two ways: 1) Exposure dose can be easily optimized based on the uniform thickness of the photoresist layer ; and 2) The non-uniform solvent evaporation and dome cracking are avoided by circumventing the high temperature photoresist soft baking. The indentation and resistance tests are used to verify the mechanical and electrical properties of MFIs, which match the simulation results using ANSYS. As MFI footprint scales, the optimization of MFI dimensions, especially the thickness, is essential to obtain a trade-off between electrical and mechanical performance of MFI.

CHAPTER 4

MFIs WITH CONTACT-TIP FOR REMATABLE INTEGRATION

4.1 Introduction

Several flexible interconnects with tips were previously reported [42], [51], [63], [64]. The two main objectives of adding tips on previously reported flexible interconnects are: 1) form a better alignment and holding position for solder ball [51], [63] or 2) compensate the anchor height of flexible interconnects [42], [64]. In this chapter, the Au-NiW based MFIs have been advanced by adding a contact tip with truncated-cone shape as well. However, since the Au-NiW is designed for temporary interconnection and has no anchor height to compensate, the tip on MFI is used to enhance scrubbing on the bonding pads and form a reliable temporary contact.

The fabrication and experimental design of the MFI technology under consideration are first discussed in Section 4.2. Moreover, rematable chip assembly using MFIs is demonstrated and characterized in Section 4.3. Finally, robust assembly of a silicon chip on a non-planar surface using MFIs is reported in Section 4.4.

4.2 Experimental Design and Fabrication Process

4.2.1 Fabrication of MFIs with Contact-Tip

Based on our previously reported Au-NiW MFIs [65], the fabrication process of Au-NiW MFIs with a contact tip has been developed and is shown in Figure 39. The fabrication process of the MFIs begins with the formation of a sacrificial polymer dome accomplished by patterning and thermally reflowing a spin-coated polymer layer on a nitride passivated silicon wafer. Next, a Ti/Cu/Ti film was sputtered on

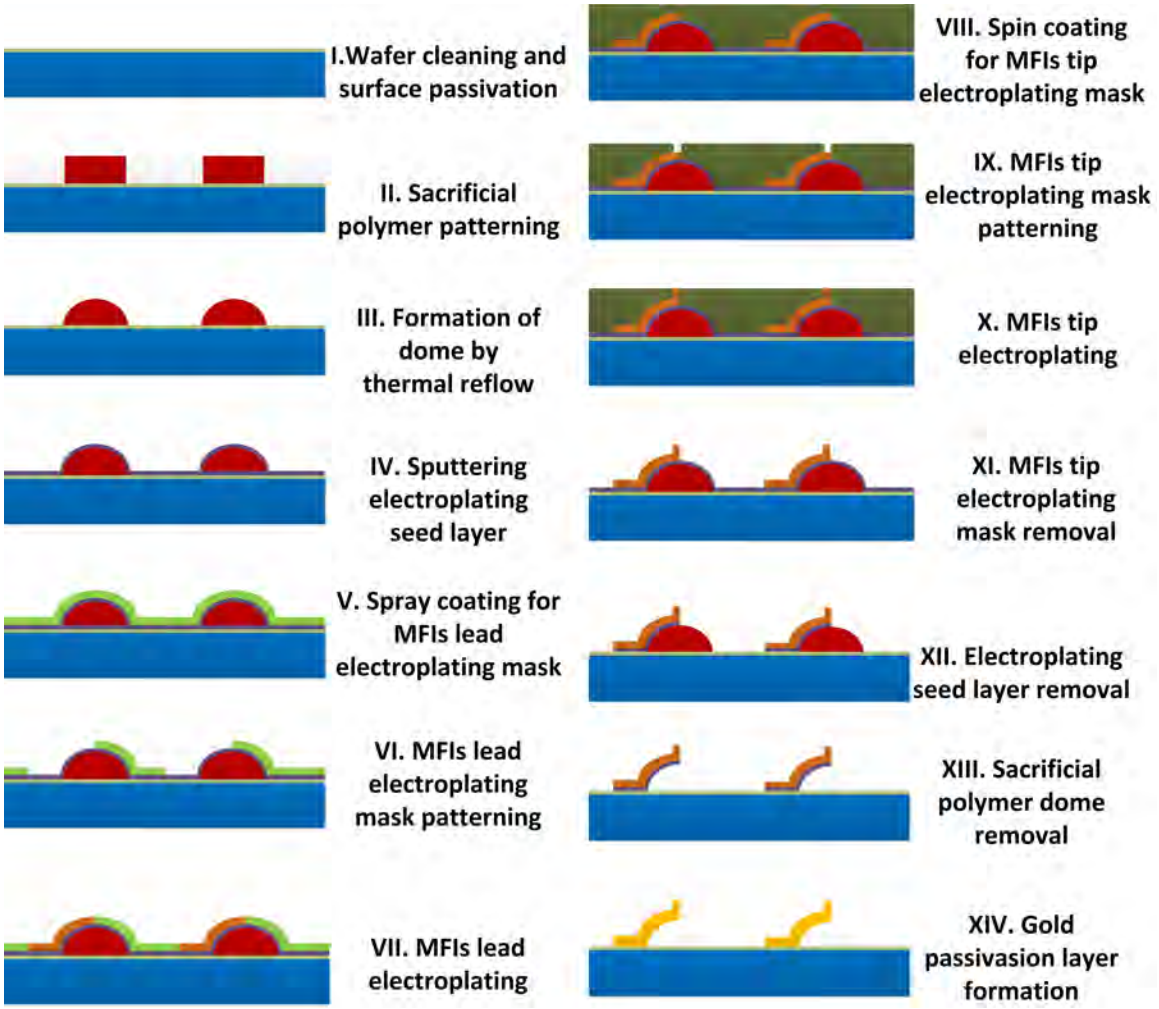


Figure 39: Fabrication process of the Au-NiW MFIs with contact tip.

top of the 65 μm tall polymer domes as an electroplating seed layer. Following seed layer formation, a 12 μm thick conformal photoresist layer was spray coated and patterned on top of the seed layer as an electroplating mold [66]. After electroplating of the MFIs, the photoresist plating mold was removed and followed by patterning of another spin-coated photoresist for the tip electroplating. Following tip formation, the tip electroplating mold, the seed layer and the polymer dome were stripped leaving behind MFIs with a truncated-cone tip and a 65 μm high vertical gap above the substrate. Finally, the free-standing NiW MFIs on the test chip are passivated by a 0.3 μm thick electroless gold finish.

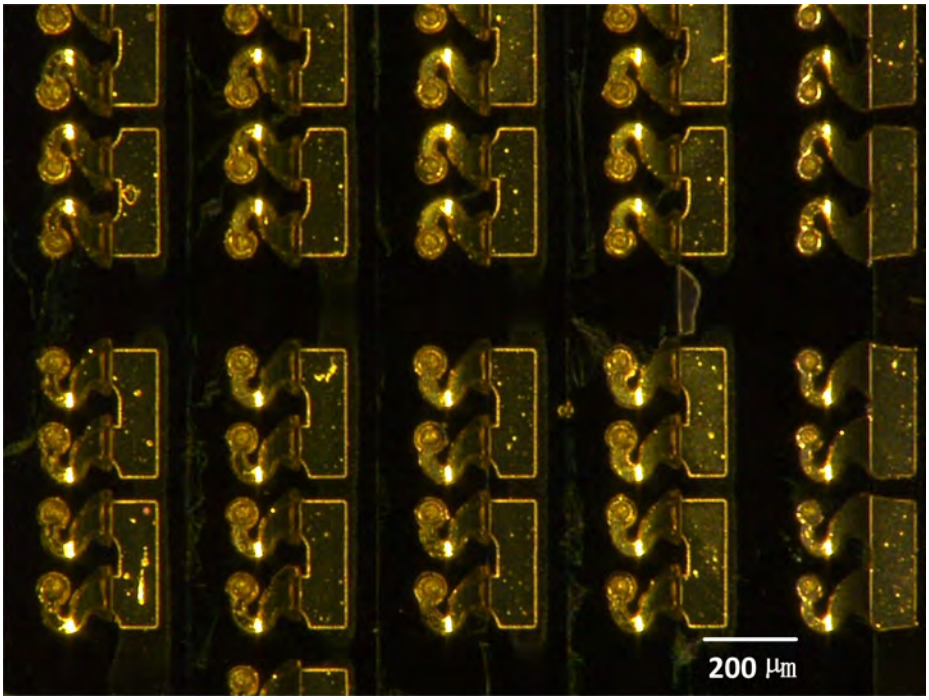


Figure 40: MFIs with contact tip after being passivated with and electroless gold layer.

An array of Au-NiW MFIs with truncated-cone tip is shown in Figure 40. As reported in [65], compared with the sputtering method, electroless gold plating does not take any extra lithography steps and covers the entire surface area of the free-standing MFIs. The very thin (about 0.3 μm) Au passivation layer lowers the resistance and enhances the life-time of the NiW MFIs while maintaining the excellent mechanical properties [65]. In addition, during the assembly process, the Au-NiW MFIs form a low-contact resistance, in particular, to gold passivated bonding pads.

SEM images of Au-NiW MFIs with truncated-cone tip are shown in Figure 41 (a)-(d). The inline pitch of the fabricated MFIs is 150 μm and exhibit a standoff height of 65 μm. The thickness of the MFIs is 10 μm; the tip formed above each MFI adds another 30 μm of height. Therefore, the aggregate height of each MFI with tip is up to 105 μm, which is large enough to overcome the surface variation and the warpage of organic substrates. The contact tip was designed and fabricated as a

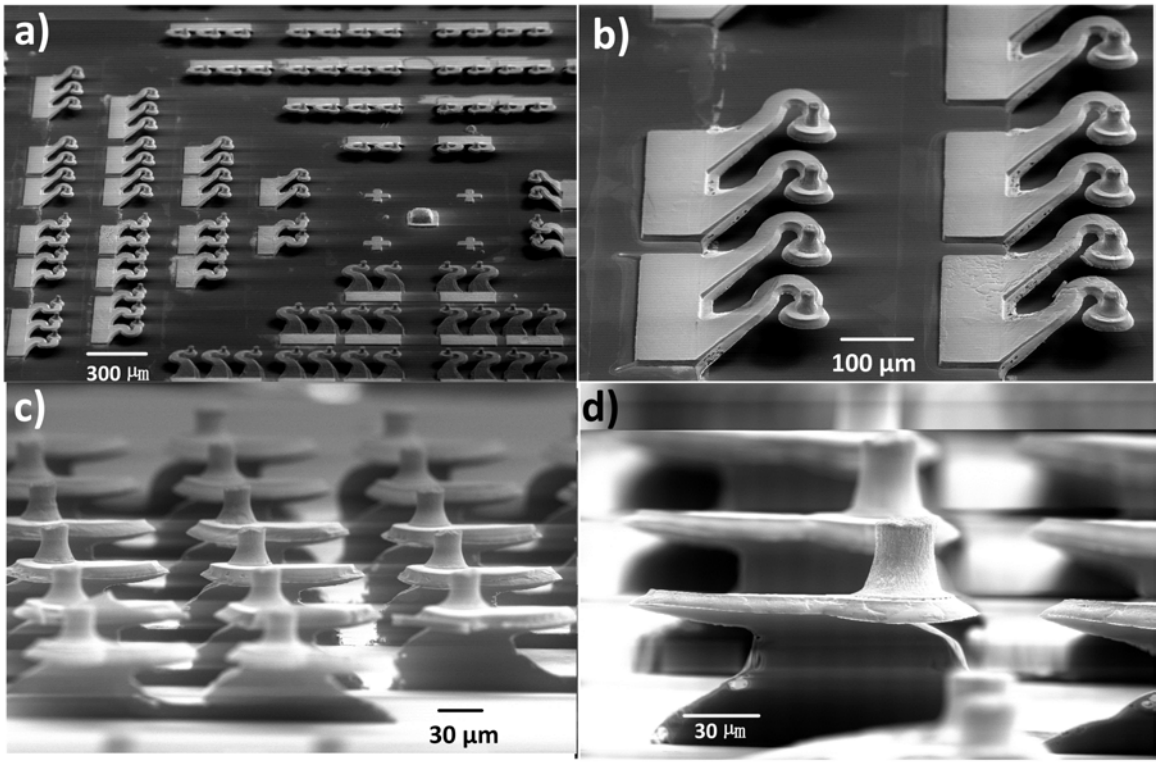


Figure 41: Free standing Au-NiW MFIs with truncated-cone tip. The Au-NiW MFIs exhibit a 65 μm elastic vertical range of motion and a 30 μm tall truncated-cone tip.

truncated-cone shape for the following reasons: 1) the base of the tip is enlarged for better tip-to-lead adhesion and lower resistance, and 2) the contact tip can enhance the scrubbing capability over bonding pads. The truncated-cone profile was formed by an electroplating process using a photoresist mold with a negative sidewall profile.

4.2.2 Experimetal Design

Two types of assembly experiments were conducted to characterize the electrical and mechanical properties of the MFIs: 1) Assembly of a chip with MFIs onto a substrate with uniform height pads multiple times to demonstrate the rematable assembly (Figure 42 (a)); and 2) assembly of a chip with MFIs on a substrate with non-uniform height pads to demonstrate robust assembly and the ability of the MFIs to compensate for non-planar surfaces (Figure 42 (b)). In both experiments, the

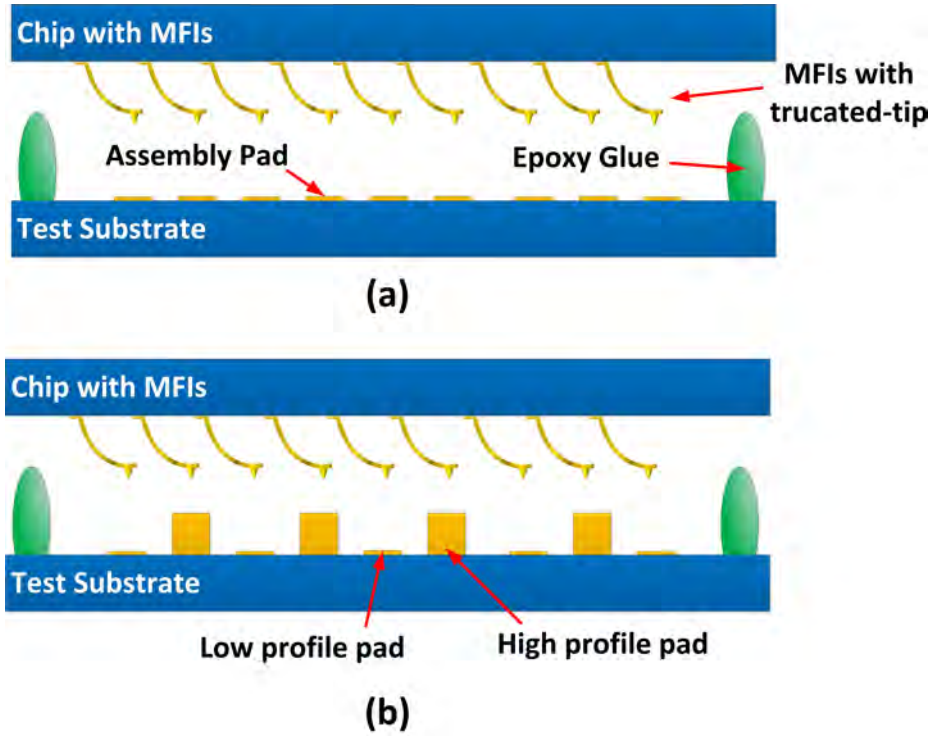


Figure 42: Two investigated assembly experiments: (a) assembly of a chip with MFIs on a substrate with uniform height pads multiple times for rematable assembly demonstration; and (b) assembly of a chip with MFIs on a substrate with non-uniform height pads for robust assembly demonstration.

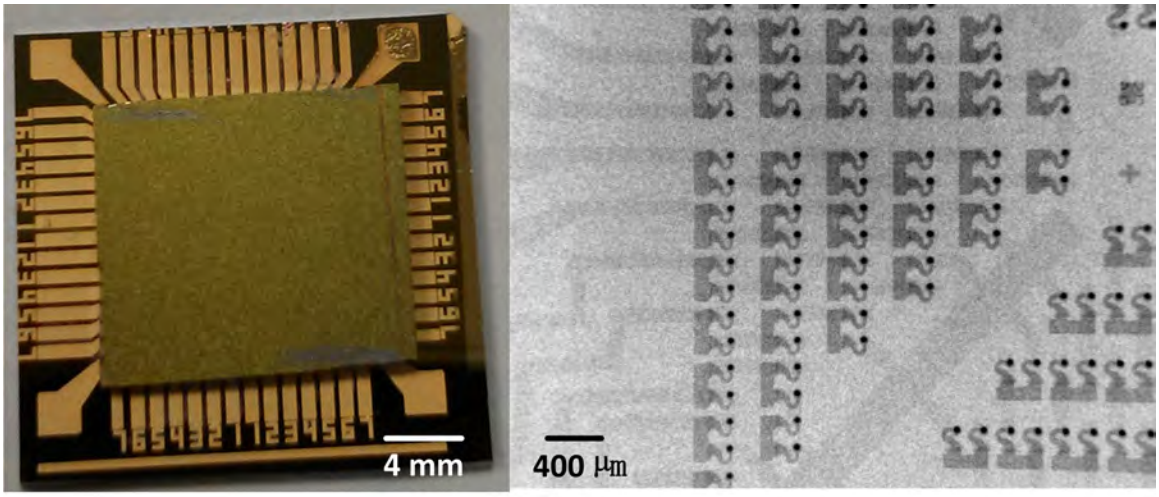


Figure 43: An optical image (a) and an X-ray image (b) of assembled test bed.

chips are assembled using a Finetech sub-micron resolution flip-chip bonder. Once aligned and mounted on the substrate, the chips were affixed by applying epoxy to the corners. The applied force during the bonding process was calculated based on the compliance, deformation depth and number of MFIs on the chip. For example, given a chip with 304 MFIs and assuming each MFI has a compliance of 5 mm/N and will be deformed by 30 μm during assembly, the applied force during assembly is 1.82 N.

An assembled test bed sample is shown in Figure 43 (a). After assembly, an X-ray imaging tool, Dage X-Ray XD7600NT, was used to verify assembly alignment accuracy. The X-ray image shown in Figure 43 (b) not only illustrates the alignment accuracy but also lack of any voids in the fabricated (electroplated) electrical links. In Figure 43 (b), the 3 μm thick traces on the substrate are represented in the x-ray image by the light gray traces; the dark dots on top of MFIs in the x-ray image are the truncated-cone tips.

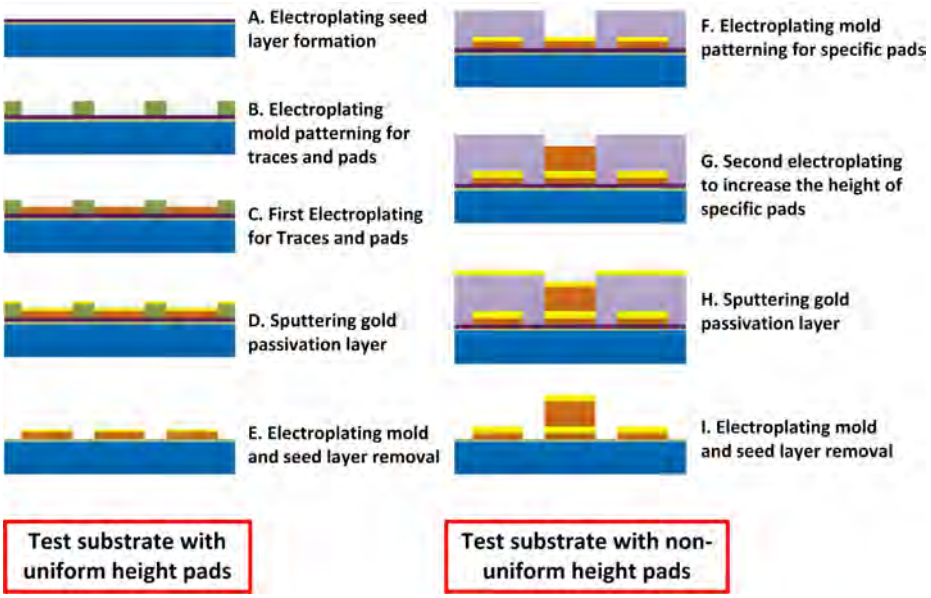


Figure 44: Fabrication process of the test substrate with uniform height pads (step A-E), and the test substrate with non-uniform height pads (step A-I).

4.2.3 Fabrication of Test Substrate

Figure 44 illustrates the fabrication processes of the two test substrates used in this work. The fabrication of the substrate with uniform height pads is shown in steps I-V: One lithography step was used to pattern the electroplating mold on top of sputtered Ti/Cu/Ti seed layer; pads and traces were formed by Cu electroplating; next, a 300 nm thick Au layer was sputtered as a passivation layer. After the Au layer lift-off and seed layer removal, the substrate with uniform height pads was obtained for the first set of assembly experiments (Figure 44 (a)). For the assembly on non-uniform height pads (Figure 44 (b)), in additions to steps A-E, a second plating process was used to form the non-uniform height pads (steps F-I).

Figure 45 shows the test substrate with various height pads. A surface topography scan using Dektak 150 profilometer was performed to characterize the height of the pads across the substrate. As shown in Figure 46 (a), the low profile pads are 3 μm tall, and the high profile pads are 48 μm tall, which leads to a 45 μm height difference.

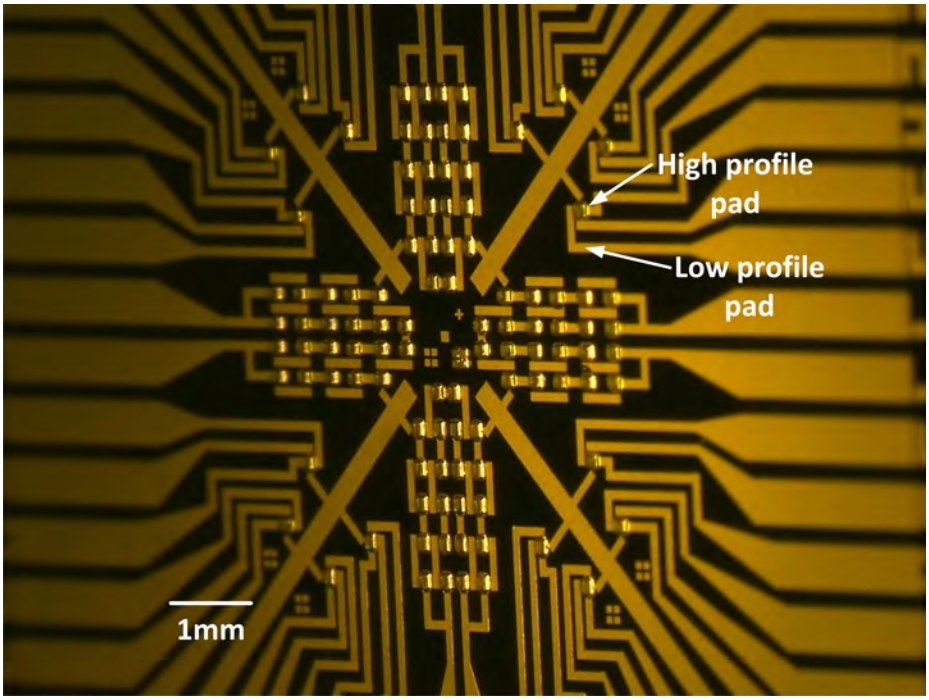


Figure 45: A test substrate with non-uniform height pads..

The surface roughness of the high profile pads (approximately 5 μm) is much larger than that of the low profile pads (approximately 1 μm) and was verified by SEM as well (SEM images of the surface of the high and low profile pads are shown in Figure 46 (b) and (c), respectively). The rougher surface of the high profile pads is believed to be caused by the higher deposition rate and longer deposition time used in the second electroplating step. The impact of surface roughness difference on the contact resistance will be discussed in Section 4.4.

4.3 MFIs Assisted Rematable Assembly

In this section, the assembly experiment shown in Figure 42 (a) is used to demonstrate the rematable assembly of chips consisting of Au-NiW MFIs with truncated cone tip.

4.3.1 Rematable Assembly

Four-point electrical measurements of the MFIs were performed using the test bed shown in Figure 47. The rematability of the MFIs is demonstrated by comparing

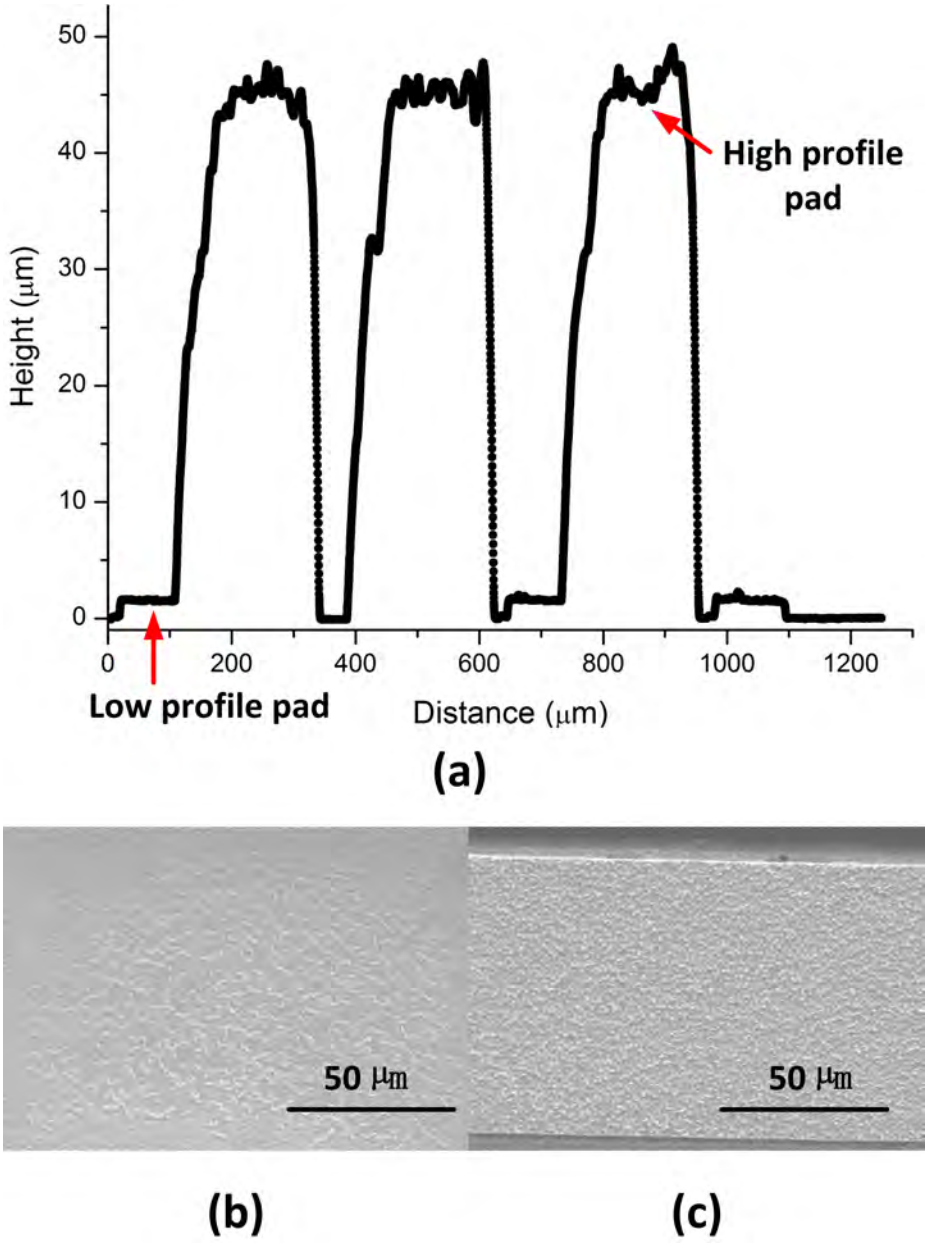


Figure 46: Surface profile of the test substrate with non-uniform pads (a), and the SEM images of the surface of high profile pad (b) and low profile pad (c).

the four-point resistance measurement results from a test bed in which the chip was assembled once to that of a test bed in which the chip was mounted and remounted for a total of ten-times.

Four-point resistance measurements were conducted using a Signatone Probe Station. The detailed schematic of the four-point resistance measurement setup is shown

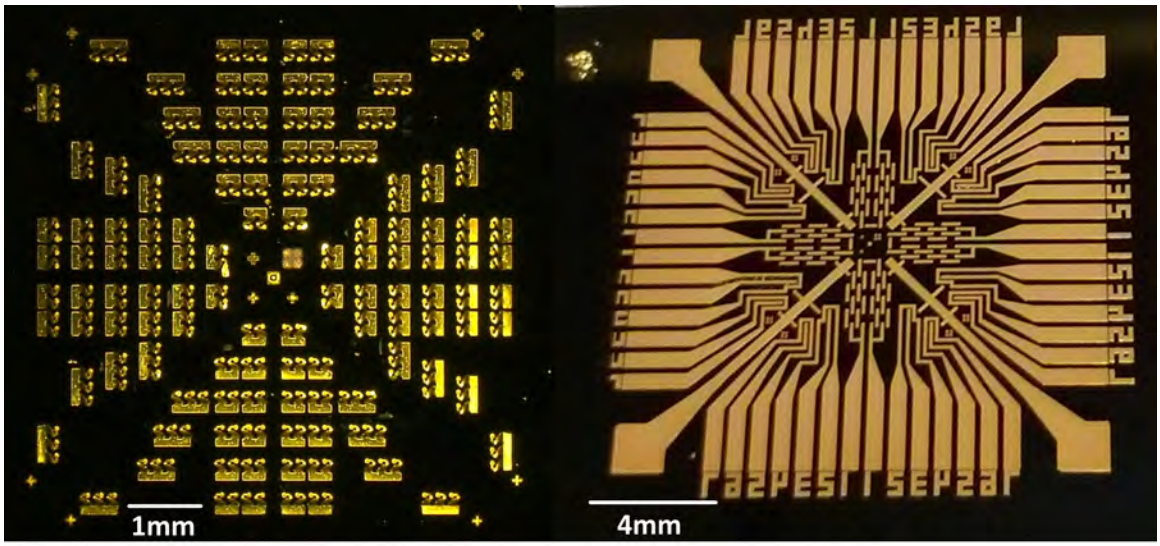


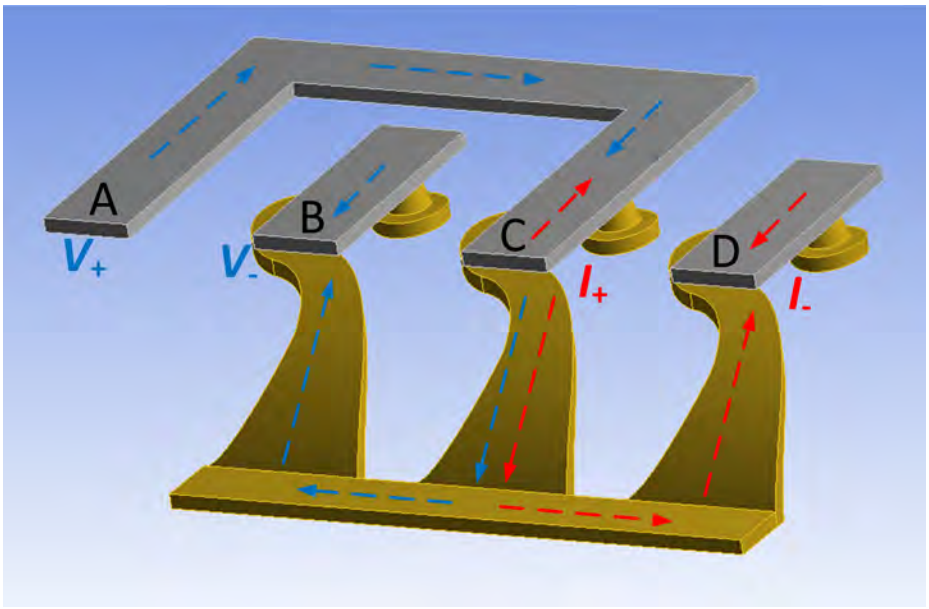
Figure 47: The test bed with four-point resistance measurement structures, which includes a chip with MFIs (a) and the corresponding substrate (b), is used for rematability verification.

in Figure 48 (a). X-ray imaging, as shown in Figure 48 (b), was used to ensure the testing structure was aligned correctly. The measured resistance includes that of the MFI plus the contact resistance to the pad. The average resistance of 12 assembled samples is 103.21 mΩ, and the standard derivation is 4.06 mΩ.

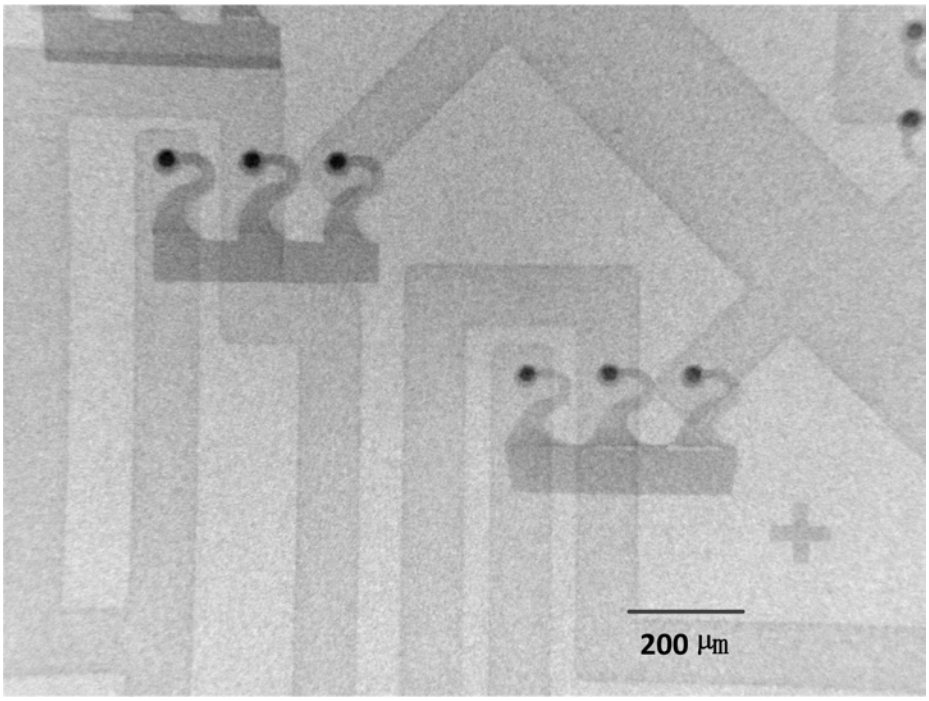
Table 4: Resistance characterization for rematable assembly using MFIs with contact tip

	Average Resistance (mΩ)	Standard Deviation (mΩ)
After 1st assembly	103.21	4.06
After 10th assembly	105.99	4.4

To demonstrate the rematability, the test bed shown in Figure 47 was repeatedly assembled for 10 times and then measured using the four-point resistance setup described previously. The measured average resistance is 105.99 mΩ. As summarized in Table 4, compared with the results from the test bed in which the chip was only mounted once, the difference in the resistance is negligible (less than 3 mΩ). SEM



(a)



(b)

Figure 48: The schematic (a) and X-ray image (b) of assembled four-point resistance measurement structures.

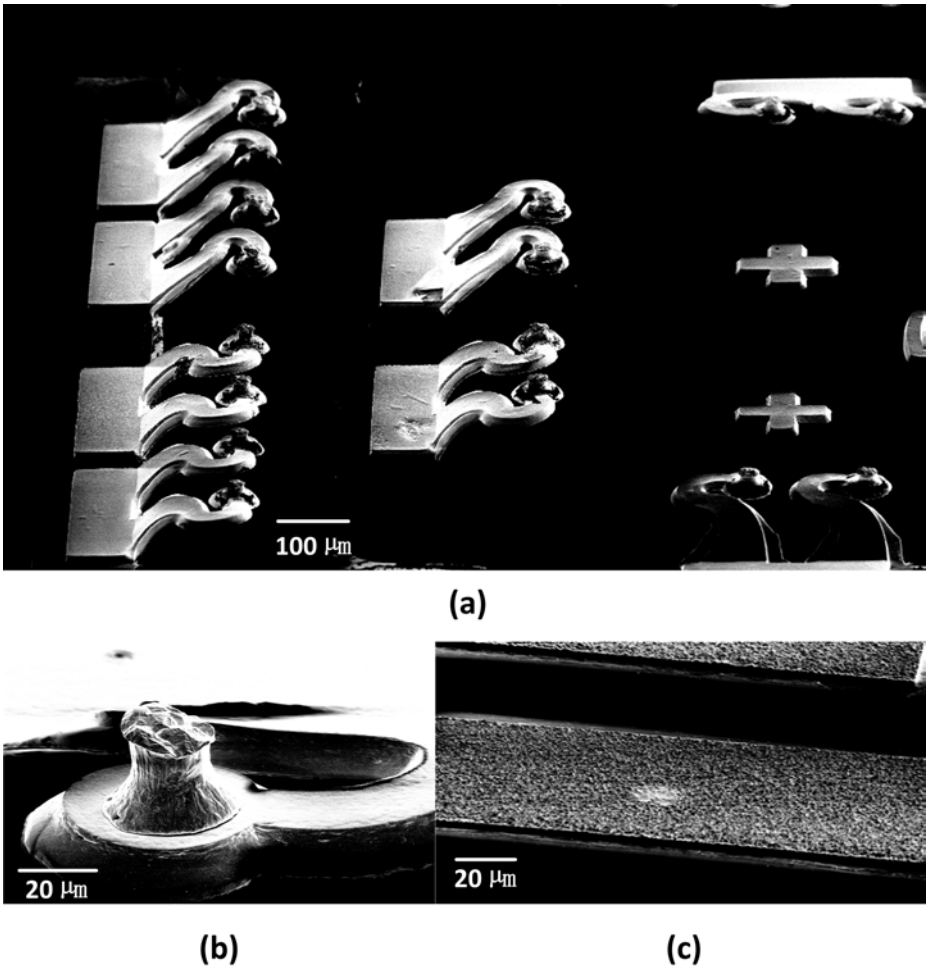


Figure 49: SEM pictures of Au-NiW MFIs (a), including detailed pictures of tip (b) and traces (c), which have repeatedly assembled on a test substrate with uniform height pads for 10 times.

images were taken, as shown in Figure 49, to verify that after repeated assembly the Au-NiW MFIs could maintain their original profile.

4.3.2 Yield and Current Carrying Capability Characterization

The yield and current carrying capability characterization were performed on the test bed shown in Figure 50. The chip and substrate were designed to form a daisy chain of serially interconnected MFIs.

Figure 51 shows three different daisy-chain lengths on the assembled test vehicle: daisy chains C1, C2, and C3 contained a total of 24 MFIs, 18 MFIs, and 12 MFIs,

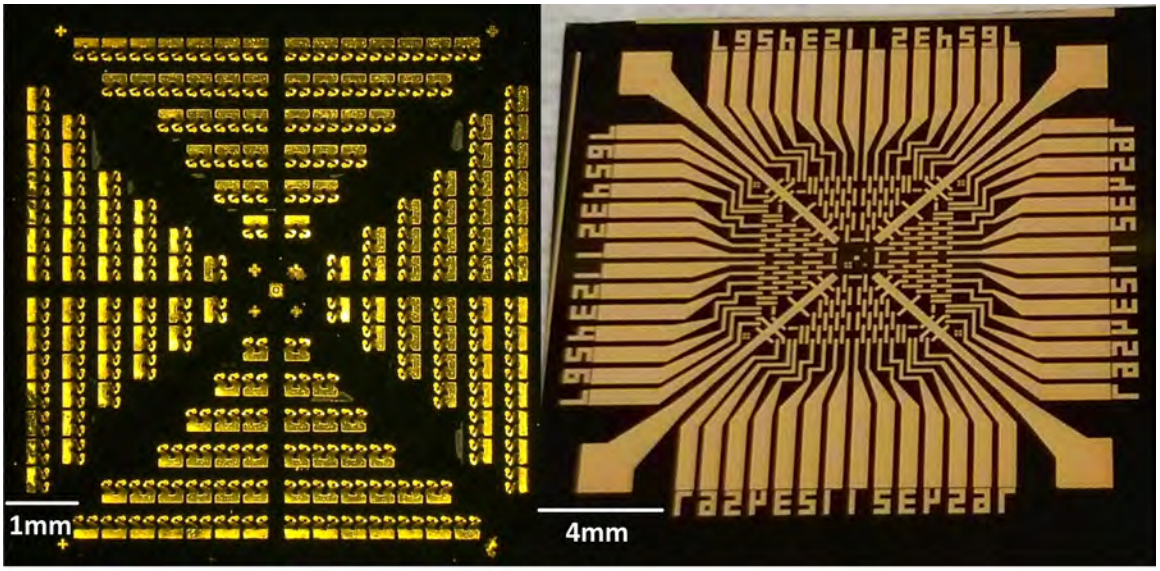


Figure 50: The test bed with daisy chain measurement structures, which includes a chip with MFIs (a) and the corresponding substrate (b), is used for yield and current carrying capability characterization.

respectively. The measured resistance of daisy chains C1, C2 and C3 is 2.897 Ω, 2.115 Ω and 1.378 Ω, respectively, as summarized in Table 5.

Table 5: Resistance of various daisy chain design

Daisy Chain Design	Number of MFIs	Average Resistance (Ω)	Standard Deviation (Ω)
C1	24	2.897	0.045
C2	18	2.115	0.025
C3	12	1.378	0.03

Daisy chain C1 was used for current carrying capability measurement as well. The test setup is shown in Figure 52. The assembled test bed was attached on an FR-4 test board with an opening at the center. An Agilient N6705B power analyzer was used as a power supply as well as for recording the input current and the output voltage of the test bed. Since significant amount of heat is generated during the current carrying capability test, an air cooled heat sink, RCK-ZAIO-92, designed for

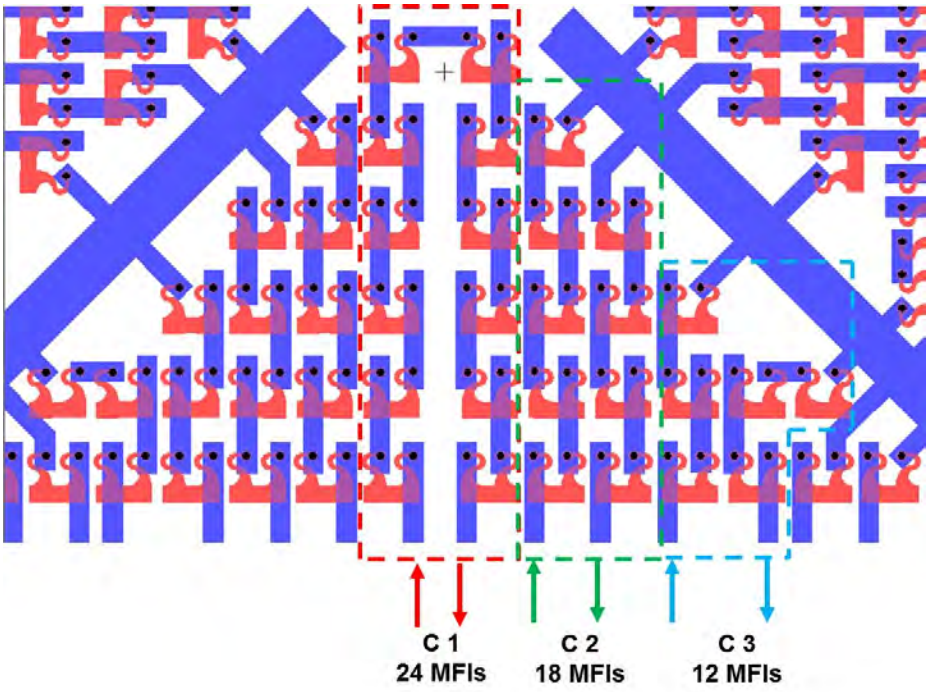


Figure 51: Three daisy chain designs consisting different number of MFIs: daisy chain C1, C2 and C3 contained 24, 18 and 12 MFIs respectively.

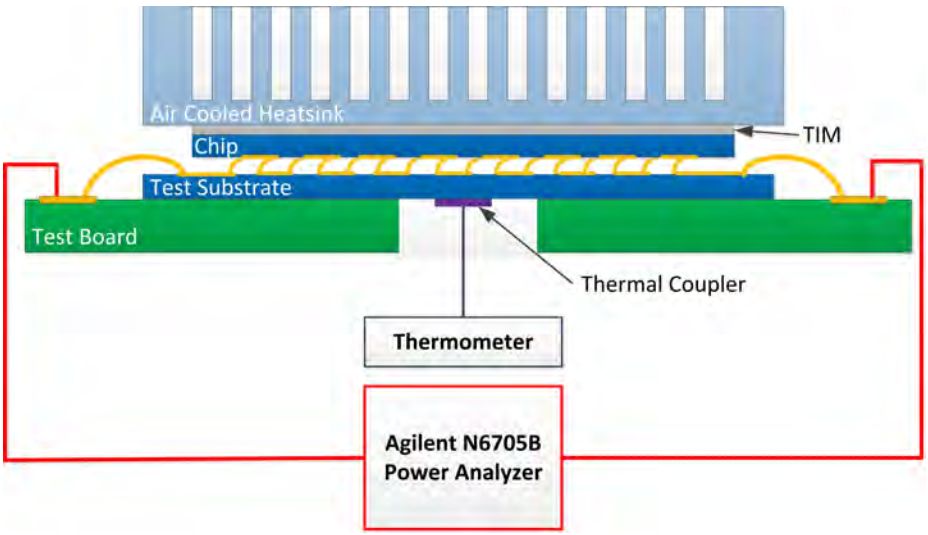


Figure 52: The schematic of the test bed used for current carrying capability test.

an Intel i7 processor, was attached on top of the test vehicle via a TIM layer to avoid overheating. In addition, a thermal coupler was attached on the test bed through the opening of the test board to monitor the real-time temperature of the test bed.

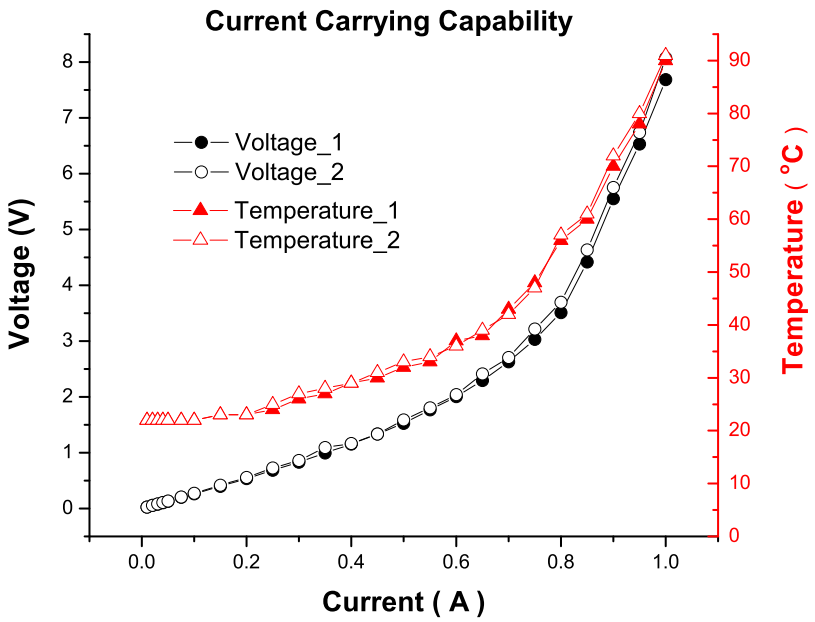


Figure 53: The Current-voltage and current-temperature curve of current carrying capability test performed on a test bed with daisy chain design.

For each test, the input current is increased from 10 mA to 1 A . The current increases at an increment of 10 mA for the current range of 10 mA to 50 mA; the increment is increased to 50 mA for the current range of 50 mA to 1000 mA. After the first current ramp was accomplished, the test bed was cooled down for 20 minutes. Once the sample reached approximately room temperature, a second run was performed for comparison. The voltage and corresponding temperature of the two runs were recorded, as shown in Figure 53. At the beginning of each test, the voltage was linear with respect to the input current. The slope of the I-V curve is 2.89 Ω, which is the resistance of daisy chain C1 at room temperature. This linear relationship remained until the current reached approximately 0.4 A, which coincides with the temperature of the assembled test vehicle reaching 30 °C. As the input current and power increases further, the voltage becomes non-linear to input current, which indicates an increased daisy chain resistance. Such resistance change is believed to be

caused by the increased temperature, which is plotted in Figure 53 as well. As shown in Figure 53, the I-V curves from these two runs are overlapped, which indicates that the MFIs can sustain an input current of 1 A.

4.4 MFIs Assisted Assembly on Non-planar Substrate

In this section, temporary assembly on non-planar substrate is demonstrated using the test bed shown in Figure 42 (b). As noted previously, the pad-to-pad height difference on the substrate was 45 μm.

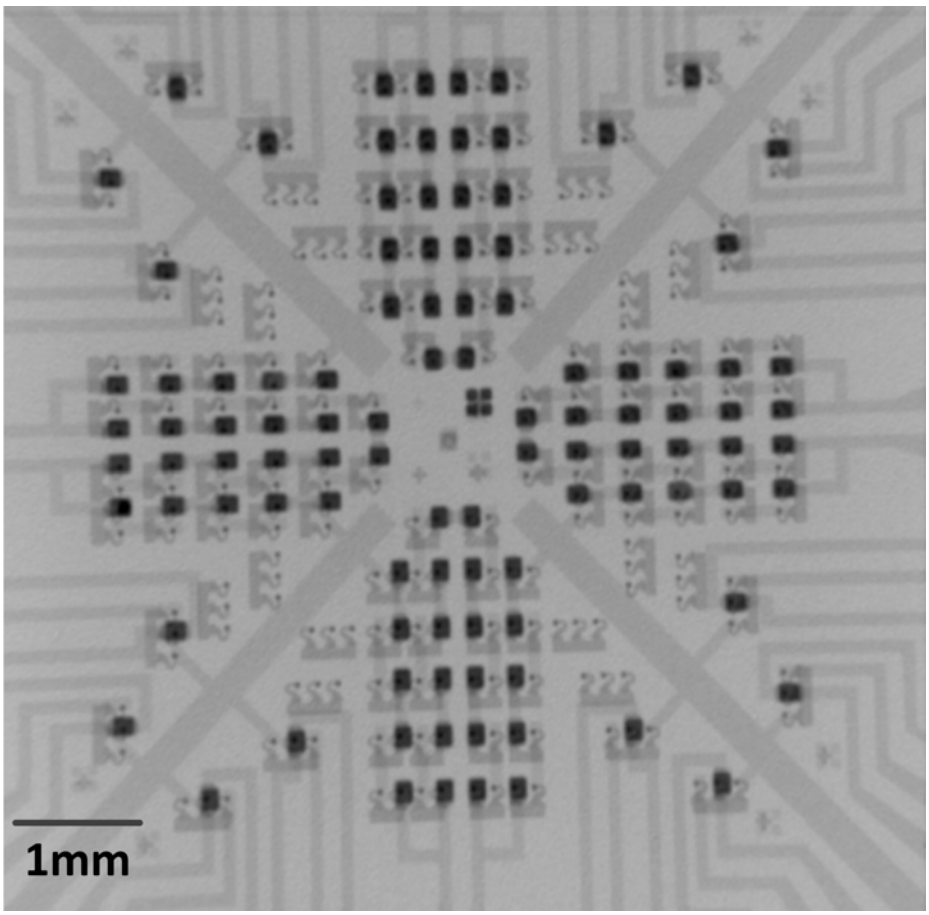


Figure 54: X-ray image of the assembled test bed with non-uniform height pads.

As shown in Figure 54, the X-ray image following assembly indicate that the chip was well aligned with the substrate. The black dot on top of the MFIs is the truncated-cone tip, and the dark rectangular area above the center-located MFIs is

the high profile pads, which are 48 μm tall as described previously.

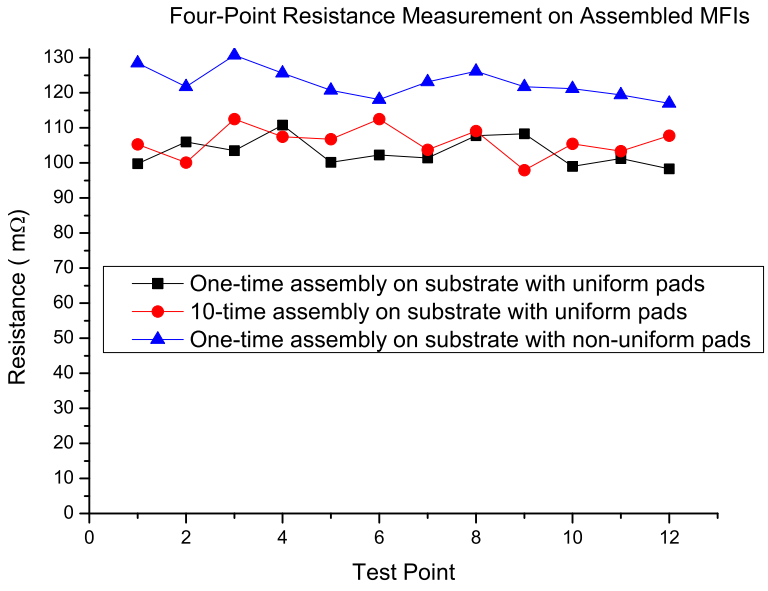


Figure 55: Four-point resistance measurements of MFIs assembled on various test substrates.

Four-point resistance measurements of the assembled MFIs making contact to the high-profile pads are summarized in Figure 55. The average resistance of the assembled MFI/high-profile pad combination is 122.81 mΩ with a standard deviation of 4.16 mΩ. The measured average resistance is 9.6 mΩ larger than the average resistance of the assembled MFI/low-profile pad combination reported in Section 4.3 and summarized in Table 4. This increase in resistance can be attributed to both the thicker pad and the increased surface roughness described previously, which can increase the contact resistance.

4.5 Conclusion

Au-NiW MFIs with truncated cone tip were wafer-level batch fabricated and used to demonstrate rematable assembly on various substrates. The truncated cone tip enhances bonding pad scrubbing while maintaining a long lifetime by avoiding tip

damage. Four-point resistance measurements were performed on the sample after a single and ten repeated assemblies, and the measured results verified the assembly using MFIs is rematable. In addition, daisy chain and current carrying capability measurements indicate that the Au-NiW MFIs form reliable interconnects and exhibit a large current carrying capability of 1 A. Lastly, due to the large vertical range of motion, Au-NiW MFIs enable the assembly of a silicon chip on a substrate with up to 45 μm surface variation.

CHAPTER 5

MULTI-PITCH MULTI-HEIGHT (MPMH) MFIs

5.1 Introduction

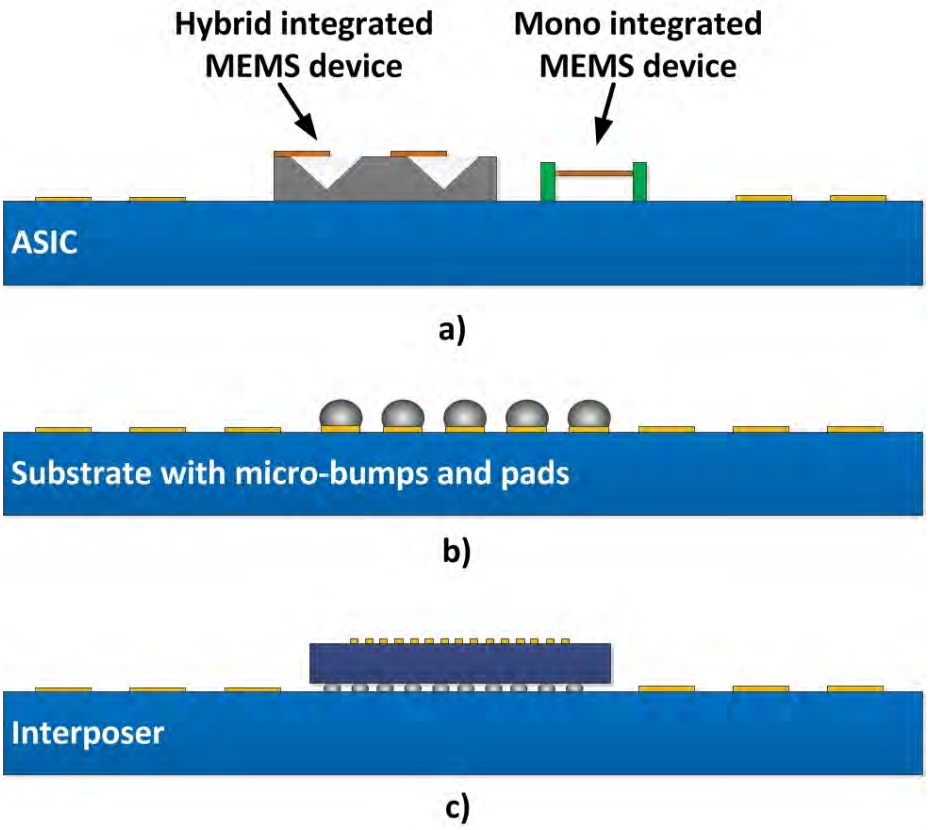


Figure 56: Potential applications of MPMH MFIs: a) Assembly on substrate with fragile MEMS structures, b)Probing on substrate with micro-bumps and pads simultaneously, and c) Assembly on the embedded chip with fine I/O array.

The MFI arrays formed using the process technologies developed in Chapters 2, 3 and 4 have uniform vertical height. Such uniform height MFIs are suitable for applications that include: 1) assembly on an initially flat substrate to overcome the CTE mismatch induced warpage during the bonding process or field use, and 2) assembly on a substrate that has a large surface variation but is not sensitive to the

assembly force and contact position since the different magnitudes of deformation will yield a large difference in MFI contact force and scrubbing length.

For the case of chip mounting on a substrate with large surface variation and sensitivity to assembly force or contact position, a chip containing multi-pitch and multi-height (MPMH) MFIs may improve the assembly yield. For example, as shown in Figure 56 (a) and (b), low profile MFIs with smaller deformations and reaction forces are necessary to prevent damage of the fragile MEMS structures and micro bumps during assembly. Another potential application for hybrid MFIs is shown in Figure 56 (c) in which the low profile MFIs with fine pitch can minimize the scrubbing length during assembly and ensure accurate and reliable interconnection when a second interposer is stacked above an initial interposer with assembled components.

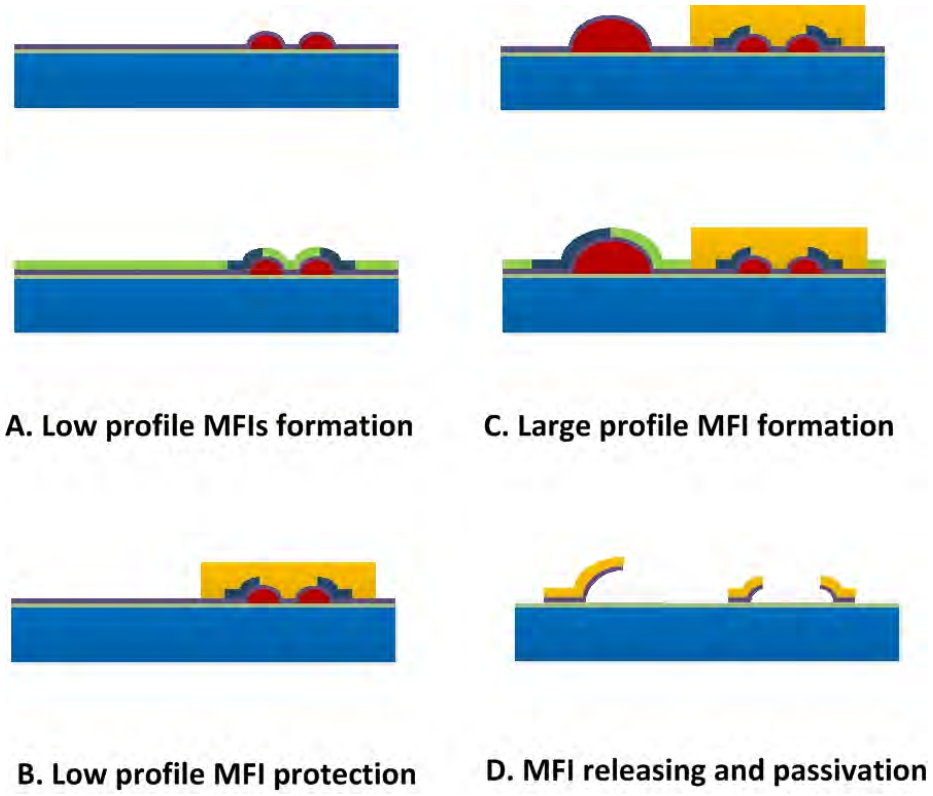


Figure 57: Brute-force approach to form MPMH MFIs.

A brute-force approach to form such a MPMH MFI array could be achieved by

fabricating the MFIs with different heigth/pitch sequentially, as shown in Figure 57. Due to the complexity of the process, the fabrication throughput and yield may be significantly lower compared to the uniform-height MFI process. Therefore, in this chapter, a novel MPMH MFI process technology that extends our prior proccesses with one additional lithography step is developed to address the cost and throughput issues and to enable the applications shown in Figure 56.

This chapter first describes the formation of domes with various heights (multi-height domes) using double-lithography and double-reflow processes. Fabrication challenges and dome height verification are discussed as well. Next, the fabrication process of multi-pitch MFIs on multi-height domes using photoresist spray-coating is described. Finally, the mechanical and electrical experimental characterization of the MPMH MFIs is reported.

5.2 Multi-height Domes

The formation of domes with various heights is the key to realizing MPMH MFIs. In this section, the fabrication of multi-height domes using double-lithography and double-reflow processes is reported. Next, challenges in the fabrication of high yield multi-height domes are discussed along with their solutions. Finally, the profile of multi-height domes is measured using contact profilometer.

5.2.1 Double-lithography and Double-reflow

The double-lithography and double-reflow processes are shown in Figure 58. This process extends Yang's double-exposure process [67]. The process begins with the formation of large sacrificial polymer domes using the first exposure and reflow (steps I-IV shown in Figure 58); note that this is the same process used to fabricate the previously reported uniform-height MFIs. Moreover, note that the formed domes, which are fabricated using positive photoresist, are unexposd at this stage in the process. Thus, following a controlled first reflow step, the positive photoresist domes

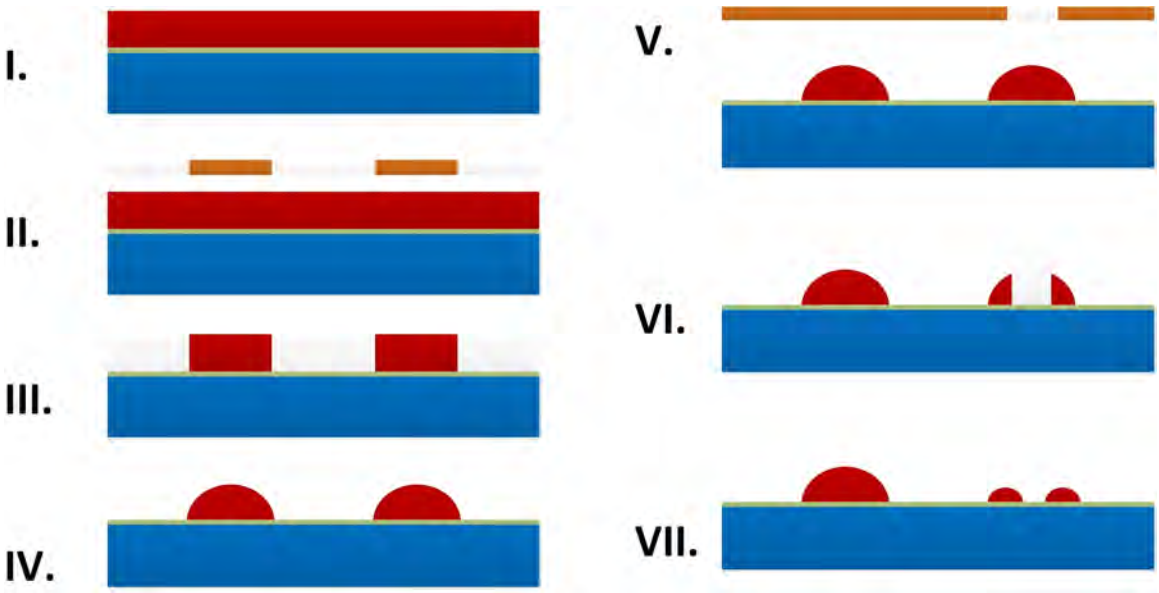


Figure 58: Double-lithography and double-reflow processes.

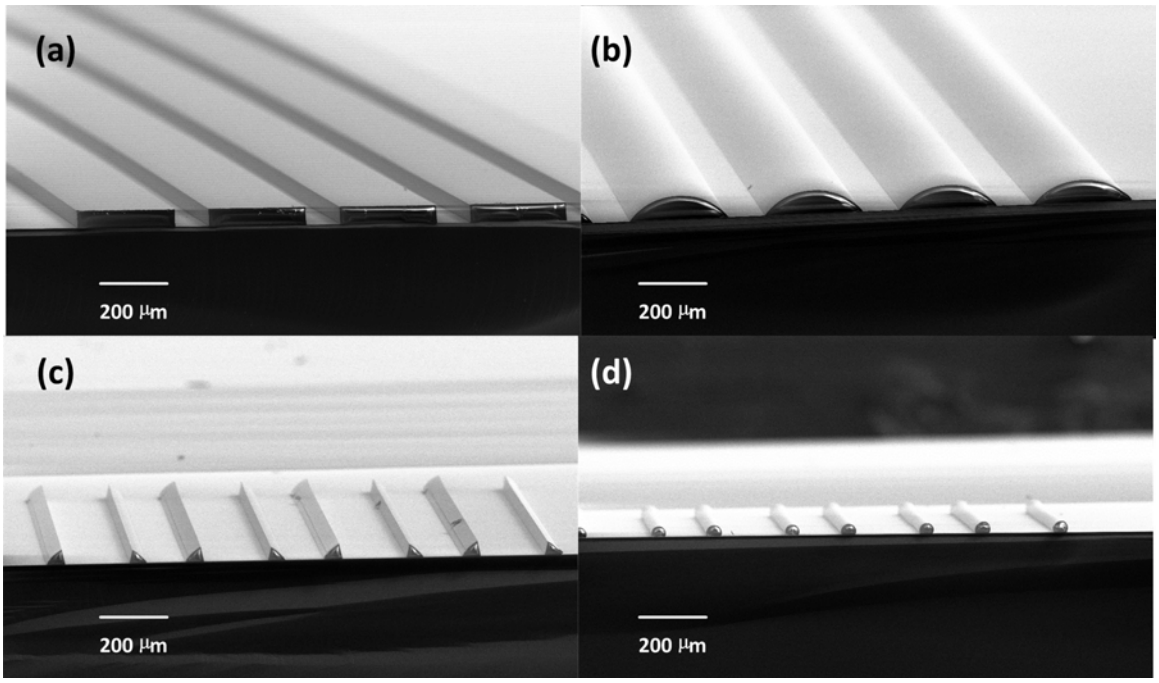


Figure 59: Key steps of double-lithography and double-reflow: a) polymer strips after first development; b) polymer domes after first reflow; c) polymer strips after second development and d) polymer domes after second development.

are UV-light sensitive. Next, a second exposure (step V shown in Figure 58) is performed on specific domes (i.e. the right dome in step V of Figure 58). Following

the second development, only the edges of the corresponding original domes remain. During the second reflow, these newly formed dome edges reflow to form lower height domes. Because the height of the domes formed by the edge strips is smaller than the original dome height (the height after first reflow), this double-lithography and double-reflow processes are suitable to the formation of MPMH MFIs. SEM images of the key steps in the double-lithography and double-reflow processes are shown in Figure 59.

5.2.2 Fabrication Challenges

The challenegs in the fabrication of multi-height domes are described in this section and include: 1) misalignment of the second exposure step, and 2) dome twisting and bubbling resulting from the second development and reflow processes.

5.2.2.1 Second Exposure Misalignment

There are two fabrication challenges associated with any misalignment during the second exposure: dome height variation and dome peak position shift.

Low-profile Dome Height Variation

The height of the low profile domes is determined by the width and the position of the remaining dome edges following the second development. The remaining dome edge is UV defined during the second exposure step. Therefore, the alignment accuracy of the second exposure step significantly affects the final height of the low profile domes. If both edges are utilized, as shown in Figure 60, the height variation among the low profile domes induced by the second exposure step misalignment will be worse than the case using one edge. Assuming a pair of low-profile domes formed from a single dome, the height of one dome decreases as the height of the other dome increases, which induces a large height variation as shown in Figure 61.

Low-profile Dome Peak Shift

Because the surface tension dominates the dome profile after reflow, the peak of

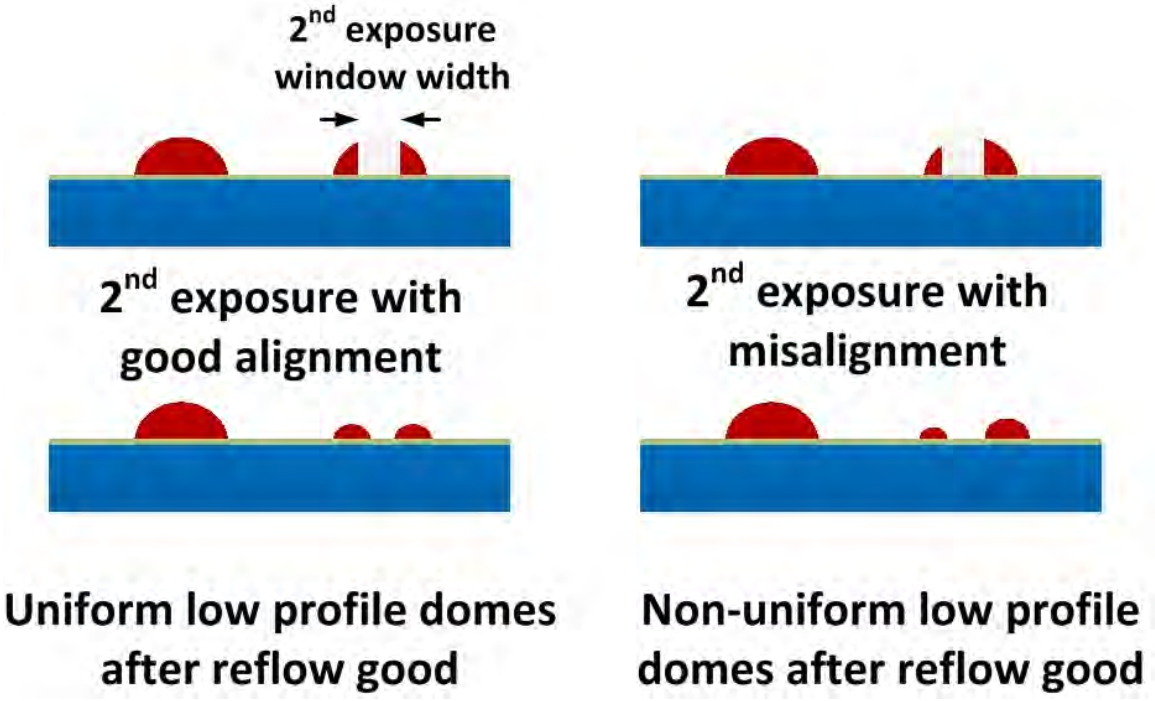


Figure 60: Non-uniform domes induced by the misalignment of second exposure.

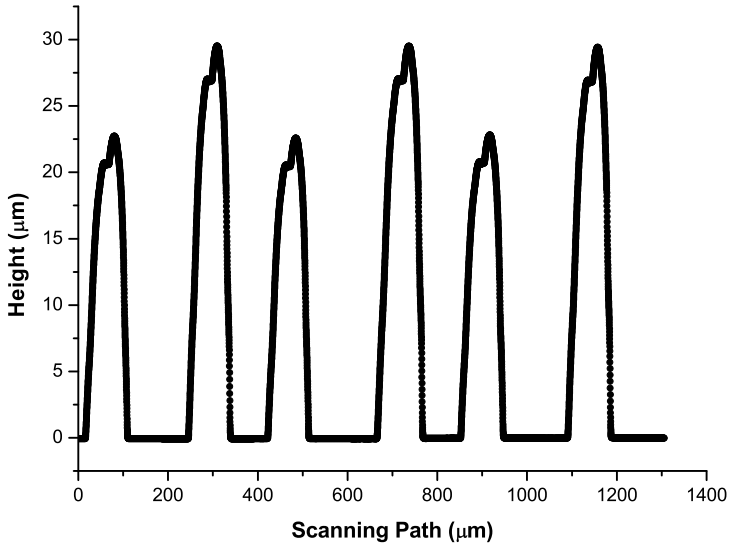
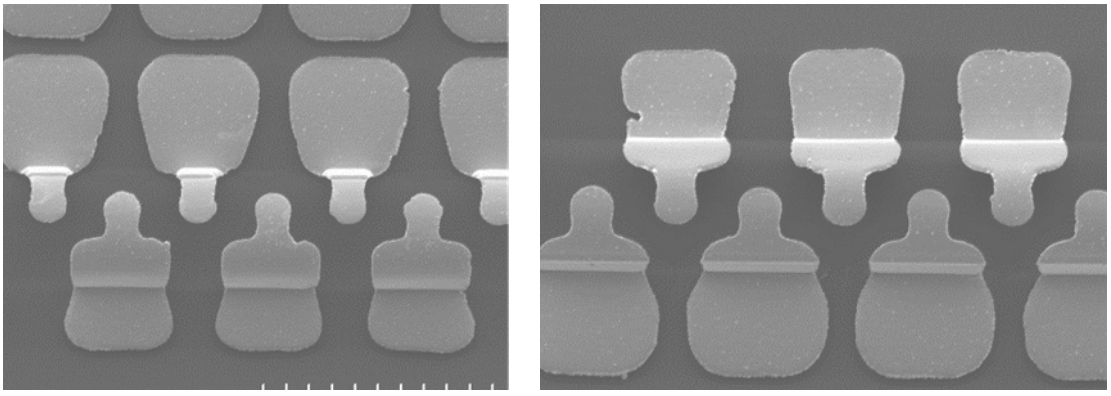


Figure 61: Dome height variation induced by second exposure misalignment.



(a) (b)

Figure 62: MFI peak position shift induced by second exposure misalignment: (a)Peak position shift induced by misalignment, and (b) No peak position shift after correct second exposure.

the low-profile dome is always along the center of the remaining dome edge after the second development. If the misalignment occurs during the second exposure, the peak position of the low-profile domes will shift. Dome peak position shift becomes very obvious after the MFI formation, as shown in Figure 62. The height and length of the free-standing portion of the MFIs formed on a dome with a shifted peak position (Figure 62 (a)) will be different from those that are formed using a second exposure step with no misalignment (Figure 62 (b)). A variation in MFI dimensions will results in an MFI array with non-uniform mechanical and electrical properties, which may present challenges during both assembly and device operation.

5.2.2.2 Dome Twisting and Bubbling in Photoresist

The fabrication challenges resulting from the second development and reflow steps, which include dome twisting and bubbling (Figure 63), are described as follows.

Dome twisting or delamination following the second photoresist development is caused by the poor adhesion between the dome and the substrate. Using a surface promotor (HDMS, for example) prior to photoresist spin-coating and carefully releasing the thermal stress accumulated during second post-bake will alleviate this issue.

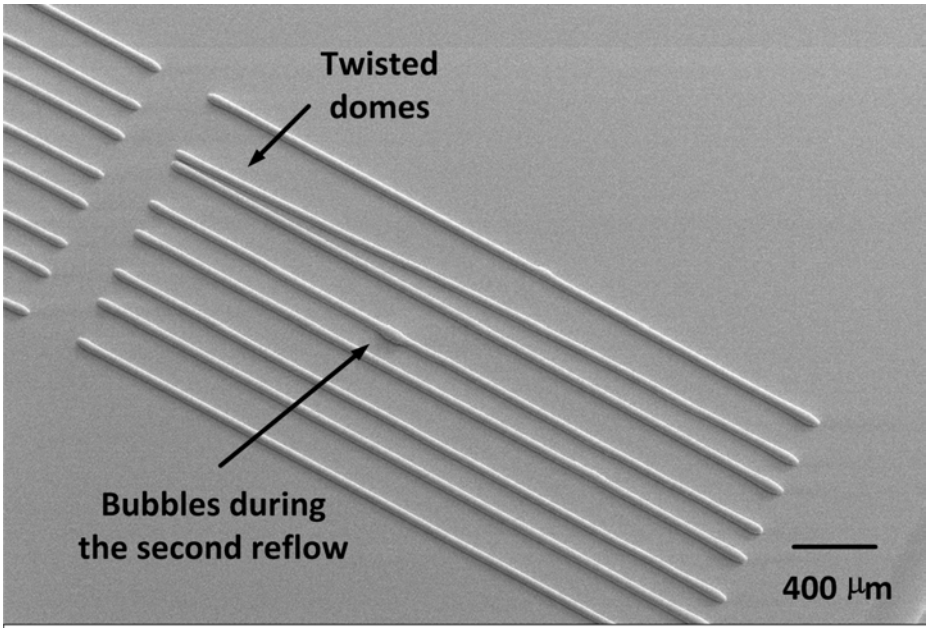


Figure 63: Two fabrication challenges in dome formation process: (a) Dome twisting after second exposure, and (b) bubbles formation in photoresist during second reflow.

In addition, the large DI water surface tension during the wafer drying process could twist the remaining polymer strips following the second development step as well.

Similarly to the dome outgassing discussed in [57], dome bubbling is induced by insufficient soft-baking of photoresist after the first reflow. Because the dome height is low, outgassing is more severe for the low-profile domes.

5.2.3 Multi-Height Dome Characterization

The multi-height dome array formed using double-lithography and double-reflow processes is shown in Figure 64. There are four different zones (I-IV) in the array with each zone corresponding to a specific dome height; the measured height for each of the four zones is shown in Figure 65.

The dimensions of the multi-height domes are summarized in Table 6. The domes in Zone I are not exposed during the second lithography step and have the largest width (300 μm) and height (66 μm). The domes in Zone II-IV are formed following the second lithography and reflow steps. The second exposure window width

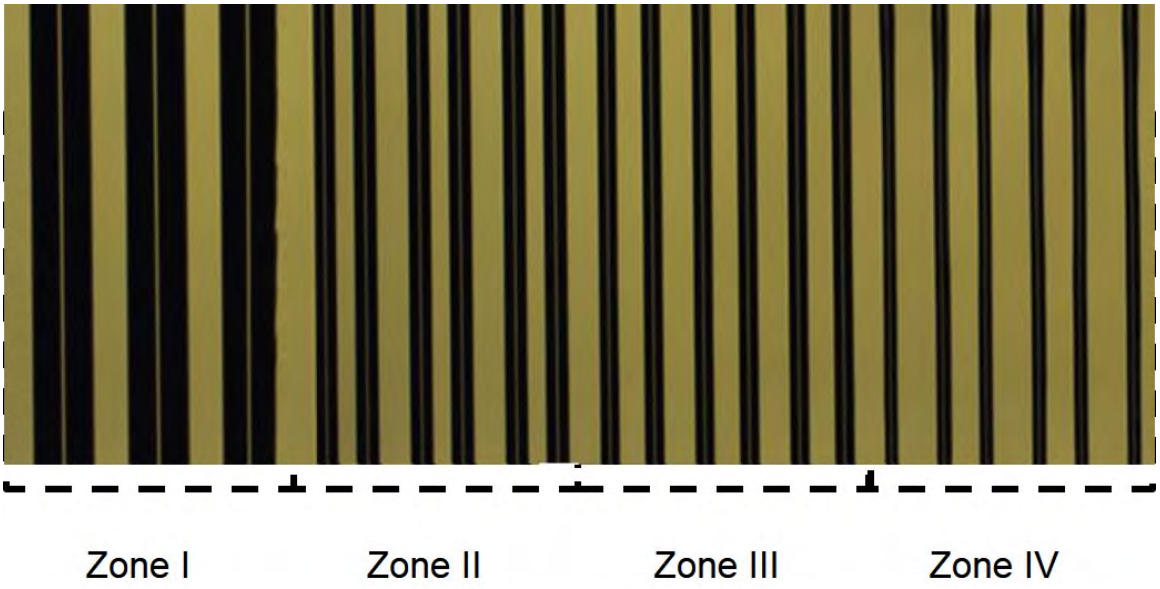


Figure 64: Multi-height domes after double-lithography and double-reflow processes.

defines the width of the exposed area on the original domes (300 μm wide), which also determines the width of the removed area from the initial dome, as shown in Figure 60. Therefore, in Zone II-IV, *Original dome width* = 2 × *Dome width* + *Second exposure window width*. As shown in Table 6, the dome height decreases as the width of the second exposure mask window width increases. The maximum height difference among the domes formed in this array is 40 μm.

Table 6: Dimensions of multi-height domes

Zone number	Dome width (μm)	Second exposure window width (μm)	MFI pitch on dome (μm)	Dome height (μm)
I	300	0	150	66
II	100	100	80	45
III	75	150	60	38
IV	50	200	50	26

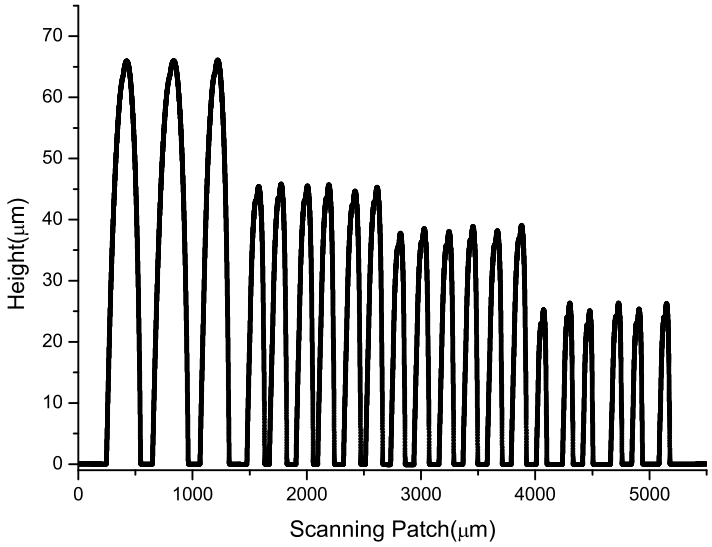


Figure 65: The surface variation data recorded by a Dektak profilometer verifies the domes with various heights.

5.3 Fabrication of MPMH MFIs

Figure 66 illustrates the fabrication process of MPMH MFIs. Since the fabrication of the multi-height domes was discussed in Section 5.2, this section will focus on the fabrication of multi-pitch MFIs.

The critical step in the fabrication of multi-pitch MFIs is to pattern a photoresit electroplating mold above the multi-height domes. Photoresist spray-coating is adopted here to form a uniform photoresist layer above the multi-height domes. Due to the large height variation between the domes (up to 40 μm), contact exposure only occurs on the top surfaces of the highest domes in Zone I. The patterns on top of the lower height domes are obtained by proximity exposure with a gap of up to 40 μm. Following the optimization of the exposure dose and development time, an electroplating photoresist mold with a large array of multi-pitch MFIs is obtained, as shown in Figure 67. The dimensions of the patterns shown in Figure 67 are summarized in Table 6. The finest in-line pitch of the MFIs is 50 μm; later in Section 7.2, we

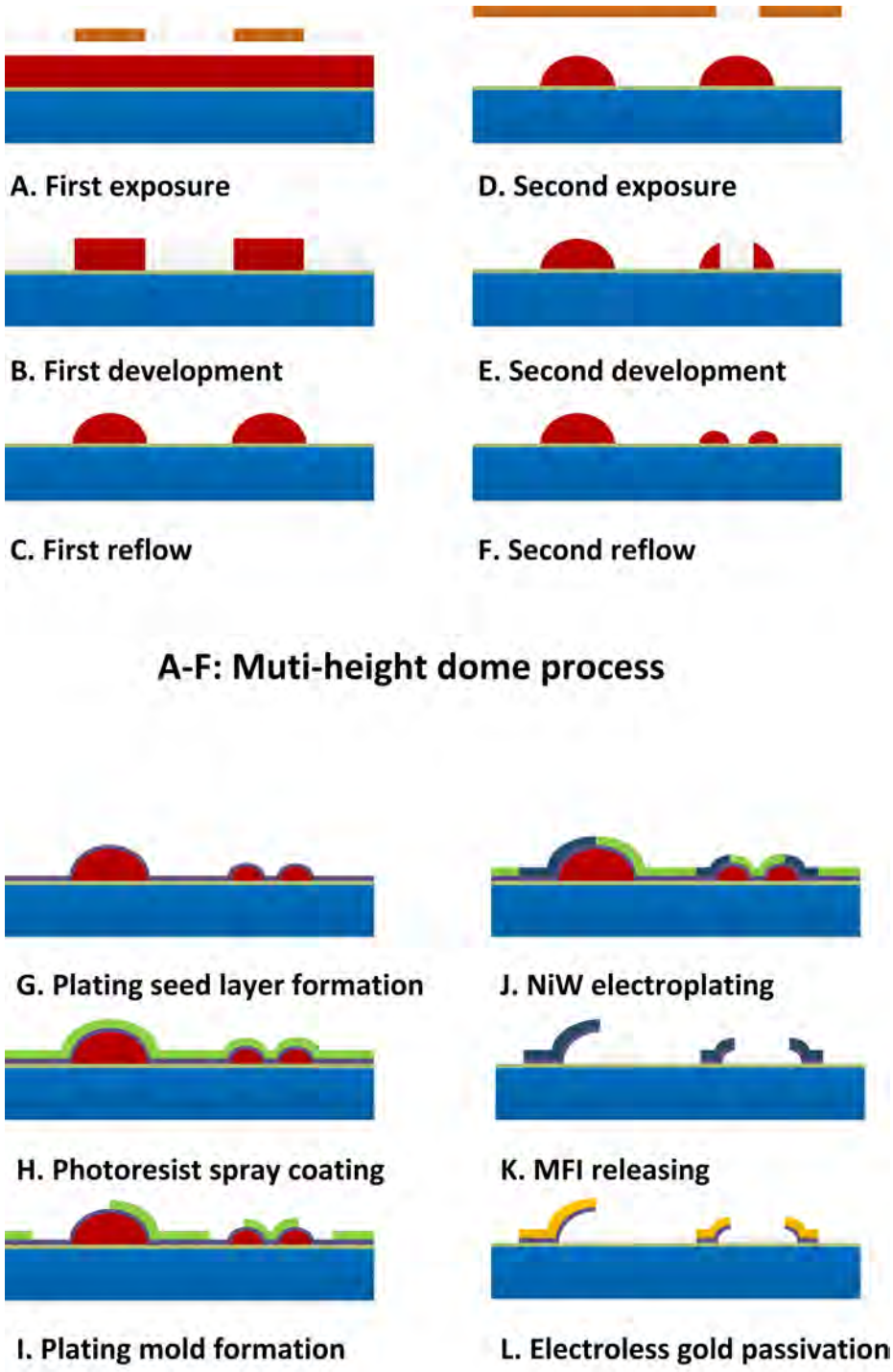


Figure 66: Fabrication process of MFIs with multi-height multi-pitch.

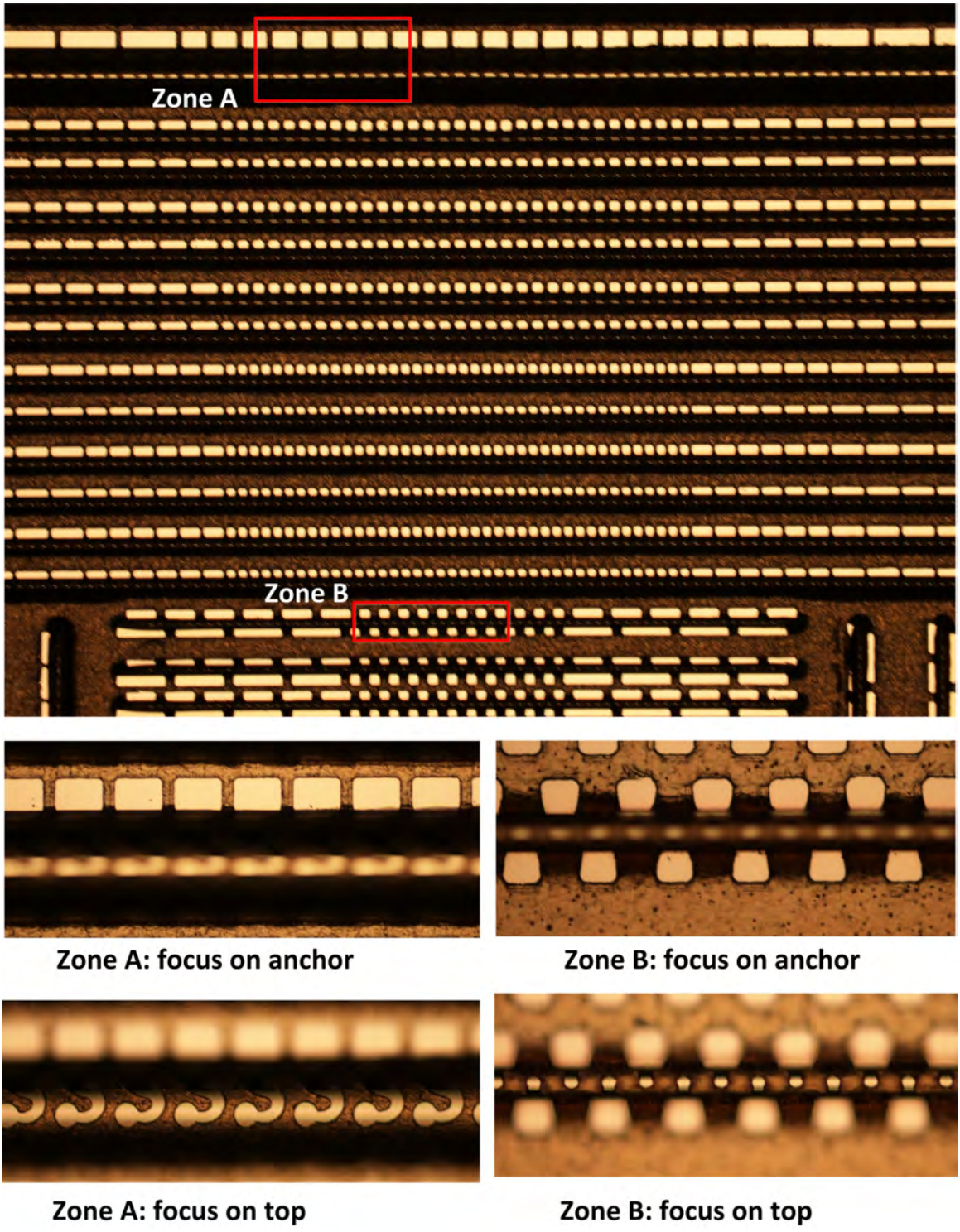


Figure 67: An electroplating mold with a large array multi-pitch MFIs pattern. Clear patterns are obtained on the area with large-profile MFIs (Zone A) and the area with low-profile MFIs (Zone B).

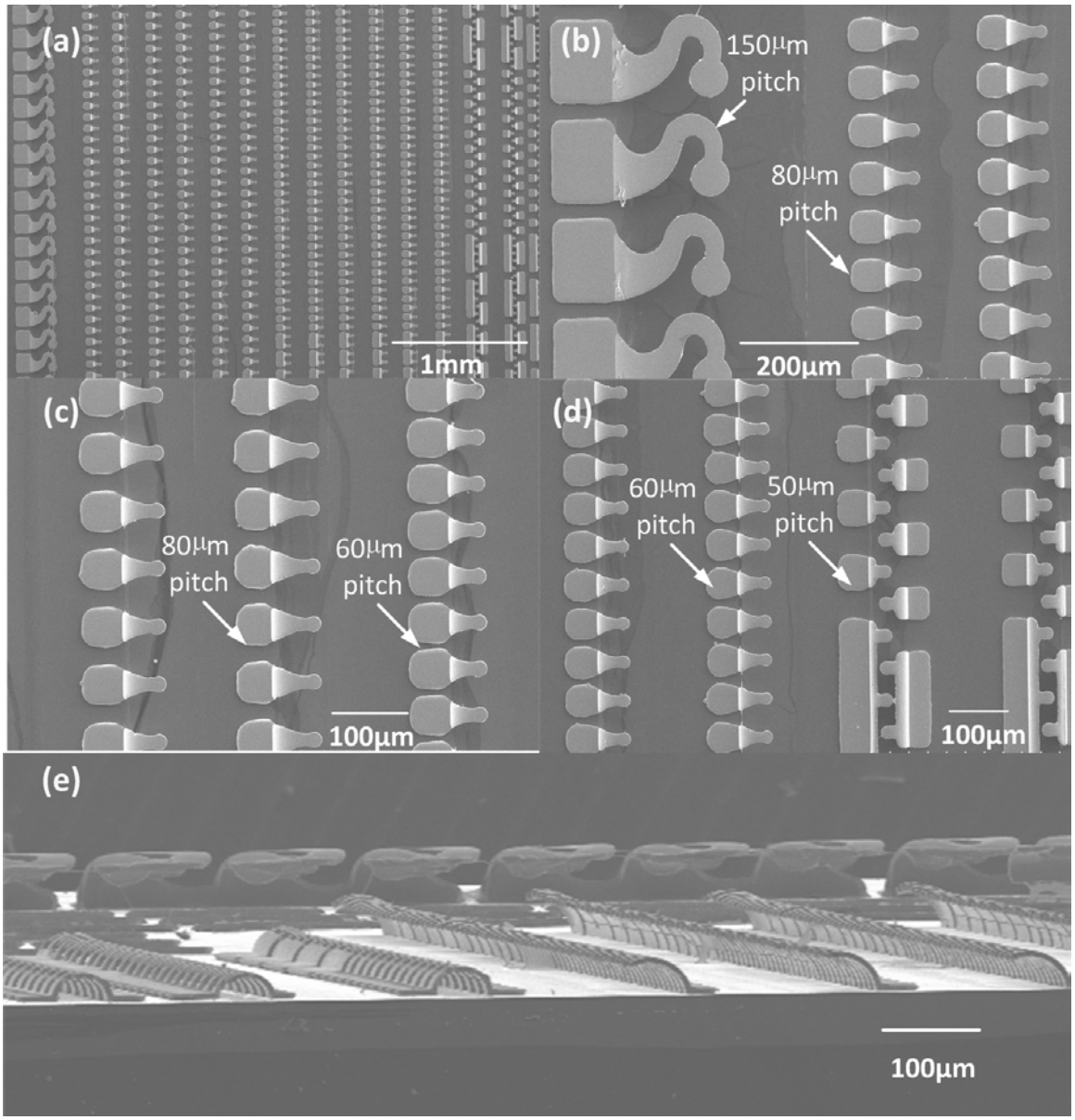


Figure 68: The overview (a) and more details (b-e) of multi-height multi-pitch MFIs.

describe MFIs with a 30 μm in-line pitch.

Following electroplating mold, seed layer, and sacrificial multi-height domes removal, free-standing MPMH MFIs array is obtained, as shown in Figure 68. Overview of the MPMH MFI array is shown in Figure 68 (a) with more details shown in Figure 68 (b-d). Figure 68 (e) shows a prospective view of the MPMH MFIs.

5.4 Mechanical and Electrical Characterization

Mechanical characterizations using indentation tests and electrical characterizations using four-point tests are described in this section.

5.4.1 Mechanical Characterization of MPMH MFIs

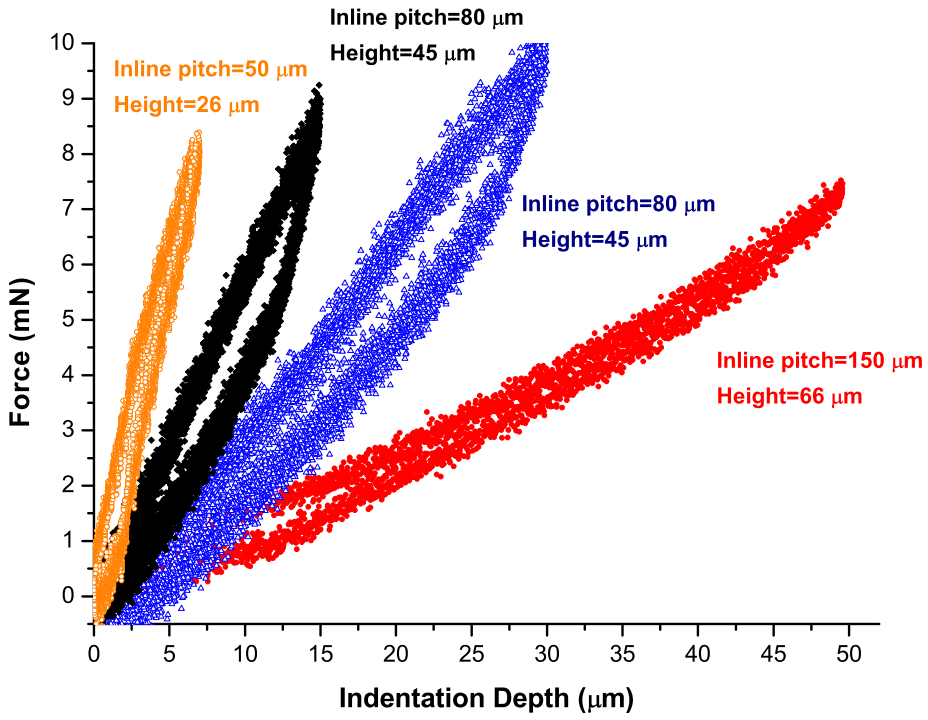


Figure 69: Indentation results of multi-pitch multi-height MFIs.

Indentation tests are performed using the same procedures discussed in Section 2.4.1. The results of indentation tests are plotted in Figure 69 and summarized in Table 7 as well. Because all MPMH MFIs are formed using NiW electroplating (thus, they are all electroplated in parallel), all MPMH MFIs have the same thickness. As discussed in Section 3.2, given identical thickness, the compliance of an MFI decreases as the footprint scales down. As shown in Table 7, the compliance of MFIs on a 50 μm pitch is smaller than MFIs on a 150 μm pitch. Reducing the thickness can increase

the compliance of low-profile MFIs, which has been verified by FEM simulation in Section 3.2. However, the large-profile MFIs might become too compliant to provide sufficient contact force. Therefore, MFI thickness needs to be optimized to obtain a tradeoff among all MFI designs.

Table 7: Mechanical properties of MPMH MFIs obtained by indentation measurements

In-line Pitch (μm)	Force (mN)	Indentation depth (μm)	Calculated compliance (mm/N)
150	7.5	50	6.67
80	9.6	30	3.12
60	9.3	15	1.61
50	8.5	7	0.82

5.4.2 Electrical Characterization of MPMH MFIs

The electrical characterization of MPMH MFIs is performed using a four-point resistance measurement as described in Section 2.4.2. The measured results are summarized in Table 8. Unlike the scaling trends reported in Section 2.4.2, the resistance decreases as the footprint scales down. This is believed to be caused by the simplified MFI design and reduced effective length of the low-profile MFIs.

Table 8: Electrical resistance of MPMH MFIs obtained by four-point resistance measurements

In-line Pitch(μm)	Resistance (mΩ)	Standard deviation (mΩ)
150	128.6	2.6
80	69.5	3.4
60	54.3	3.7
50	37.6	4.1

5.5 Conclusion

In this chapter, MPMH MFIs are reported to address a number of potential applications. As the cornerstone to the demonstration of MPMH MFIs, the multi-height dome process is realized by using double-lithography and double-reflow processes. Compared to the brute-force approach, the process complexity is significantly reduced. Next, multi-pitch MFIs are patterned and electroplated on the substrate with multi-height domes. Following MFI releasing, MPMH MFIs are demonstrated with up to 40 μm height variation for a pitch range of 150 μm to 50 μm. Lastly, mechanical microindentation testing and four-point resistance measurements of the MPMH MFIs are performed for initial mechanical and electrical characterization.

CHAPTER 6

HETEROGENEOUS SYSTEM I: MFIs ASSISTED INTERPOSER STACKING

6.1 Introduction

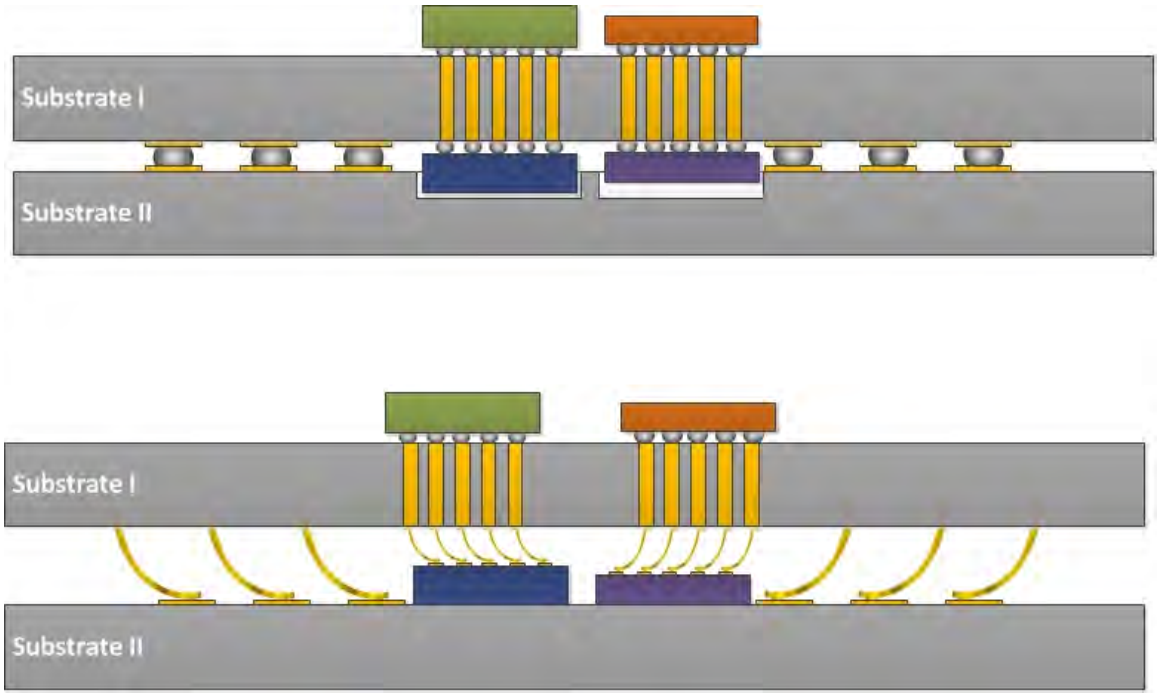
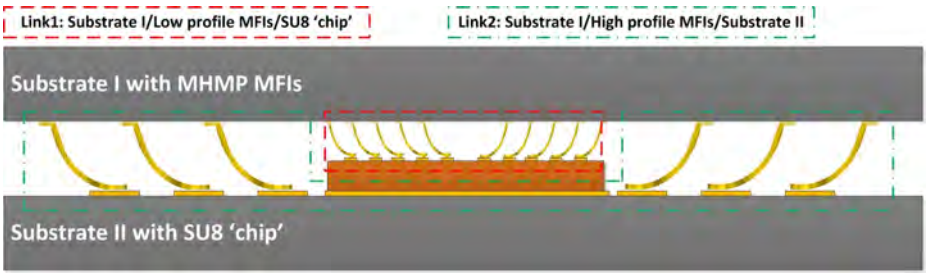
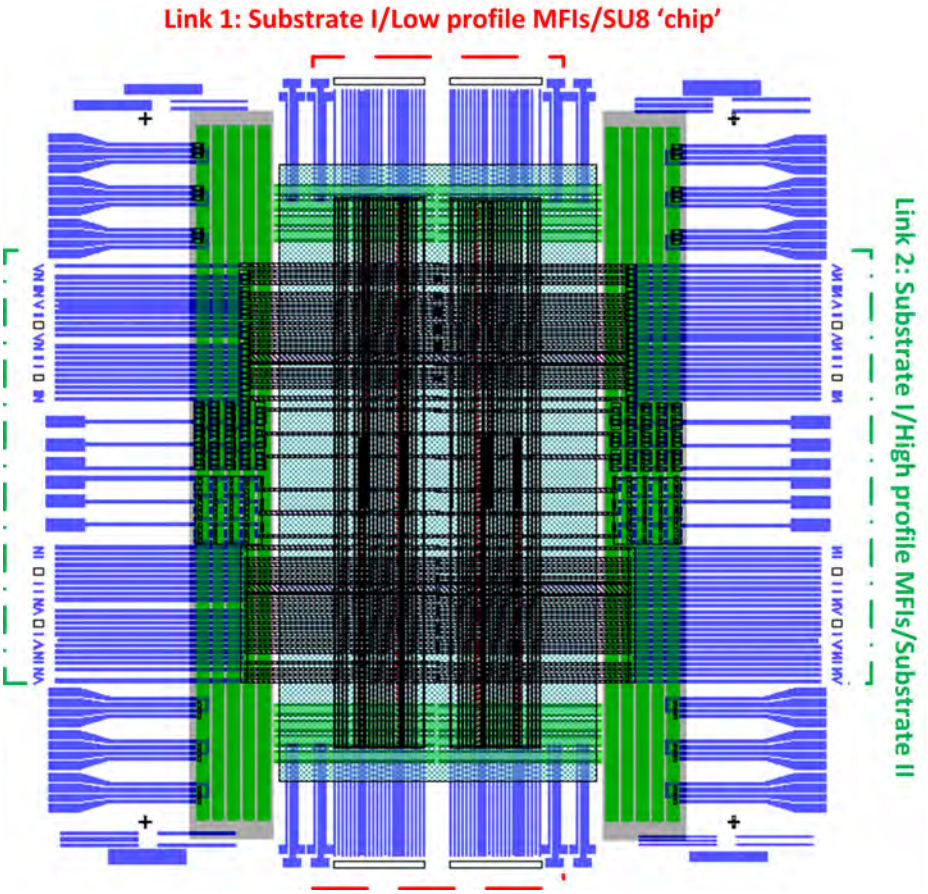


Figure 70: Schematic of 3D interposer stacking using MPMH MFIs.

The MPMH MFIs developed in Chapter 5 are utilized in this chapter to realize a novel high-performance heterogeneous system using interposer stacking, as shown in Figure 70 (bottom). Compared to traditional double-sided interposer based integration (Figure 70 (top)) [68]–[70], the benefits of 3D interposer stacking are: 1) As discussed in Chapter 1, system level testability enabled by rematable MPMH MFIs may improve assembly yield and reduce system cost; 2) Packaging cavities are circumvented, which saves silicon area, reduces the interconnection length, and increases



(a)



(b)

Figure 71: Experimental test bed of 3D interposer stacking using MPMH MFIs.

the mechanical robustness of the bottom interposer.

A simplified interposer stacking test bed, as shown in Figure 71, is demonstrated in this chapter as a proof of concept. The reported test bed includes substrate 1, which contains MPMH MFIs, and substrate 2, which contains a 'chip' formed using

SU8 to represent a surface-mount assembled chip. Two types of electrical links are used to verify the electrical continuity:

*L*ink 1: Substrate 1/SU8 chip/substrate 1. Substrate 1 and SU8 chip are connected using low profile MFIs.

*L*ink 2 : Substrate 1/substrate 2/substrate 1. Substrate 1 and substrate 2 are connected using large profile MFIs.

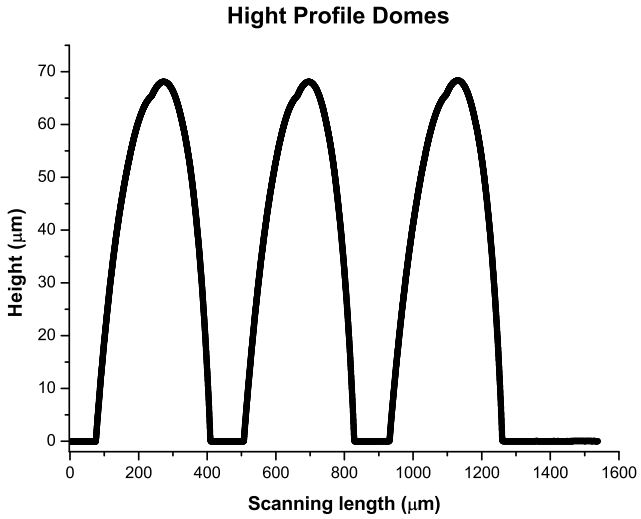
This chapter will first describe the fabrication and assembly of the test bed. In addition, DC measurements are performed to verify that the links formed by the low-profile and large-profile MFIs are functional. Finally, RF probing and RLGC extraction is used to characterize the high-frequency response of the MFIs.

6.2 Fabrication

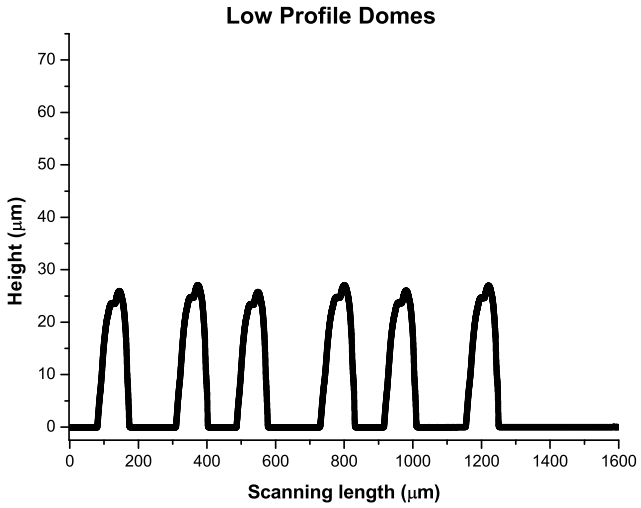
6.2.1 Fabrication of the Substrate with MPMH MFIs

Substrate 1, which contains the MPMH MFIs, is fabricated using the same processes developed in Chapter 5. In order to overcome the thickness of the 'SU8 surface mount chip,' which could represent a single or a 3D stack of chips assumed to be 40 μm in thickness, the heights of the low-profile and high-profile domes are designed as 26 μm and 68 μm, respectively. The height of the multi-height domes is measured using a contact profilometer, as shown in Figure 72.

After MFI electroplating and releasing, the MPMH MFIs are obtained, as shown in Figure 73. Additional structure details are shown in Figure 74. The large-profile MFIs have an in-line pitch of 150 μm; the in-line pitch of the low-profile MFIs used in link 1 is 50 μm. Figure 74 shows that the in-line pitch can be further scaled to 30 μm, which matches the pitch of the most dense microbumps array used for die-interposer interconnection today. Following electroless gold passivation, the substrate with MPMH MFIs is ready for assembly, as shown in Figure 75.



(a)



(b)

Figure 72: Experimental test bed of 3D interposer stacking using MPMH MFIs.

6.2.2 Fabrication of the Substrate with SU8 'chip'

Substrate 2, which contains the asembled SU8 chip, represents an interposer with assembled chips and is fabricated as shown in Figure 76. First, the traces to interconnect the large MFIs in link 2 are fabricated using a lift-off process. Next, 40 μm

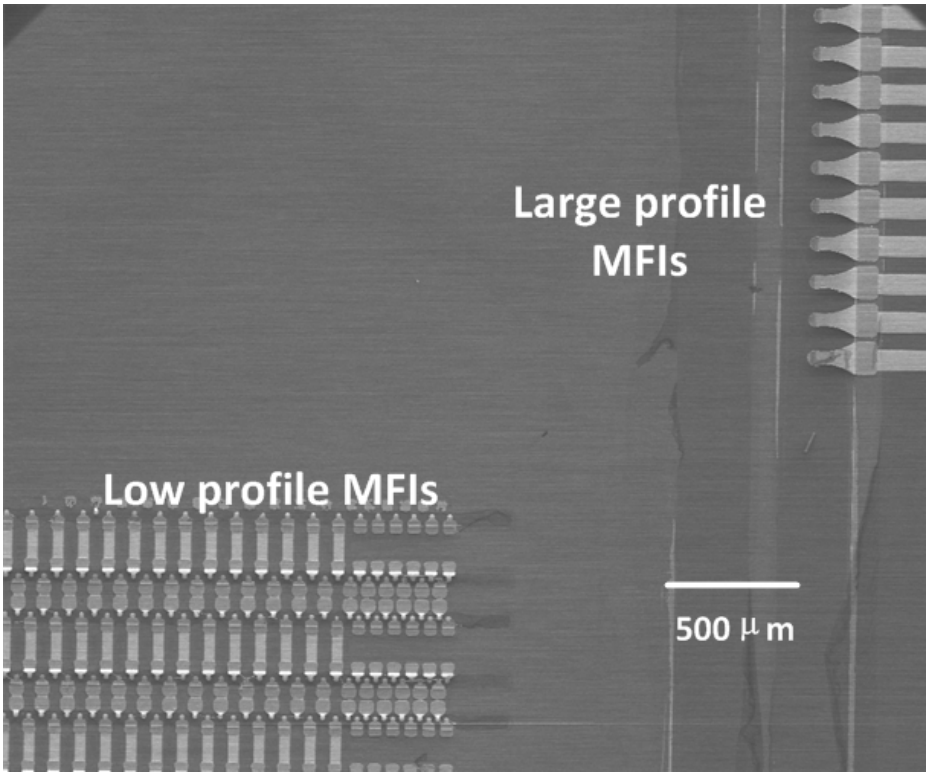


Figure 73: Overview of the MPMH MFIs used for 3D interposer stacking.

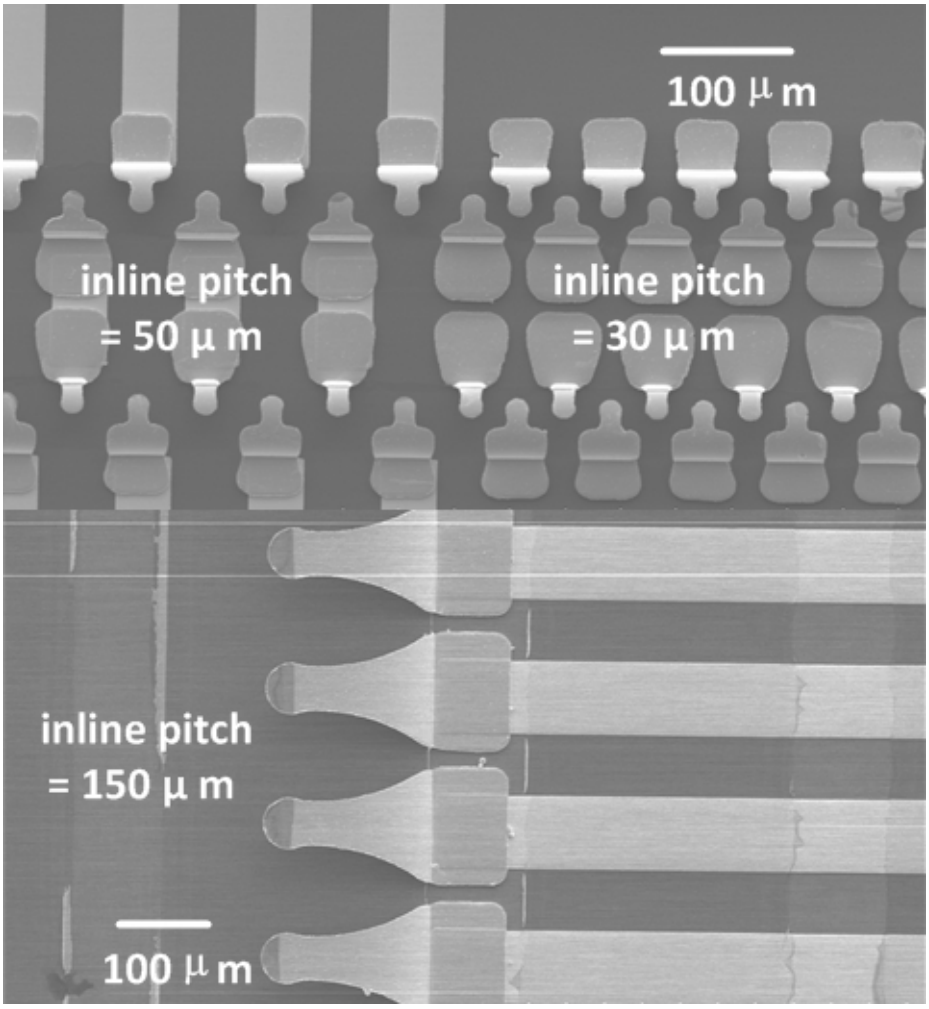


Figure 74: Details of the MPMH MFIs used for 3D interposer stacking.

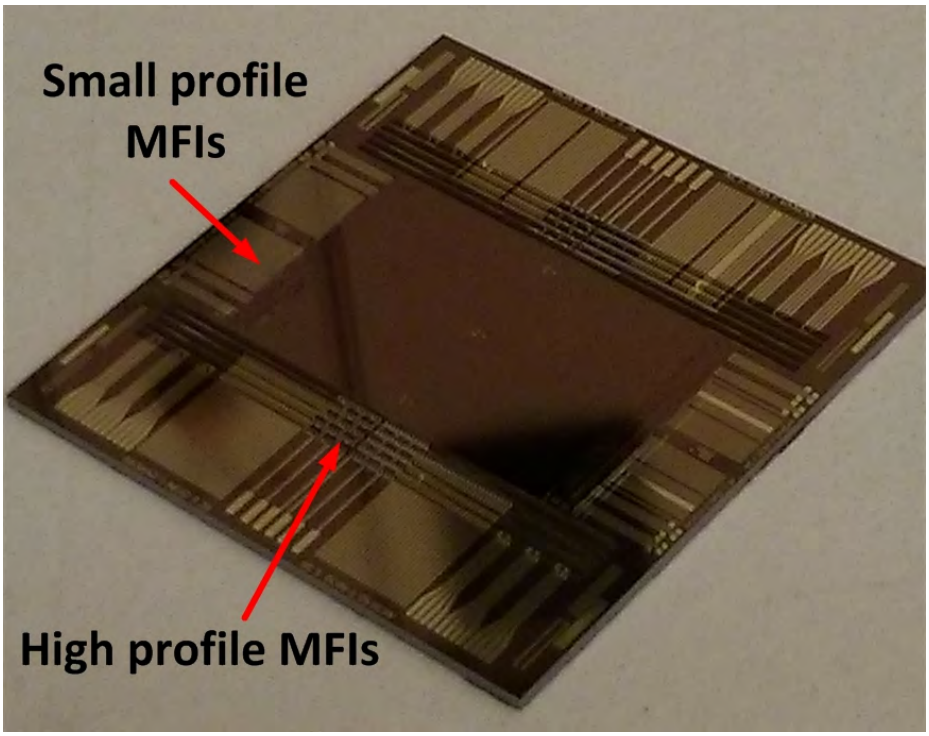


Figure 75: Optical image of the chip with multi-pitch multi-height MFIs.

thick SU8 photoresist is spin-coated on the substrate. Following SU8 exposure, the wafer is sputtered with a seed layer (Ti/Cu/Ti) without performing SU8 development. Next, the traces on top of of the SU8 chip are deposited using Cu electroplating and then passivated by a sputtered gold layer. Finally, the electroplating mold and seed layer are removed, and the unexposed SU8 is cleaned using an ultrasonic assisted development. The resulting fabricated substrate is shown in Figure 77.

Because the footprint of the SU8 chip is fairly large (16mm $\times$ 8mm), the most challenging issue in the SU8 chip fabrication is the SU8 layer delamination caused by the large inner thermal stress. Three approaches are utilized to eliminate delamination: 1) gradually baking and cooling of the SU8 at pre- and post-bake; 2) SU8 development is performed at the end of the process (after carefully cooling the wafer following the last thermal step); and 3) stress releasing trenches are added at the edge of the SU8 chip, as shown in Figure 77(b).

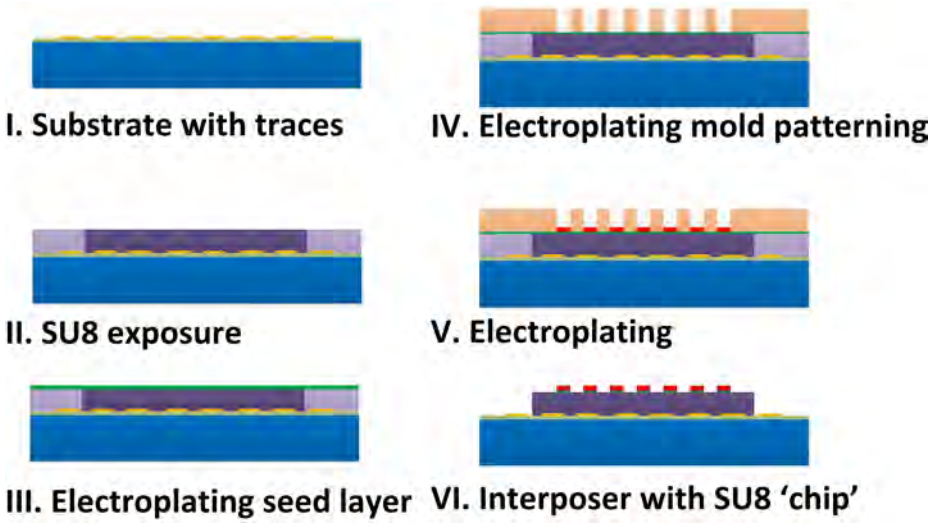


Figure 76: Fabrication of substrate with SU8 chip.

6.3 System Assembly

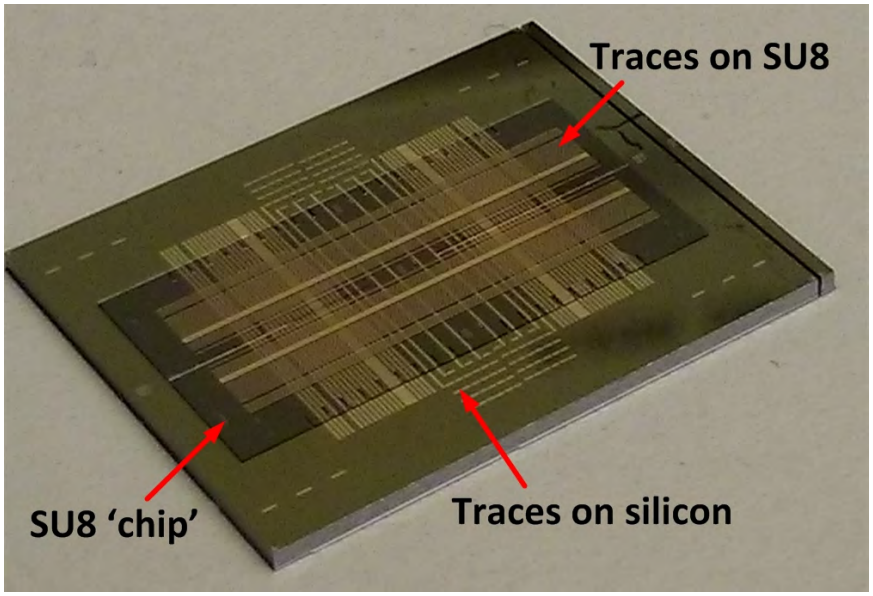
The two fabricated substrates, as shown in Figure 75 and Figure 77, are picked up and aligned using a flip-chip bonder. Epoxy glue dotlets are applied on the four edges to complete the assembly of the test bed. The final assembled test bed is 2.08 cm × 2.12 cm, as shown in Figure 78. X-ray images (Figure 79) are taken to ensure that the alignment is correct and the links are void-free.

6.4 Experimental Results

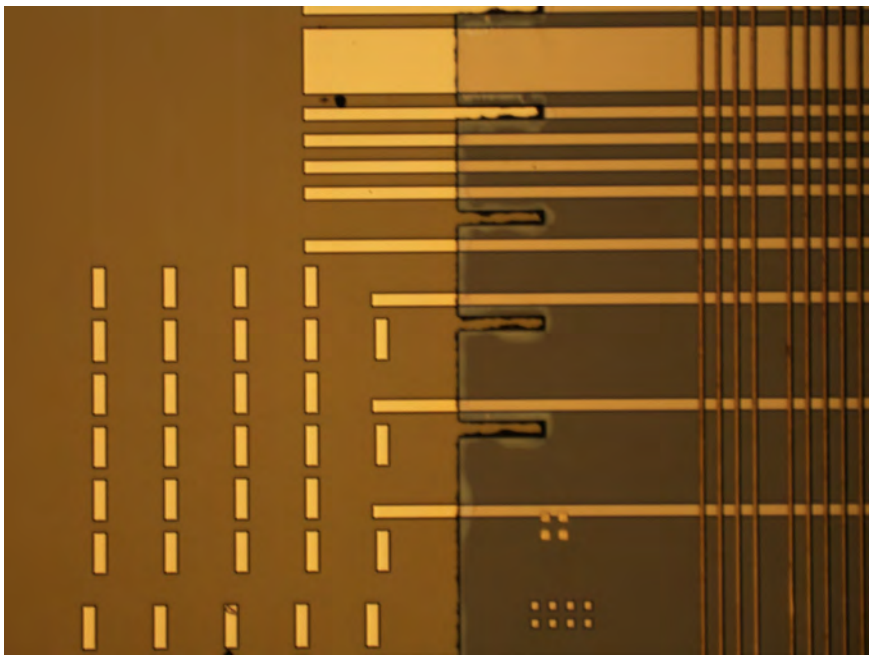
6.4.1 DC Characterization

As shown in Figure 80, two large-profile MFI designs are adopted in the 3D interposer stacking test bed: MFIs with an enhanced mechanical performance (mMFI) and MFIs with an enhanced electrical performance (eMFI). mMFI is the design described in Chapters 2-4, which has a large vertical range of motion. eMFI has a simpler geometry and a shorter effective length, which yields smaller electrical resistance and inductance.

The electrical continuities of link 1 and 2 are verified by DC measurements. The test structure dimensions and measured results are summarized in Table 9.



(a)



(b)

Figure 77: Optical image of the substrate with SU8 chip.

6.4.2 RF Characterization

6.4.2.1 RF Probing

A network analyzer interfaced to an RF probing station is used to investigate the MFI RF properties up to 50 GHz. Three MFIs are probed by a pair of GSG RF probes,

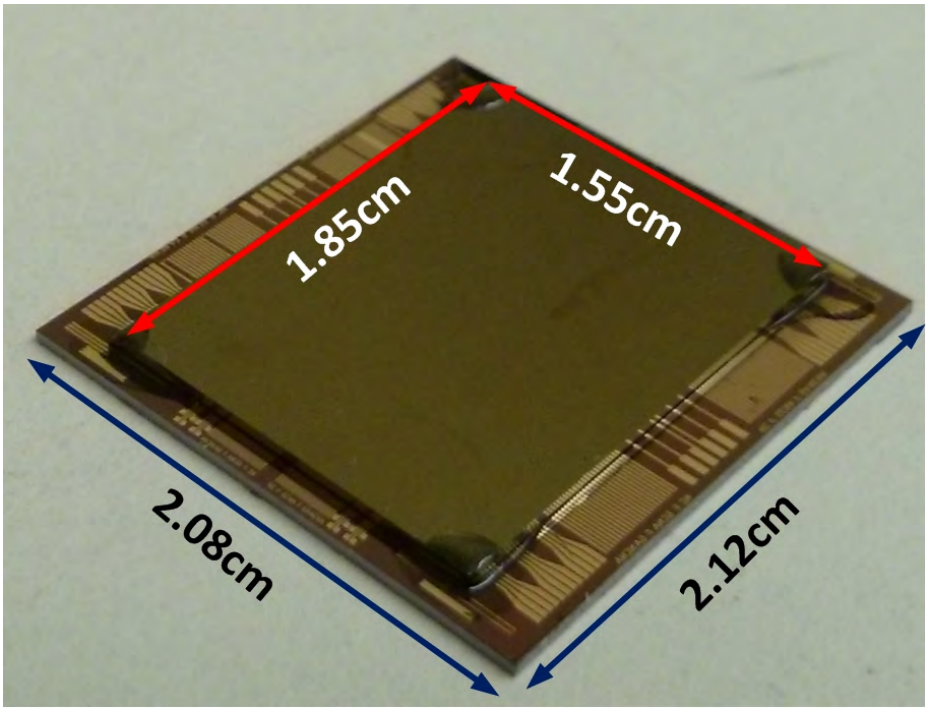


Figure 78: Assembled test bed for 3D interposer stacking demonstration.

Table 9: DC measurements of interposer stacking test bed

		High profile MFIs		Low profile MFIs
		mMFI	eMFI	
Geometry	Trace width (μm)	100	100	40
	Pitch (μm)	150	150	100
	Height (μm)	68	68	26
DC Measurements	Single (mΩ)	183.6	162.8	53
	Link A (Ω) (2 MFIs)	4.232	4.179	9.944
	Link B (Ω) (38 MFIs)	9.737	8.853	N/A

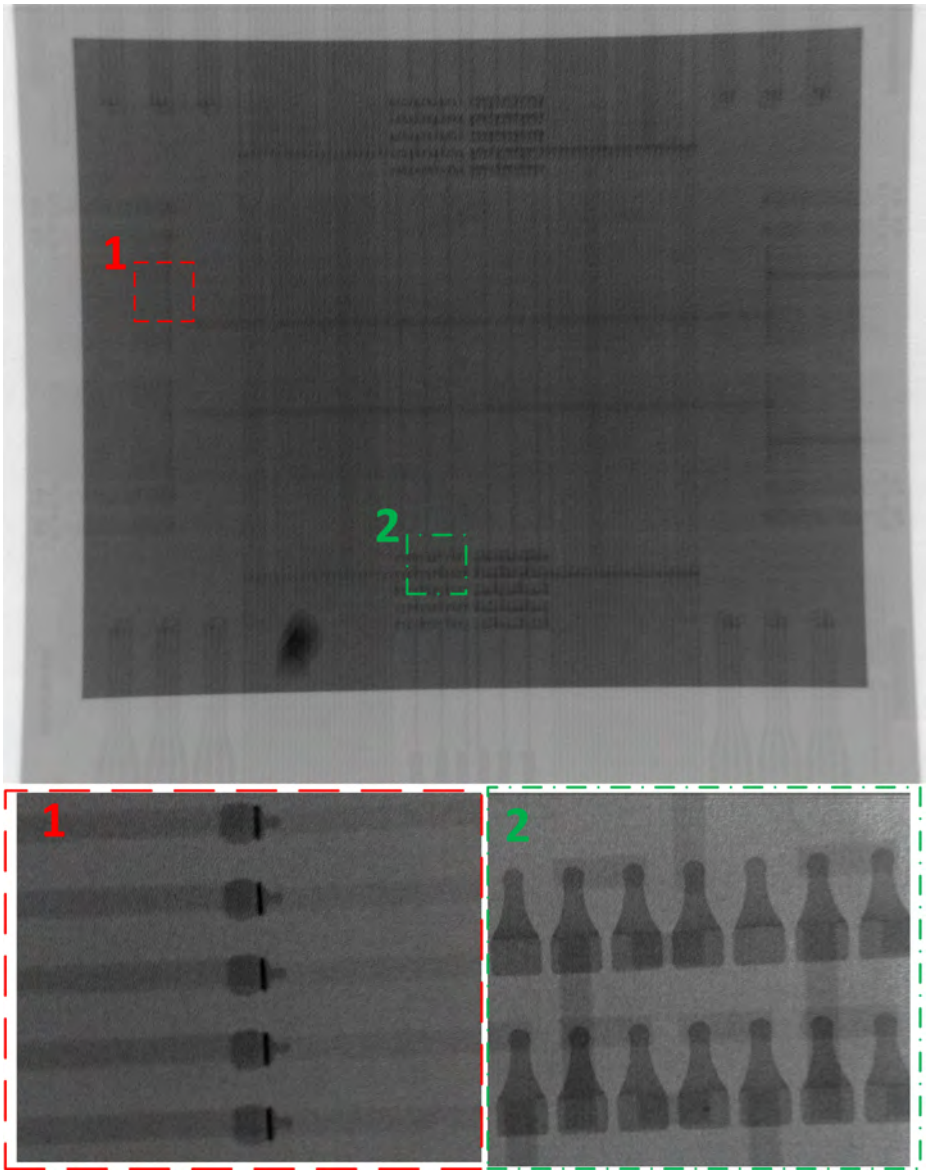


Figure 79: X-ray image of assembled test bed for 3D interposer stacking demonstration.

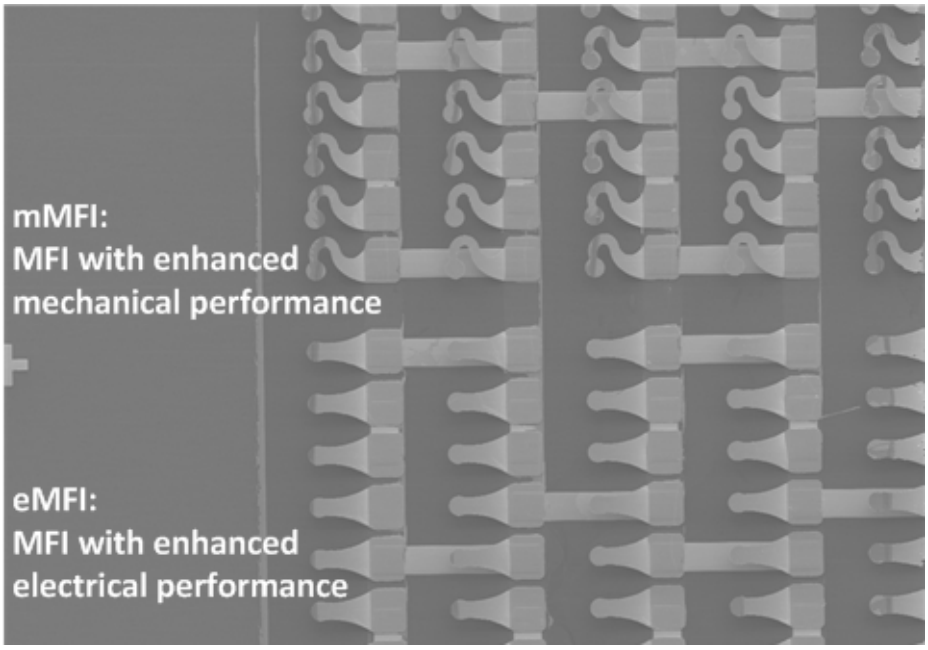


Figure 80: Two MFI designs: eMFIs and mMFIs.

as shown in Figure 81. The RF probing results plotted in Figure 82 show that the insertion loss (S21) of the mMFI is 1.05dB at 50 GHz, which matches the simulation results from HFSS. The relative permeability used in the HFSS simulation is 1 [71].

6.4.2.2 Rematability Test

RF probing was also performed on the eMFI and mMFI as a function of deformation. The measurements were made for four conditions (or stages): initial contact, while the MFI is fully deformed, following MFI recovery to its initial height, and after being indented a total of 10 times. The measured results are shown in Figure 83 and Figure 84. As shown in Figure 83, the S21 and S11 plots for the mMFI for the four conditions show that the mMFI electrical properties are preserved following deformation. The insertion loss (S21) of the mMFI while under full deformation is slightly higher than the other three cases, which is believed to be due to the modest sliding of the RF probes on the mMFI. As shown in Figrue 84, the eMFI has a lower insertion loss (0.73 dB at 50 GHz) relative to the mMFI. eMFI can recover its original shape as

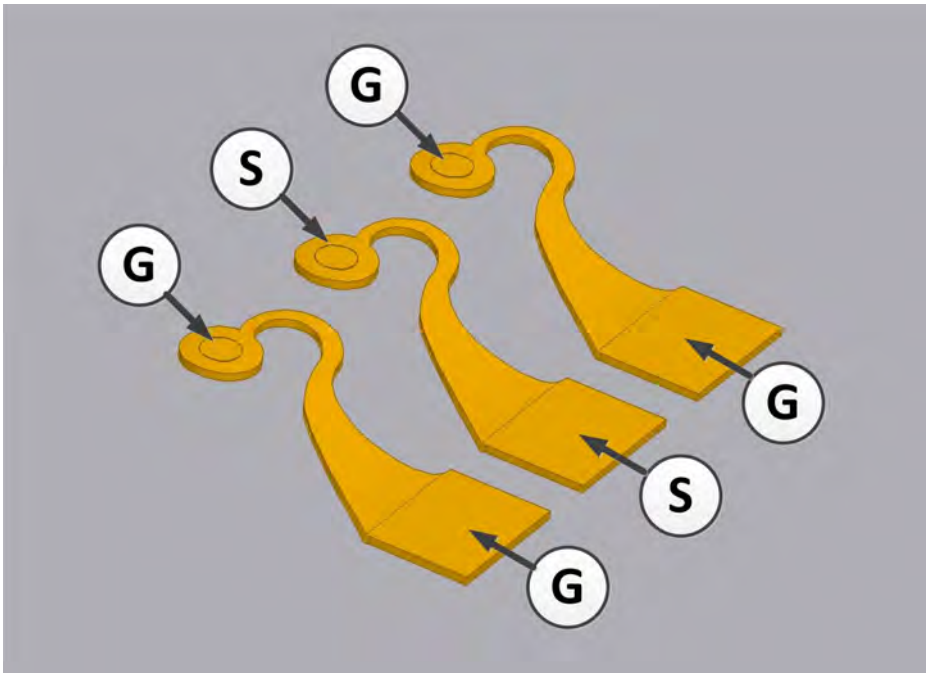


Figure 81: Schematic of RF probing performed on MFIs.

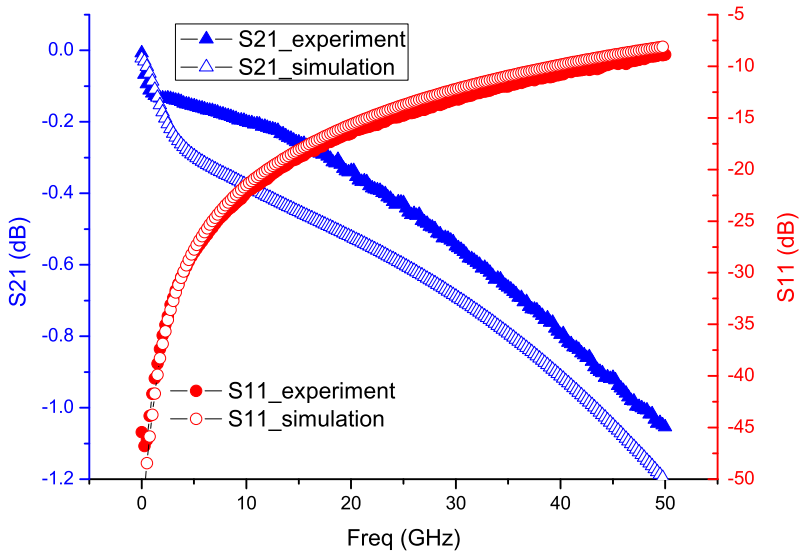


Figure 82: RF probing results of mMFI.

well after first probing, which is verified by the fact that the initial contact curve is overlapped with the recovered curve. However, the insertion loss (S21) increases after 10 deformations, which potentially indicates that the rematability of eMFI is not as robust as that of the mMFI.

6.4.2.3 RF Characterization: RLGC Extraction

In order to extract the RLGC (resistance, inductance, conductance, and capacitance) properties of the probed mMFIs and eMFIs, the following equations, Eq.1-4, were used. The extracted RLGC parameters of the mMFI and eMFI are reported in Figure 85, 86 and 87. The extracted values at 5, 10, 25, and 50 GHz are summarized in Table 11 and Table 10 as well.

The extracted parameters of the mMFIs and eMFIs show that there is a negligible difference between the mMFIs and eMFIs in terms of resistance, conductance and capacitance (Figure 85, 86). This is because these two designs have similar dimensions. The main difference is in the inductance, L, which causes insertion loss variation between the mMFIs and eMFIs, as shown in Figure 87. The inductance L is affected more by the geometry. Hence, eMFI has a better RF performance than the mMFI, which has a coil-like design.

$$R = \mathrm{Re}(Z_{11} + Z_{22} - Z_{12} - Z_{21}) \tag{1}$$

$$L = \frac{\mathrm{Im}(Z_{11} + Z_{22} - Z_{12} - Z_{21})}{\omega} \tag{2}$$

$$G = \mathrm{Re}(Y_{11} + Y_{22} + Y_{12} + Y_{21}) \tag{3}$$

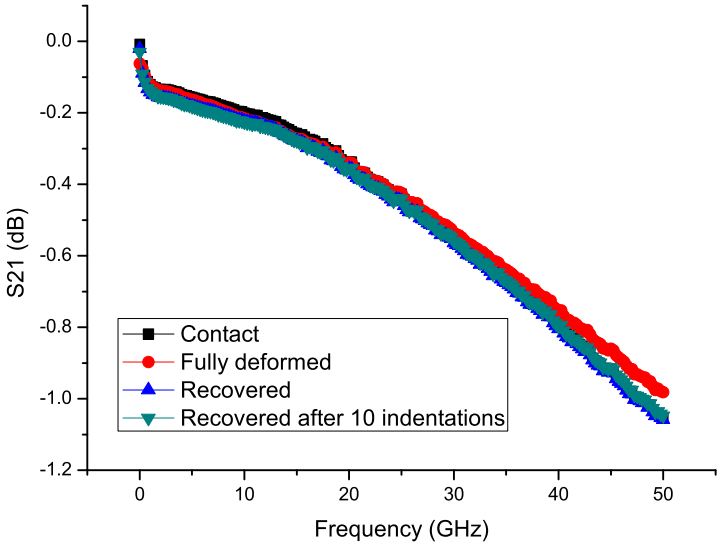
$$C = \frac{\mathrm{Im}(Y_{11} + Y_{22} + Y_{12} + Y_{21})}{\omega} \tag{4}$$

Table 10: Extracted RLGC of mMFI

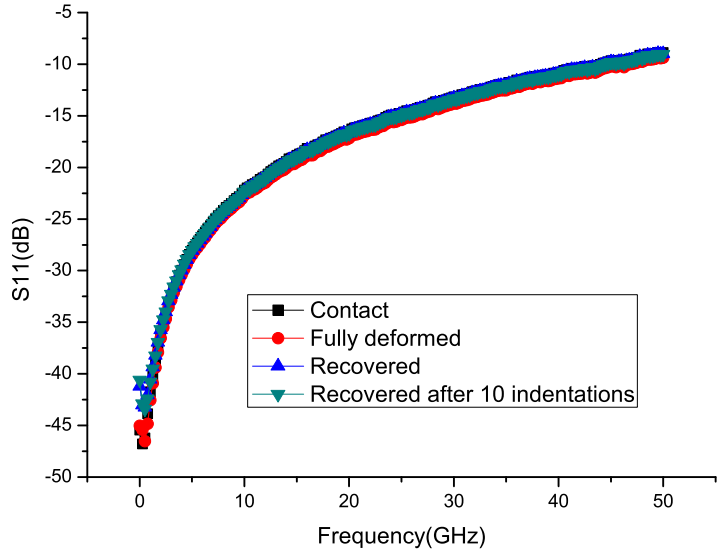
Measurement	Parameters	5 GHz	10 GHz	25 GHz	50 GHz
Initial contact	R (Ω)	1.08	1.19	1.76	1.69
	L (nH)	0.17	0.17	0.16	0.15
	G(mS)	0.25	0.32	0.52	0.87
	C (fF)	17.00	15.90	15.60	12.80
Fully Deformed	R (Ω)	1.14	1.36	1.90	1.82
	L (nH)	0.17	0.16	0.16	0.15
	G(mS)	0.27	0.34	0.55	0.91
	C (fF)	19.00	17.80	17.50	14.50
After 10 indentation	R (Ω)	1.37	1.50	1.99	1.87
	L (nH)	0.17	0.16	0.16	0.14
	G(mS)	0.25	0.32	0.52	0.87
	C (fF)	17.00	15.90	15.70	12.80

Table 11: Extracted RLGC of eMFI

Measure-ment	Para-meters	5 GHz	10 GHz	25 GHz	50 GHz
Initial contact	R (Ω)	1.17	1.26	1.55	1.21
	L (nH)	0.13	0.13	0.12	0.11
	G(mS)	0.28	0.37	0.59	0.94
	C (fF)	17.80	16.14	15.56	12.70
Fully Deformed	R (Ω)	0.77	0.85	1.09	0.78
	L (nH)	0.11	0.11	0.11	0.11
	G(mS)	0.30	0.40	0.63	0.99
	C (fF)	20.36	18.49	17.90	14.77
After 10 indentation	R (Ω)	3.17	3.28	3.36	2.71
	L (nH)	0.12	0.12	0.11	0.11
	G(mS)	0.31	0.40	0.62	0.98
	C (fF)	18.07	16.26	15.70	12.74



(a)

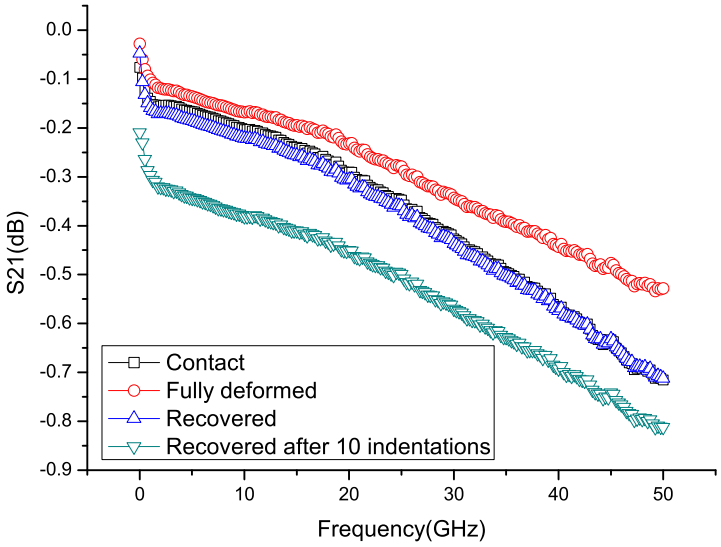


(b)

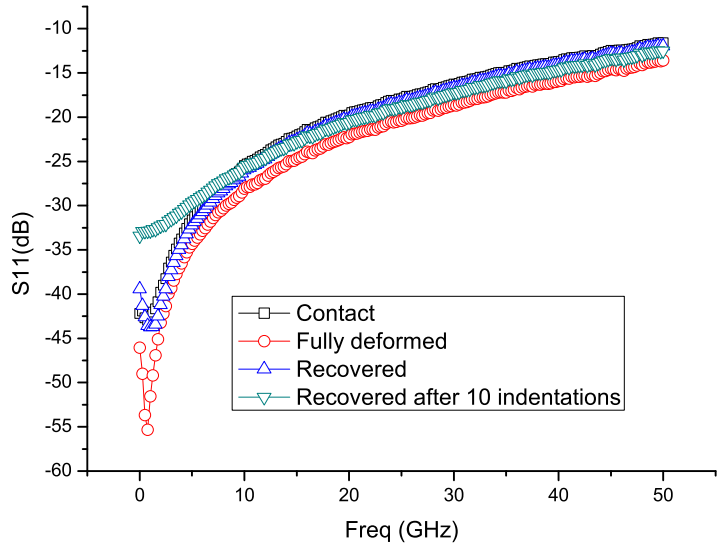
Figure 83: RF measurement of MFIs with enhanced mechanical performance (mMFIs).

6.5 Conclusion

A rematable 3D interposer stacking system is proposed using MPMH MFIs in this chapter. A substrate with MPMH MFIs is flip-chip bonded onto a substrate with



(a)



(b)

Figure 84: RF measurement of MFIs with enhanced electrical performance (eMFIs).

an SU8 chip for proof-of-concept. Electrical links interconnecting the two substrates and substrate-to-SU8 chip are realized using large-profile and low-profile MFIs, respectively. DC electrical measurements have been performed on the links to verify

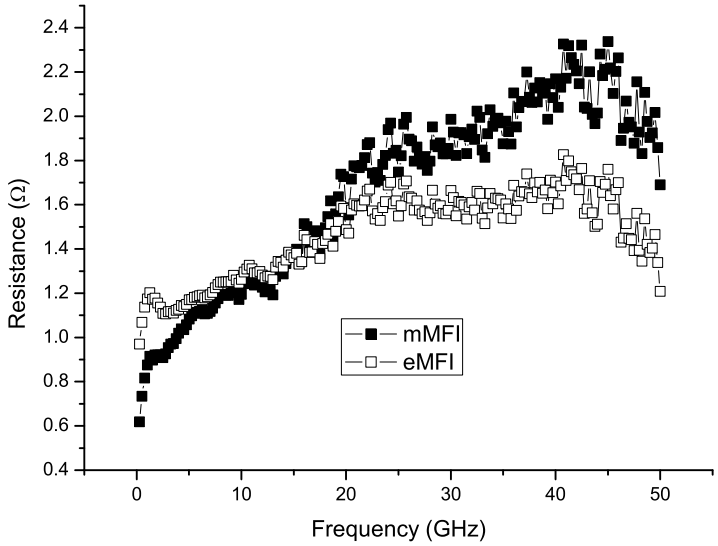


Figure 85: Extracted resistance comparison: mMFI vs. eMFI.

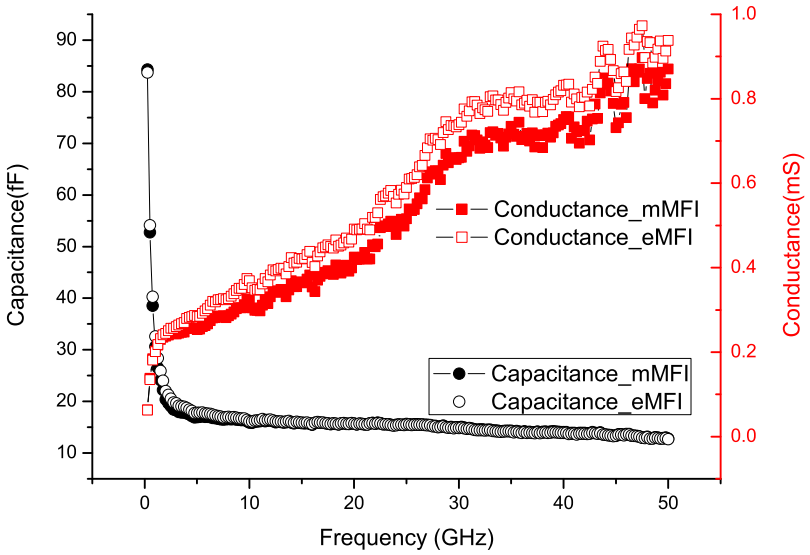


Figure 86: Extracted capacitance and conductance comparison: mMFI vs. eMFI.

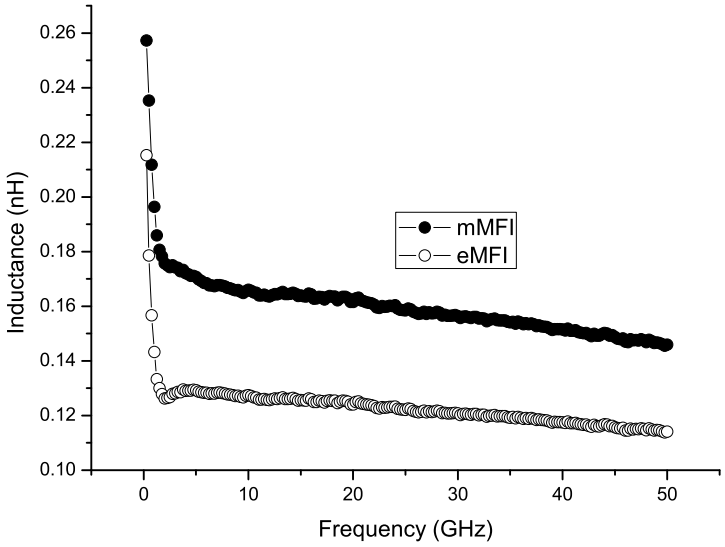


Figure 87: Extracted inductance comparison: mMFI vs. eMFI.

the electrical continuity. In addition, RF probing and RLGC extraction are used to investigate the MFI performance at high frequencies.

CHAPTER 7

HETEROGENEOUS SYSTEM II: BRIDGED MULTI-INTERPOSER SYSTEM

7.1 Introduction

Silicon interposer based 2.5D integration has received significant interest because it can provide a high-bandwidth and low-energy interconnect platform for heterogeneous systems. However, for state-of-the-art 2.5D integrated systems, the high-performance interposer interconnections are only available for chips mounted on a single interposer. Given that the size of interposers is limited by the reticle size as well as cost, there exists a limit on the number of chips that can be integrated. Therefore, an innovative interconnection platform between interposers is needed to extend interconnect benefits over a large-scale system.

As shown in Figure 88, we propose a novel vision to realize large-scale bridged

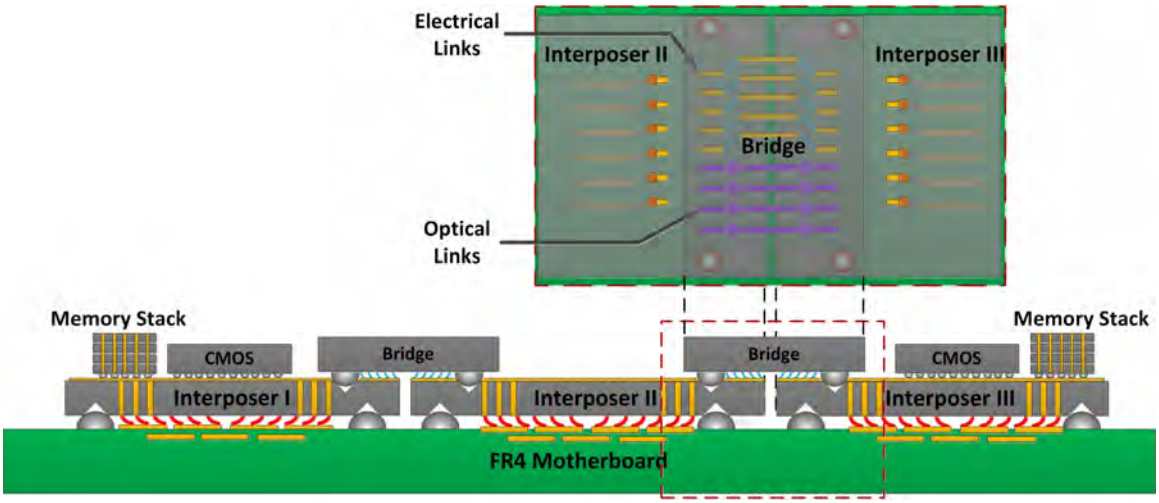


Figure 88: Bridged multi-interposer system.

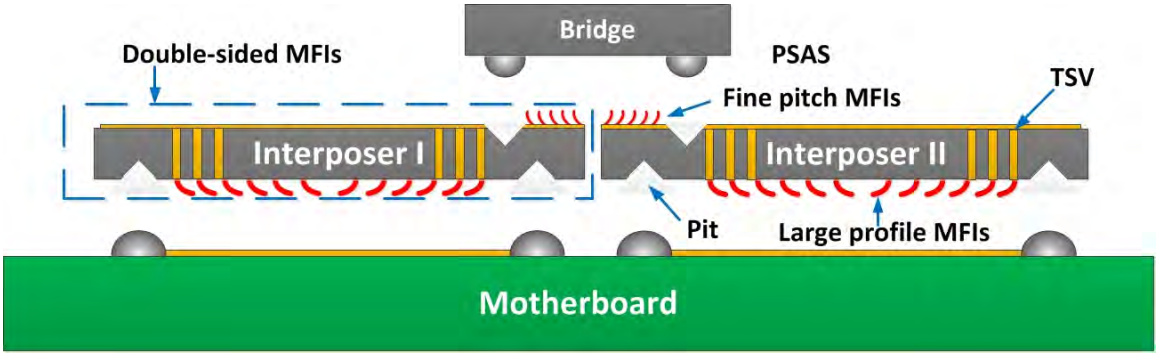


Figure 89: Key technologies to enable bridged multi-interposer system.

multi-interposer systems [72], [73]. Interposer tiles, which are essentially silicon interposers with alignment structures, can possibly be directly mounted on the motherboard (or package for some applications). The adjacent interposer tiles are interconnected by silicon bridges, which are silicon chips with MFIs and corresponding routing designs. The tile-to-motherboard and bridge-to-tile electrical interconnects are enabled by MFIs with various pitches and heights. Interposer tiles, silicon bridges and the motherboard (or package) are self-aligned with each other using PSAS and inverted pyramid pit pairs. Our proposed concept is an extension of the macro-chip concept demonstrated in [27]–[29].

Several of the key enabling technologies for the envisioned system shown in Figure 88 will be first described in this chapter. Based on the demonstrated key technologies, a proof-of-concept demonstration is reported as well.

7.2 Key Enabling Technologies

As shown in Figure 89, the key enabling technologies described in this section for the envisioned bridged multi-interposer system are: 1) positive self-alignment structures (PSAS) and pit, 2) MFI/TSV integration and 3) double-sided MFIs.

7.2.1 PSAS and Pit Self-alignment

Positive self-alignment structures (PSAS) are reflowed photoresist dome-like structures, as shown in Figure 90 (a). Depending on the initial heights of the cylinder shaped structures that are reflowed, truncated spheres or semi-spheres can be formed. Besides the silicon substrate, PSAS are successfully formed on the organic substrate as well (Figure 90 (b)), which enables silicon/organic substrate self-alignment using PSAS/Pit structures.

The shape of the PSAS and the pit structures determine the final relative position of the two substrates. Pit structures have been widely used in MEMS, and the resulting shape can be predicted accurately. Therefore, in this section, only the shape of the PSAS is determined. The shape of the PSAS is measured using an Olympus LEXT 3D Material Confocal Microscope, which captures the profile of 3D structures. The captured profile of the PSAS is shown in Figure 91. The analysis of the captured data shows that the surface of PSAS is radially symmetric and the profile through the center fits a circular segment.

Inverted pyramid pits can be fabricated in <100> silicon substrates using a two-step process. First, square shaped openings are created on a silicon wafer coated with a silicon nitride layer. Next,the wafer is submerged in a temperature and concentration controlled KOH or TMAH bath. The process forms a negative trench with sidewalls at an angle of 54.7°. This is a commonly used process in MEMS, and it is a highly controllable process. The etched pit is shown in Figure 90 (c).

Figure 92 shows a IR image of an assembled PSAS/Pit pair. With the PSAS/Pit self-alignment, position accuracy can be reached both in the lateral and vertical directions. For the envisioned system (Figure 88), lateral alignment accuracy is more critical, and alignment better than 1 μm between the transmit-receive waveguides is required. The lateral alignment accuracy is measured using Vernier patterns, as shown in Figure 92. For proximity interconnection, such as capacitive coupling [74],

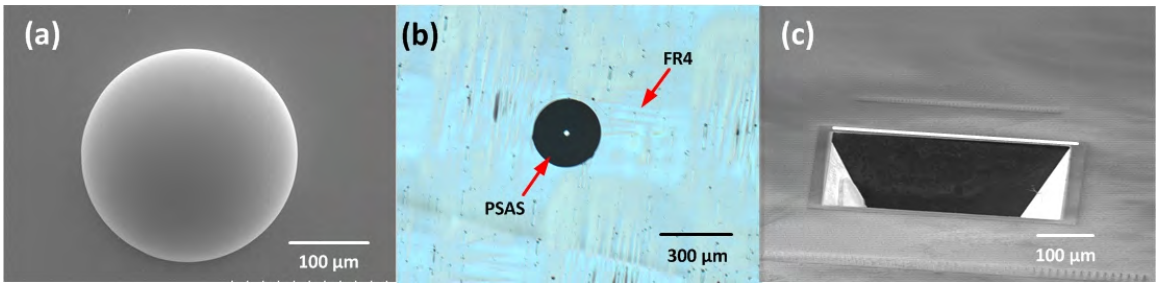


Figure 90: Positive self-alignment structures (PSAS) and pit.

vertical alignment accuracy, i.e. the gap between two chips, is very critical. It has been shown that 10 μm or less vertical separation between two capacitive couplers is required for high fidelity and low bit-error rate signaling [74]. The assembly gap is estimated by the method described in [67].

7.2.2 Double-sided MFIs

As shown in Figure 88, MFIs are needed on both sides of the silicon interposer tile: large-profile MFIs are formed on the side facing the organic substrate to overcome the large substrate surface variation and silicon/organic substrate CTE mismatch; fine pitch MFIs are formed on the side facing the bridge to realize a large bandwidth off-interposer interconnection. In this chapter, the side facing the bridge is referred to as the "front side" and the side facing to organic substrate is referred to as the "back side."

Figure 93 illustrates the fabrication flow of the double-sided MFIs along with pits. The process begins with the patterning and etching of the pits on both sides. Next, on the front side, fine-pitch MFIs are fabricated; seed layer and dome releasing are not yet performed. Following this, a temporary protection layer is coated on the front side allowing the wafer to be flipped and processed on the front side. Following back side MFI formation and front side protection layer removal, the MFIs are released on both sides simultaneously. Finally, the MFIs on both sides are passivated by electroless gold layer. The large MFIs exhibit a 65 μm vertical gap and are formed on a 150 μm

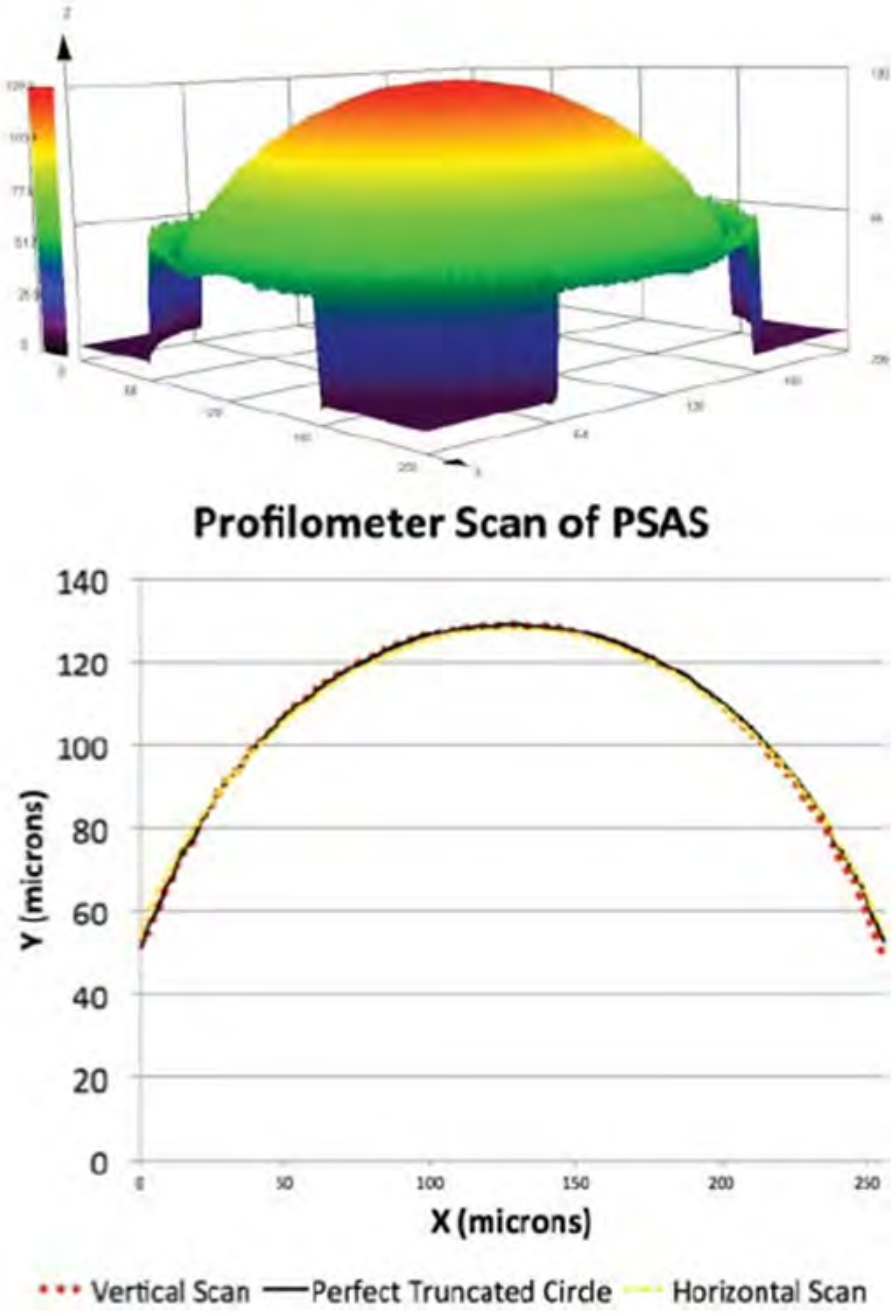


Figure 91: PSAS profile measured by 3D confocal microscope.

pitch, while the front side MFIs are 25 μm tall and are formed on a 50 μm pitch.

Figure 94 shows the co-fabricated pit and MFI array. The pit has 300 μm wide opening, which will be assembled with PSAS on the organic substrate to ensure an

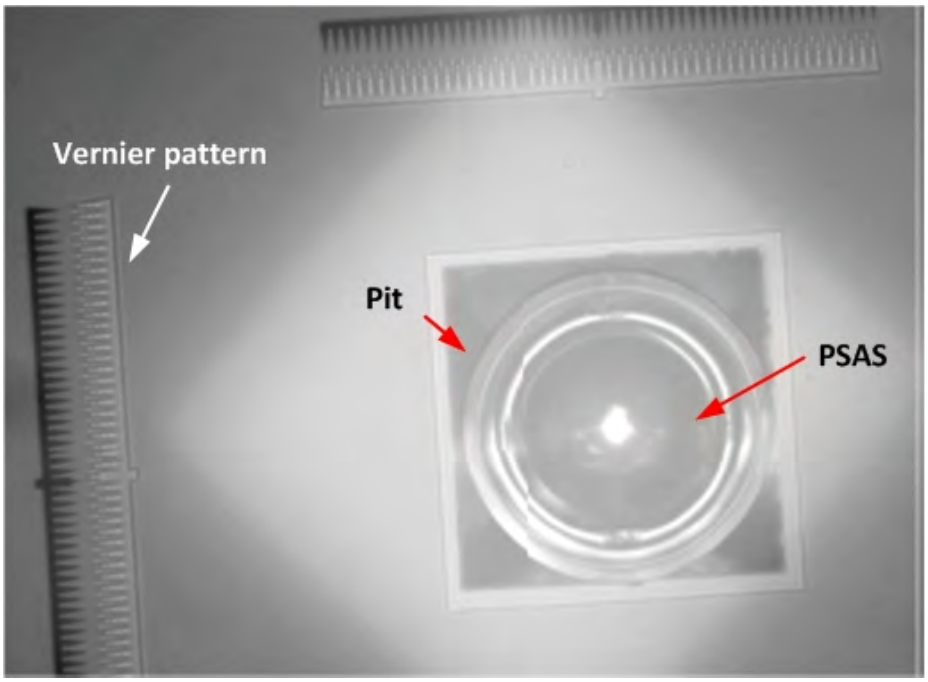


Figure 92: Assembled PSAS and Pit.

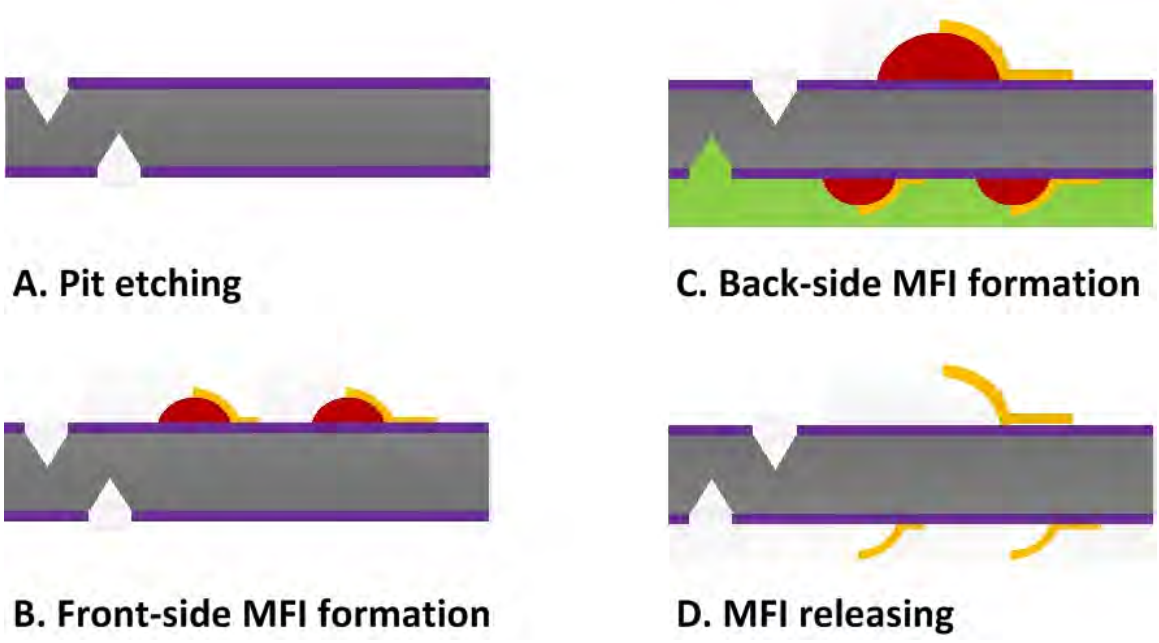


Figure 93: Fabrication of double-sided MFIs.

accurate self-alignment. Figure 95 shows the fabricated double-sided MFIs on silicon interposer. The details of the MFIs on both sides are shown at the bottom.

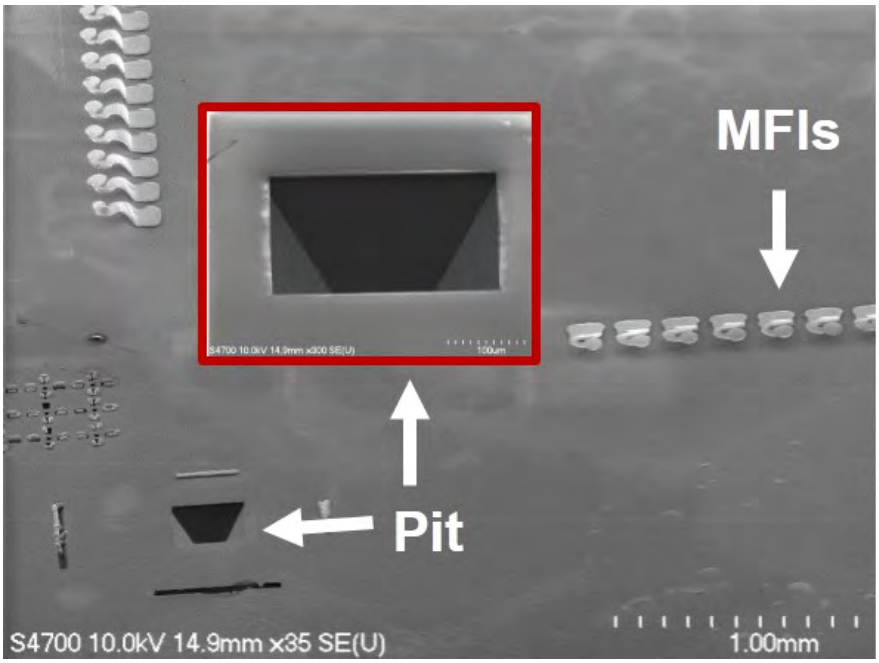


Figure 94: SEM of MFIs and pits .

One reason to integrate MFIs on both sides of the interposer rather than on chip/bridge and organic substrate is that the MFIs on both sides can be released simultaneously, which lowers the fabrication cost and increases the throughput as well.

7.2.3 MFI/TSV Integration

As shown in Figure 88 and Figure 89, TSVs are essential to routing the signal and power between the front and back side of the interposer. In this section, the MFI/TSV co-fabrication is demonstrated as a key enabling technology for our envisioned bridged multi-interposer system.

Figure 96 illustrates the process of MFI/TSV co-fabrication. First, the TSVs are fabricated using the mesh process developed previously [54]. Silicon via etching is performed using an STS ICP, and the mesh etching is performed using a Vision RIE. After silicon dioxide liner deposition, the mesh side of the wafer is pinched-off and the via is filled by Cu electroplating followed by chemical mechanical polishing (CMP) to

remove the over-electroplated Cu. The TSV process concludes with back side routing layer formation. Next, after front side routing layer formation, the MFI process is performed on the wafer with TSVs.

The two key steps in this process are TSV CMP polishing and MFI photoresist electroplating mold formation. A uniform CMP polishing is critical to avoid photoresist bubbling and twisting during sacrificial domes formation. As shown in Figure 97, a well defined MFI pattern transfer is accomplished.

Figure 98 shows the fabricated MFI/TSV array. X-ray images show that the vias are filled with Cu without voids. The dimensions of the fabricated MFI/TSV array

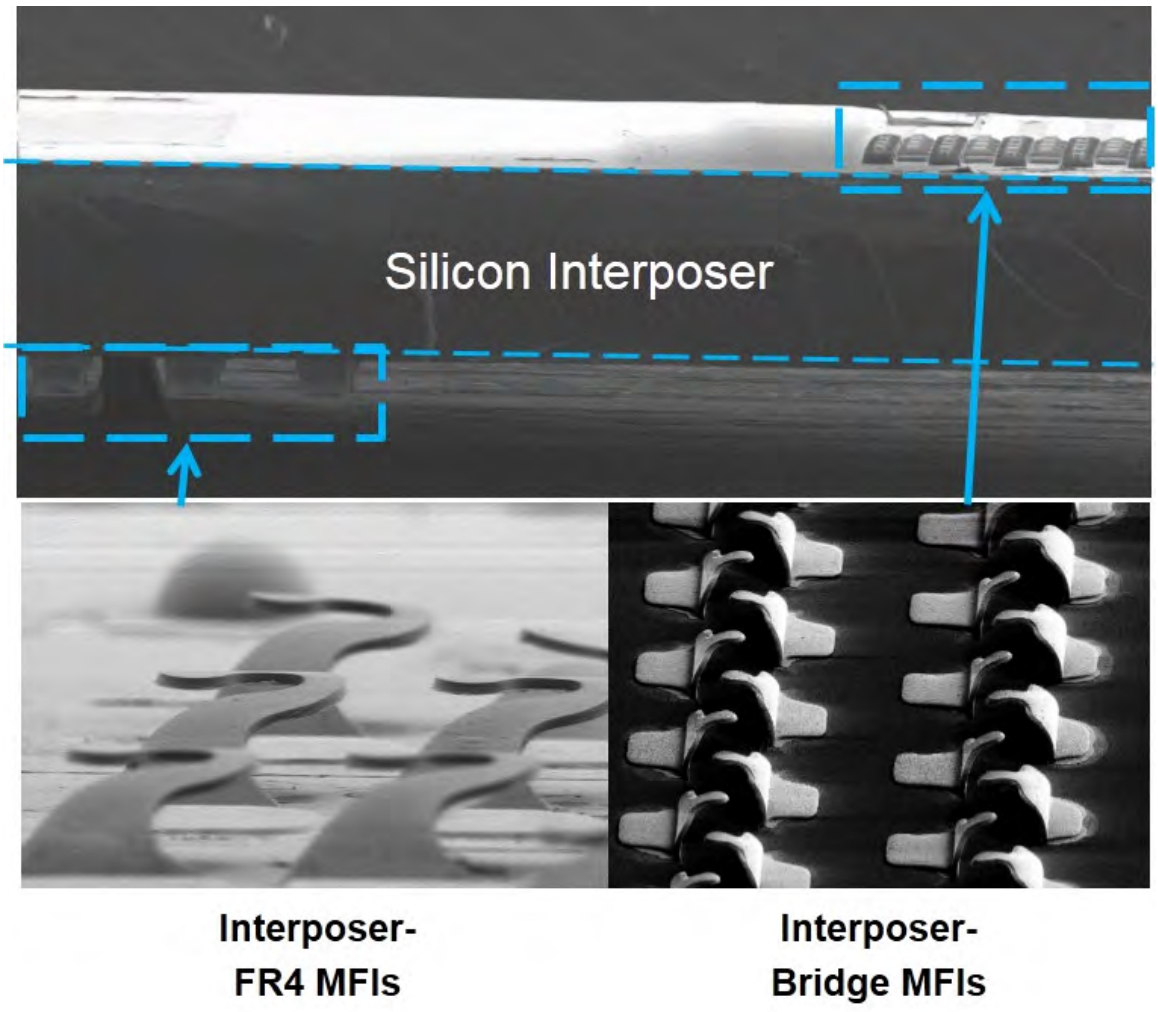


Figure 95: SEM of double-sided MFIs.

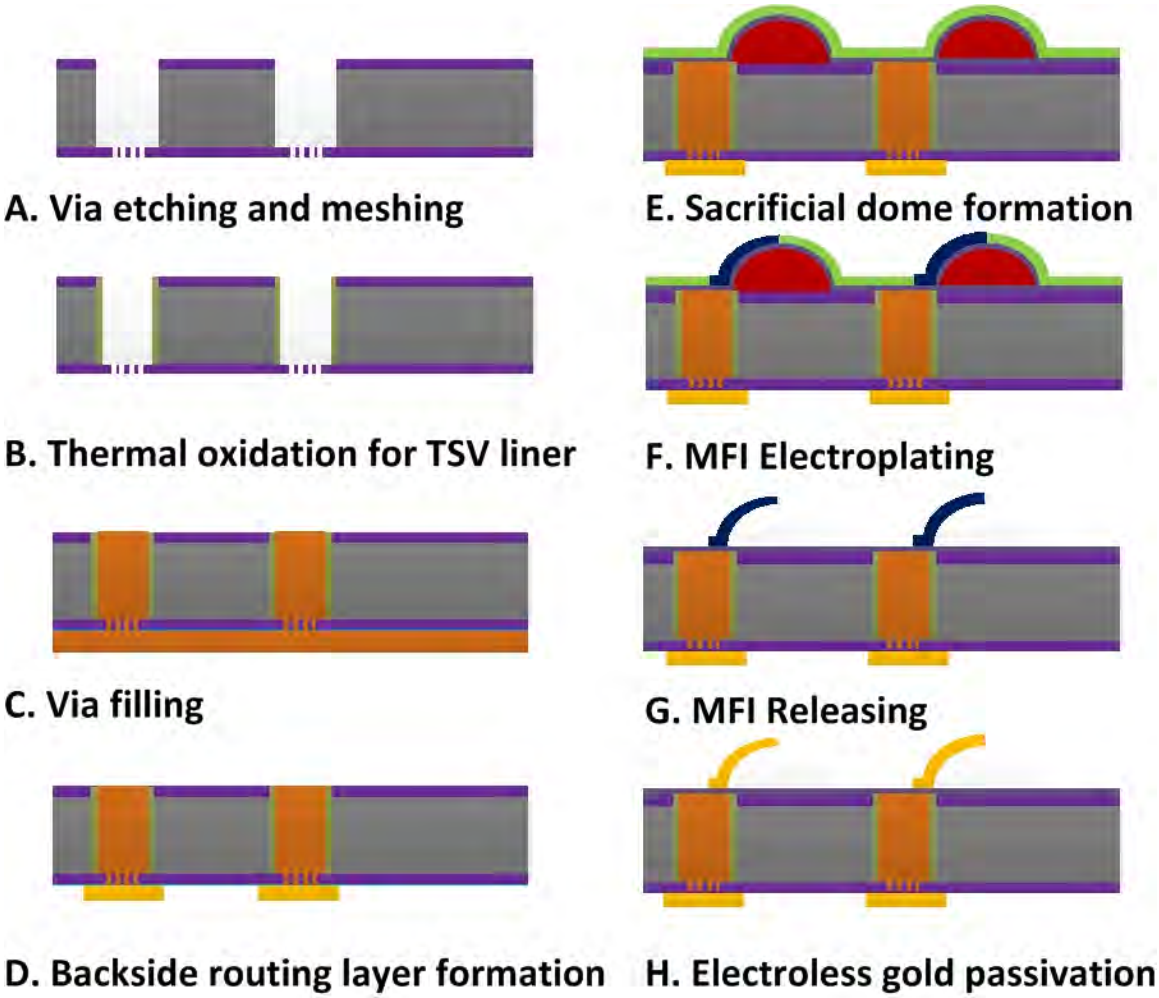


Figure 96: Fabrication of MFI/TSV integration.

are summarized in Table 12.

DC Measurement

As shown in Figure 99, using a flip-chip bonder, a silicon chip with MFIs and TSVs is assembled on an oxide passivated silicon substrate with a gold-coated surface. Using this setup, four-point resistance measurements are performed to measure the resistance of each MFI/TSV pair plus the contact resistance between the MFI and the gold surface. The measured resistance is 76 mΩ, which agrees well with calculated values.

RF Probing

Table 12: Dimensions of TSV/MFI array

	Demension	Value (μm)
TSV	Diameter	50
	Height	300
	Pitch	100
MFI	Vertical height	30
	Thickness	5
	Pitch	100

The RF performance of MFI/TSV structure is investigated using single port RF probing, as shown in Figure 100 (top). The results are plotted in Figure 100 (bottom) as well and matches HFSS simulation.

In order to realize a low-loss link, HFSS simulations with various parameters of the MFI/TSV structure have been performed. Figure 101 shows that the insertion loss increases with the increase of silicon substrate conductance significantly. Similarly, as shown in Figure 102, larger TSV diameter yields higher insertion loss as well. Therefore, TSVs with smaller diameter in high resistivity silicon substrate are preferred for low-loss MFI/TSV application.

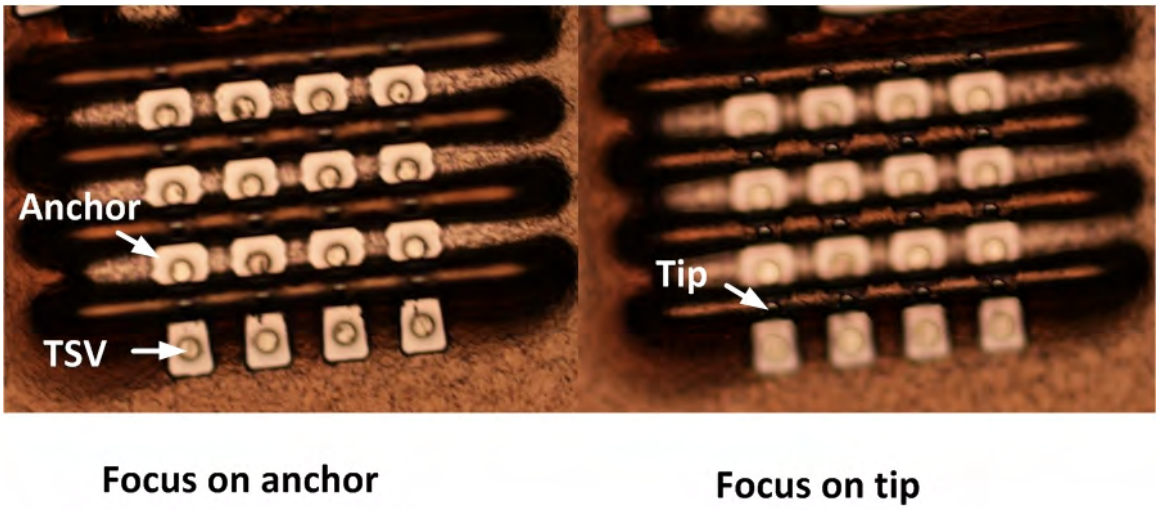
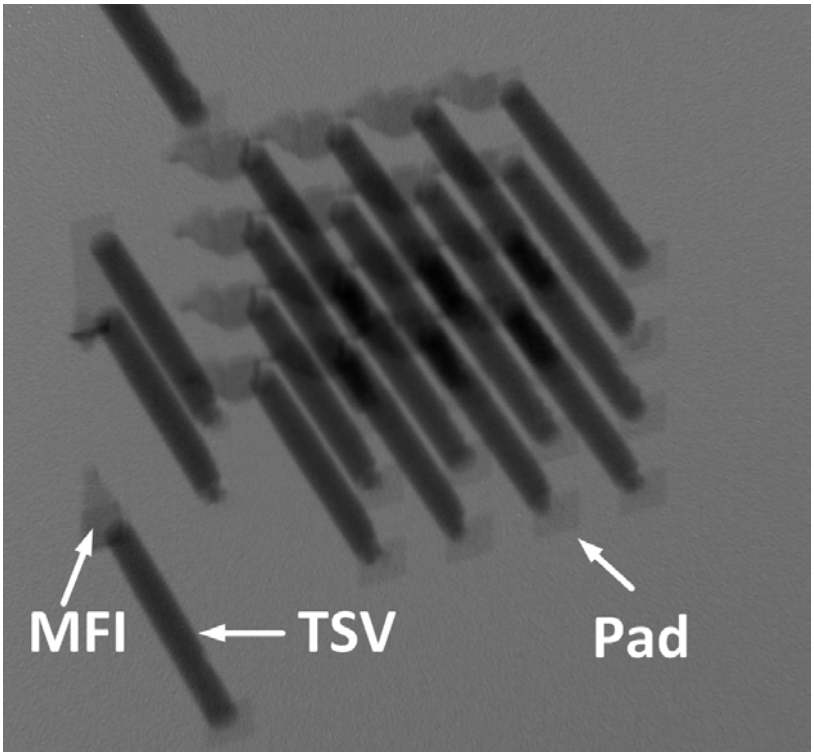
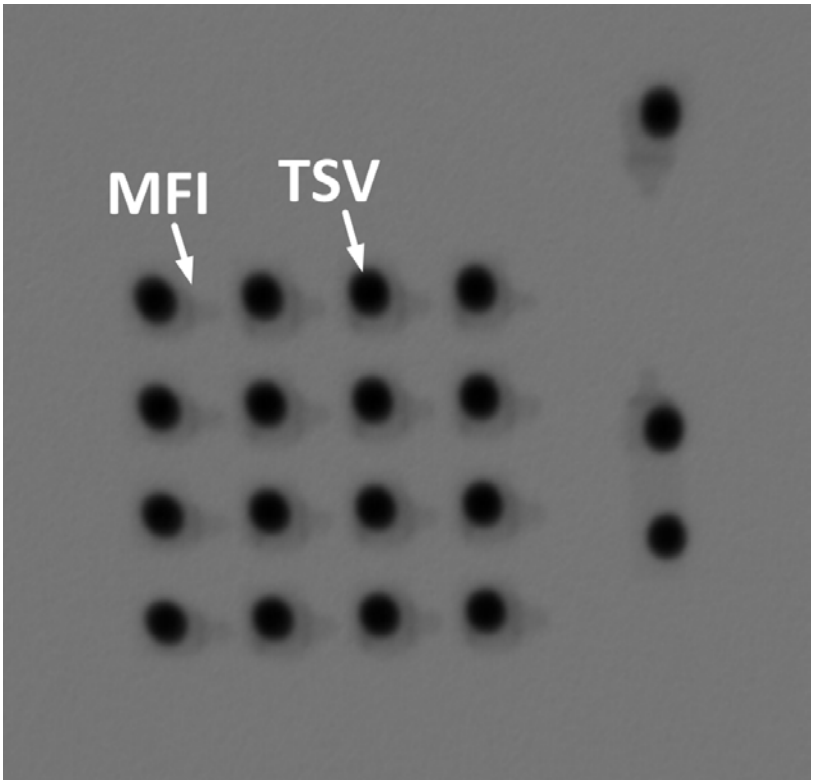


Figure 97: MFI electroplating mold formation on a substrate with TSVs.



(a)



(b)

Figure 98: X-ray image of TSV/MFI integration: (a) top view and (b) prospective view.

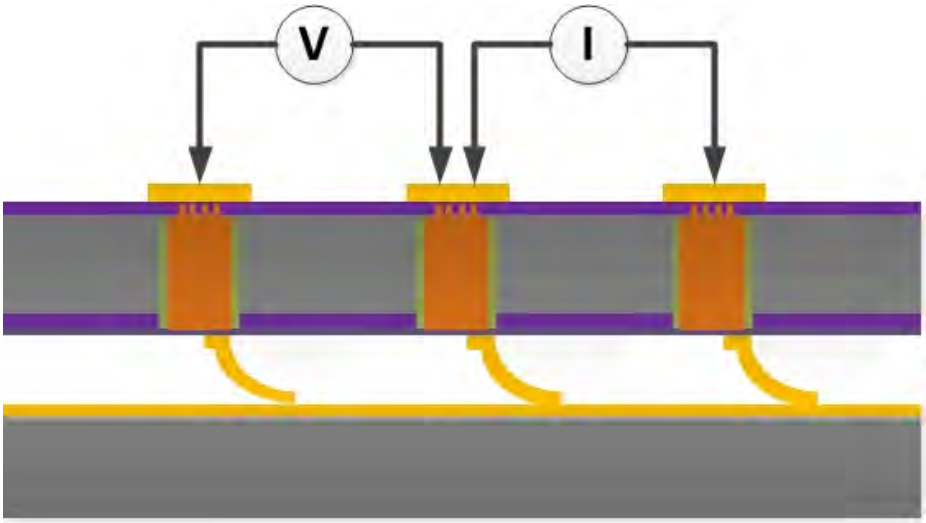


Figure 99: Four point resistance measurement of assembled MFI/TSV.

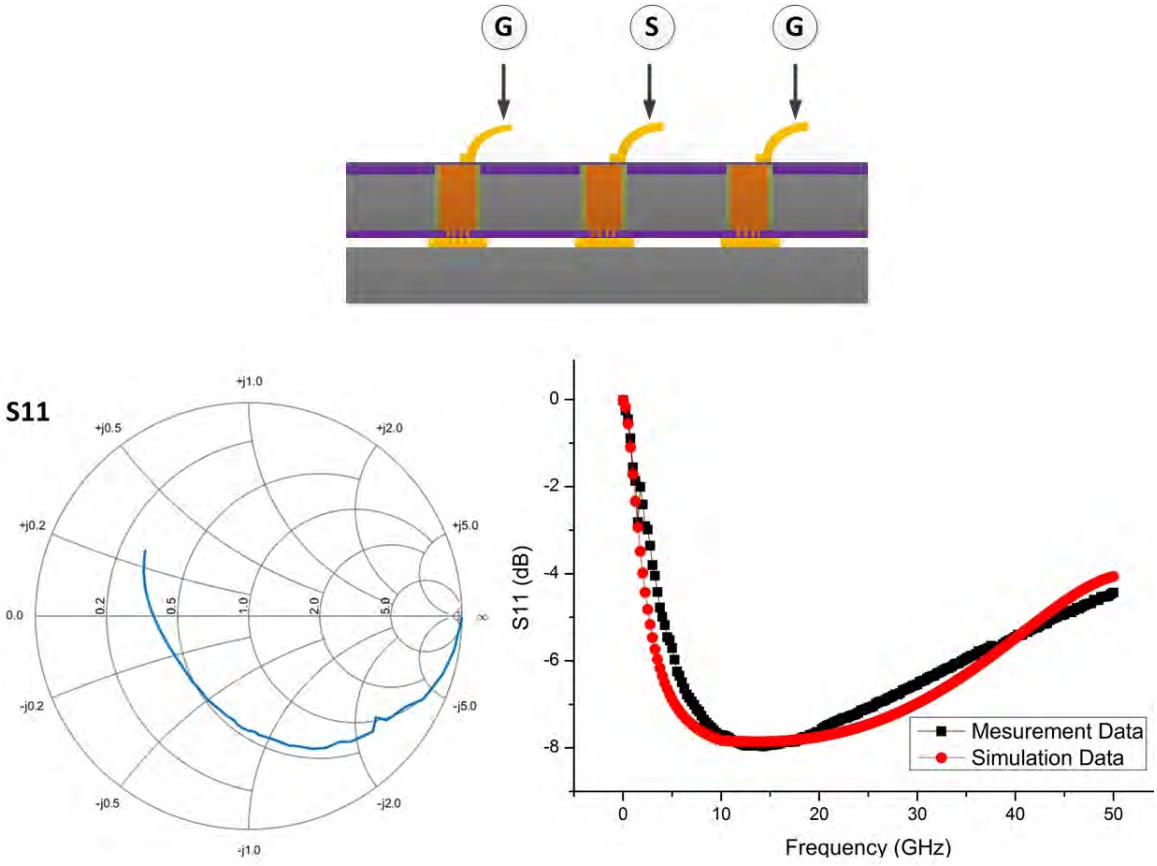


Figure 100: Single port RF probing measurement of MFI/TSV.

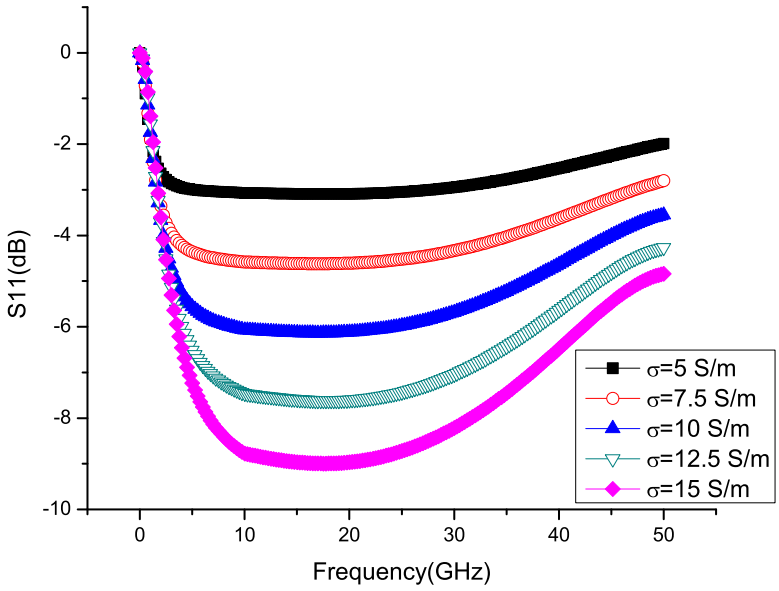


Figure 101: Silicon substrate conductivity effect on MFI/TSV insertion loss.

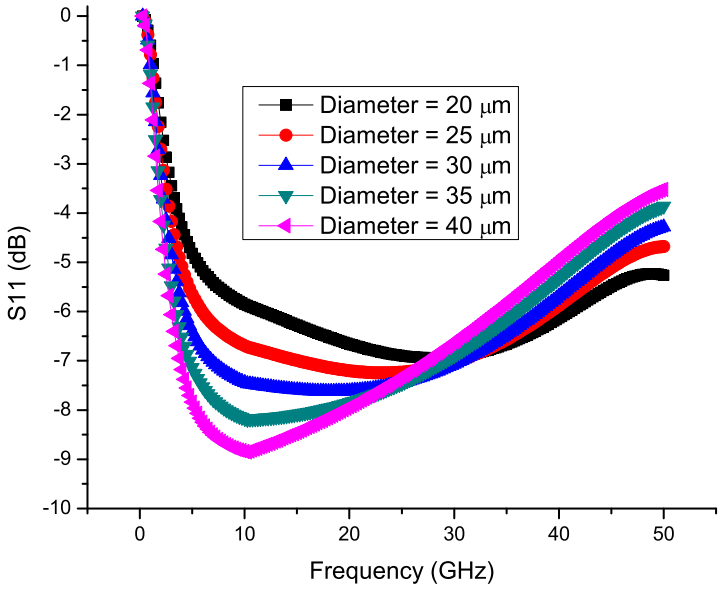


Figure 102: TSV diameter effect on MFI/TSV insertion loss.

7.3 System Level Demonstration

The proof-of-concept demonstration of bridged multi-interposer system, as shown in Figure 103, is described in this section. Three interposer tiles are mounted on top of the FR4 board. The position of each tile is determined by the PSAS on the FR4 board since they are designed to mate with the pits on the back side of the silicon tiles. Next, the silicon bridges are assembled across the adjacent tiles with PSAS side facing downward. Finally, all components of the test bed are glued by applying epoxy around the edge (this was used to simplify the mounting).

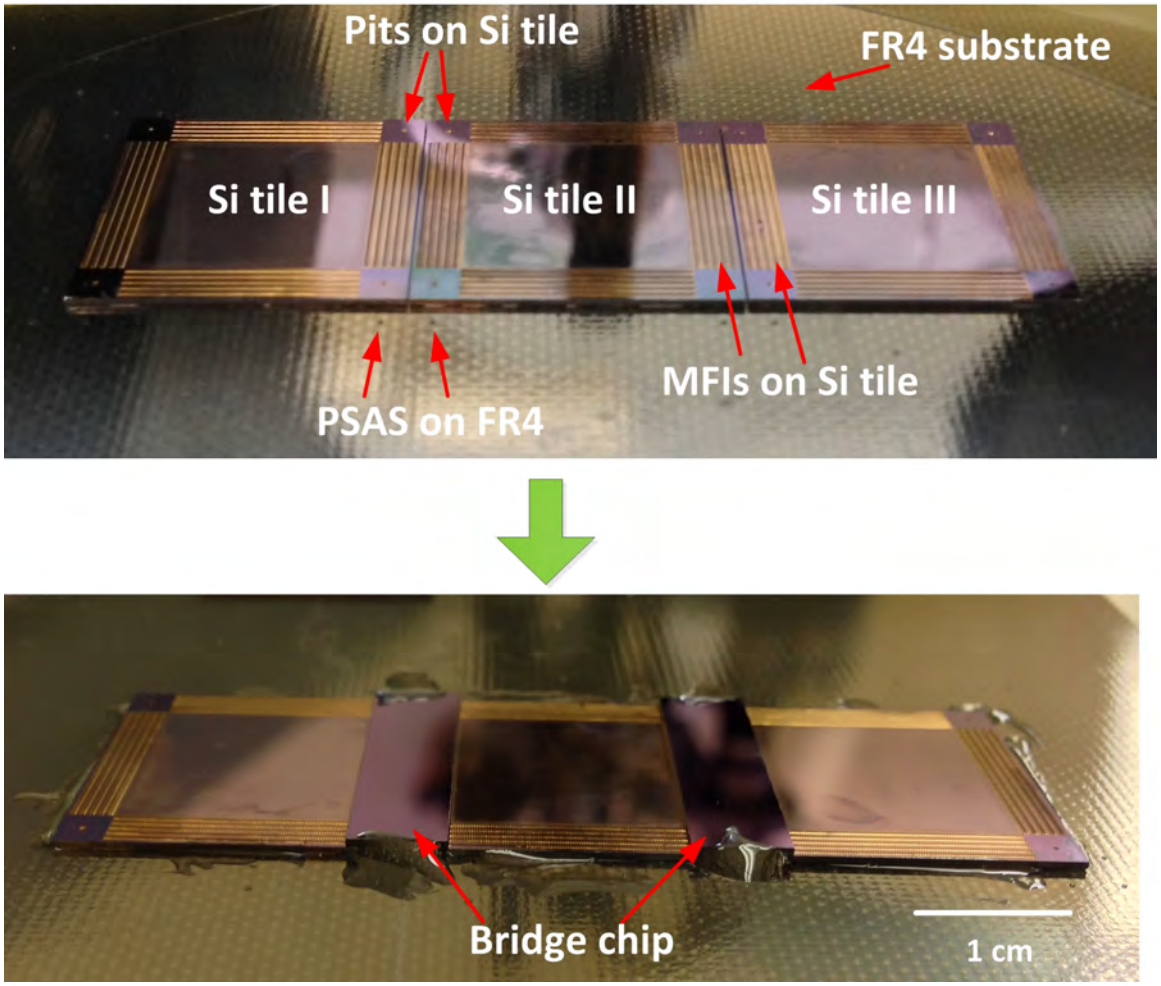


Figure 103: The bridged multi-interposer system.

The alignment accuracy of the assembled test bed is measured by observing vernier

Table 13: PSAS assisted self-alignment accuracy between silicon bridge and tile.

Regions	Si Bridge I		Si Bridge II	
	Horizontal	Vertical	Horizontal	Vertical
Bottom Left (μm)	-4	4.6	-5.2	-5
Bottom Right (μm)	-5.4	-4.8	-5	-5
Top Right (μm)	5.8	3.2	-5.8	-5.2
Top Left (μm)	6	-5	-7.6	-5

patterns via infrared microscopy. As summarized in Table 13, the maximum misalignment between silicon bridges and interposer tiles is at the top left corner of the bridge 2, which is about 7.6 μm. This alignment system, with further optimization, can be used to support silicon nanophotonic interconnection between silicon tiles using the silicon bridge.

Table 14: Resistance between interposer tiles

	1&2	2&3	1&3
Average (Ω)	1.51	1.6	4.98
Expected Value (Ω)	1.32	1.32	4.36
Standard Deviation (Ω)	0.138	0.14	0.363
No. of Samples	20	20	20
No. of MFIs in Chain	20	20	40

Electrical resistance is measured between interposer tiles to verify electrical connectivity. The X-ray images show that the assembled system and the location of the probes for measuring resistance. Table 14 summarizes the results. Expected values are calculated by taking into account the resistance of MFIs measured using four point electrical measurement as well as the gold-coated wire traces fabricated on the interposer tiles and silicon bridges. Data shows that the resistance is within a single standard deviation of the expected resistance. The major source of variation is the wire traces, which have been electroless plated; noticeable thickness variation is

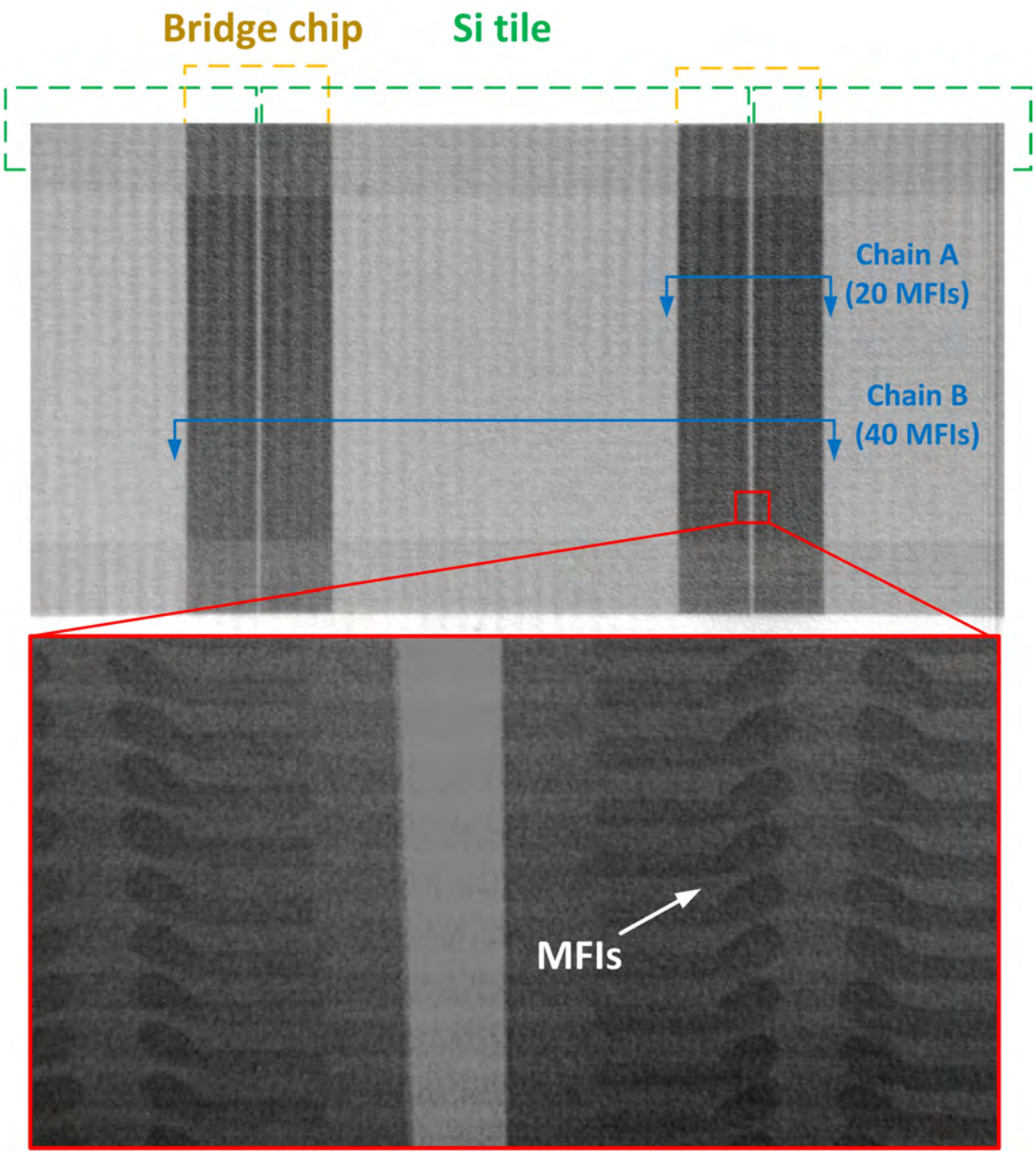


Figure 104: X-ray image of bridged multi-interposer system.

introduced after the process.

7.4 Conclusion

A novel 2.5D interconnection platform, bridged multi-interposer system, is described to address the need for a large-scale high-performance heterogeneous system in this

chapter. In the envisioned system, multiple interposer tiles are aligned and directly assembled on an organic substrate using PSAS/pit self-alignment. Interconnections between the tiles are provided through silicon bridge chips, which are mounted above two or more tiles. MFIs are used to enable a reliable tile-to-bridge and tile-to-organic substrate interconnection. In addition, the key enabling technologies of this platform are demonstrated as well, including: 1) low cost accurate alignment mechanism based on PSAS/Pit self-alignment; 2) MFI/TSV integration and 3) double-sided MFIs. Finally, a test bed with three tiles mounted on FR4 and bridged by two chips is demonstrated. The accurate alignment between tile and bridge is calibrated by IR images. The electrical continuity between three tiles is experimentally verified as well.

CHAPTER 8

SURFACE TENSION ASSISTED BALL-IN-PIT SELF-POPULATION (STAP)

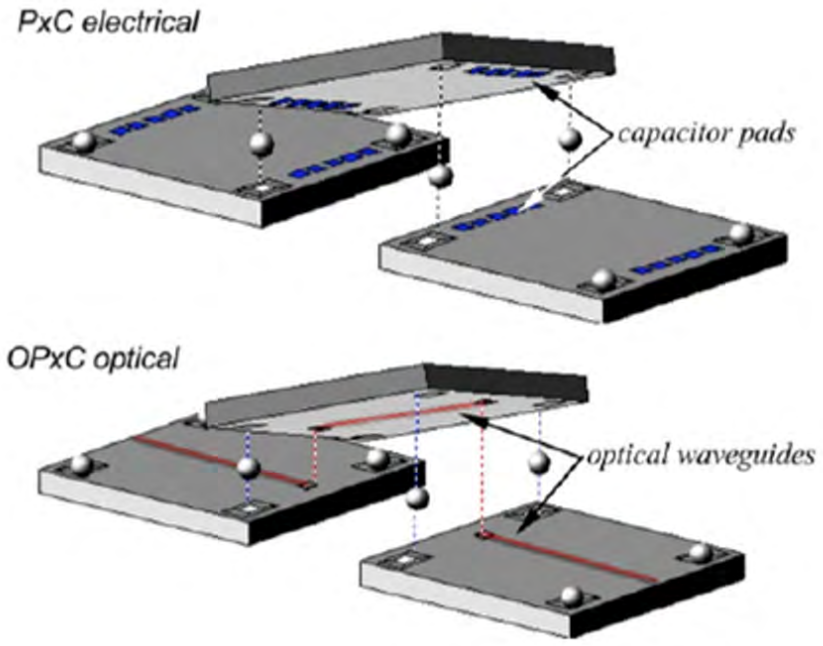
8.1 Introduction

As discussed in Chapter 1, to address the limitations in performance and I/O density, wireless inter-chip interconnects, called Proximity Communications (PxC), are being developed at Oracle Labs. Figure 105(a) [75], [76] shows an illustration of Capacitive PxC and Optical PxC interconnects. Inter-chip communication with bandwidth densities as high as 430 $Gbps/mm^2$ [77] and 700 $Gbps/mm^2$ [78] have been demonstrated by capacitive and optical PxC I/Os, respectively.

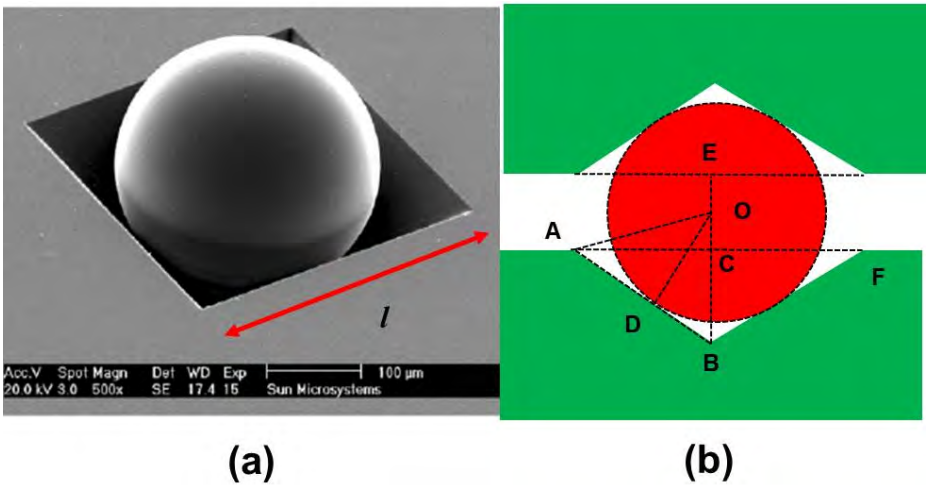
As shown in Figure 105(b), Ball-in-pit is an alignment mechanism to achieve highly precise and repeatable chip-to-chip alignment by combining two naturally complementary geometries: an inverse pyramid shaped pit and a precision microsphere. The pit has sidewalls angled at 54.7° fabricated by the anisotropic wet etching of a (100) patterned silicon wafer. For optical PxC, lateral alignment accuracy is more important, and alignment better than 1 μm between the transmit-receive waveguides is required. For capacitive PxC, vertical alignment accuracy, i.e. the gap between two chips, is more critical. It has been shown that 10μm or less vertical separation between two couplers is required for high fidelity and low bit-error rate PxC [79].

Overall, the Ball-in-Pit fabrication and assembly process being developed at Oracle Labs has the promise of a low-cost approach for integration and critical alignment in a multi-chip system [28]. However, populating etched pits with balls is presently performed manually by a technician using vacuum pick-up tools and is therefore not feasible for large-scale i.e. wafer-level application. A brute force method to populate

pits on a wafer with balls would likely involve using a pick-and-place tool with a large area vacuum chuck that picks up balls from a ball-reservoir and drops them onto the target substrate. This is similar to solder ball population tools for flip chip assembly,



(a)



(b)

Figure 105: Proximity communications enabled by ball-in-pit self-alignment

such as the solder sphere transfer system from PacTech [80]. While such an approach could be scaled to cover large substrates, it bears the overhead of custom, design dependent vacuum tooling. The elegant surface tension assisted self-population approach we report in this paper is inherently parallel, design-independent, and does not require expensive vacuum assisted precision pick-and-place tooling.

In Section 8.2, we describe the concept and two approaches of surface-tension assisted population (STAP). A surface energy based model is also analyzed to show that the surface tension force is enough to hold the populated ball inside a pit. The fabrication details to form a hydrophobic/hydrophilic pattern on a pitted chip, which is one of the key contributions of this paper, are presented in Section 8.3. The custom setup, experimental procedure and results of STAP are presented in Section 8.4.

8.2 Surface Tension Assisted Population

8.2.1 Concept of STAP

Surface tension assisted population (STAP) is a self-assembly approach for populating balls dispersed in water into etch pits fabricated on a chip or wafer to yield ball-in-pit alignment structures. Figure 106 illustrates the main steps of this process. First, the substrate surface is temporarily modified such that the pits exhibit a hydrophilic behavior and the rest of the chip (i.e. yield area exhibits a hydrophobic behavior.) Following this, a population of appropriately sized balls, which could be made of sapphire, ruby, metal or another hydrophilic material, is dispensed in water, and the aqueous mixture is dragged across the substrate surface. The surface tension of the fluid keeps the balls confined within the liquid volume and the entire population of balls can be moved around freely on the hydrophobic field area. When this aqueous mixture comes across an unpopulated hydrophilic pit, a ball that sufficiently overlaps with the pit opening will fall into the pit and stay there owing to surface

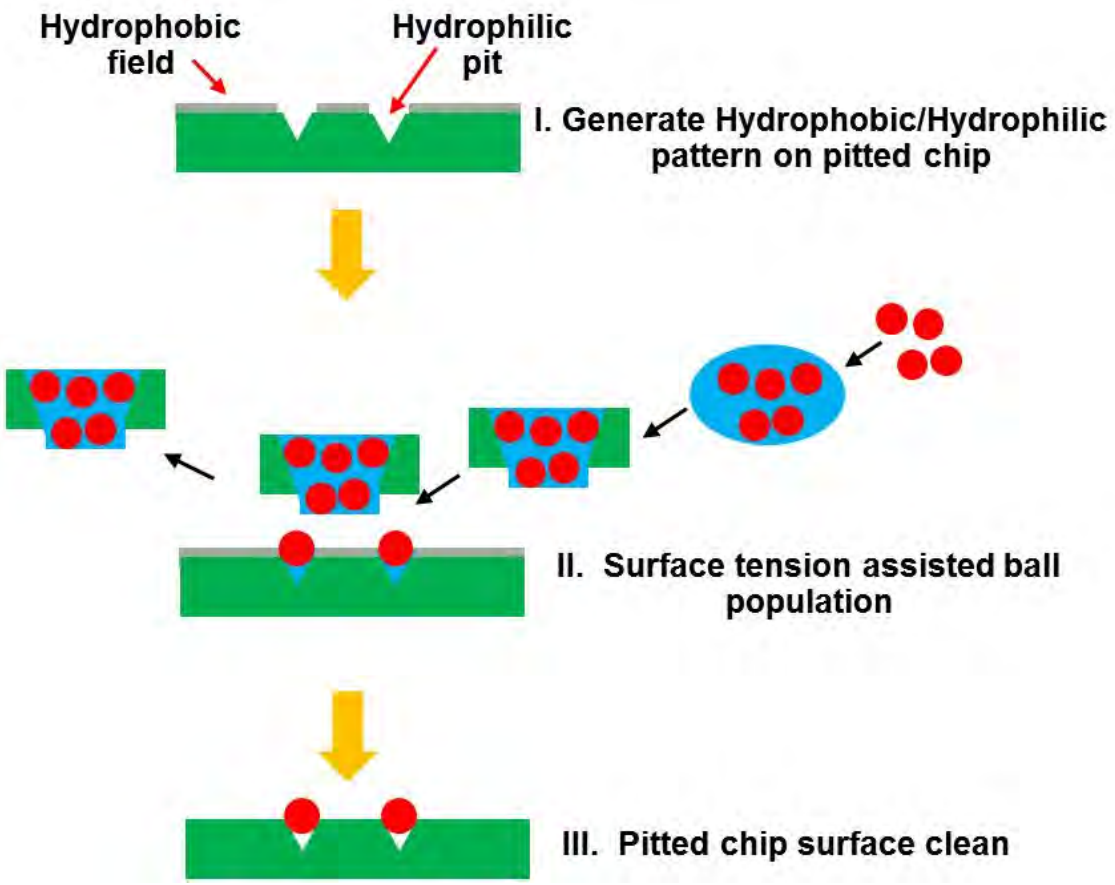


Figure 106: Surface tension assisted ball in pit self-population.

tension from the water in the pit. Once all pits on the substrate have been populated, the hydrophobic surface modification is removed. As will be discussed later, in our approach, the substrate surface is made hydrophobic by selectively depositing a polymer nanolayer. At this point, the populated chip or wafer is ready for assembly using ball-in-pit alignment.

8.2.2 Methods for STAP

As shown in Figure 107, there are two ways to achieve ball-in-pit population as described above: (1) by scanning a population of balls immersed in water across the target pits using a scanning head, and (2) by using a dropping head. In both approaches, hydrophilic balls dispersed within DI water are guided to move over pits to be populated.

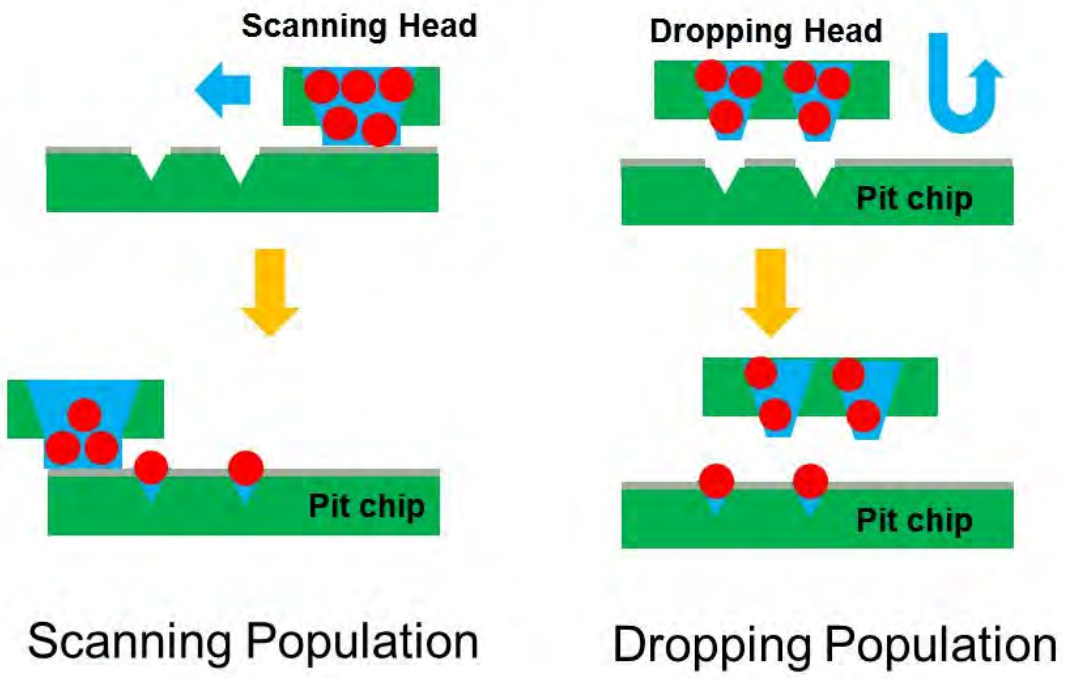


Figure 107: Surface tension assisted scanning and dropping population.

For the scanning population method (Figure 107), balls within DI water are guided by a scanning head and move across the pitted wafer surface. As this scanning

head moves over a pit or an array of pits, a ball which crosses over any part of an unpopulated pit will be caught by the hydrophilic pit due to surface tension force from the water inside the pit; any ball standing over the hydrophobic field area will move away with the water column that is being guided, thus leaving behind a clear field area.

For the dropping population approach, a dropping head fixture containing balls and DI water is required as shown in Figure 4. Each dropping head on this fixture is essentially a through hole that functions as a reservoir containing multiple balls in an aqueous solution. On this dropping fixture also, the field area is hydrophobic and the through holes/reservoirs are hydrophilic. As such, surface tension of the water keeps the balls confined to their respective dropping head. The number and pattern of holes in the fixture matches the design or a subset of the design of the targeted pitted wafer that is to be populated. During the population process, the dropping head is precisely aligned with the targeted array of pits and then moved downwards to contact and drop balls into hydrophilic pits. Alternatively, the dropping head is moved down to contact the hydrophobic field area of the pitted substrate first then scanned over a short distance to drop balls into pits. This short scanning assisted dropping approach decreases the alignment accuracy required between the dropping head and the target pits on the wafer. After dropping balls into pits, the dropping head is moved away from the pits so that any balls that did not fill a pit come into contact with the hydrophobic field area. After this short lateral movement, the head is lifted away from the wafer/chip surface to disconnect the water column from the pitted chip. Any ball that is not inside a pit will be held by the surface tension of the water column and carried away by the dropping head.

Both these population processes have the potential to achieve large-scale ball-in-pit population, but one may fit some scenarios better than the other. Population by scanning is a straightforward and pit pattern independent approach, which lowers the

population cost. However, the scanning population method counts on having a large number of balls in the aqueous mixture much greater than the number of pits. As long as this condition is met, then pits have a high probability of being populated. On the other hand, the dropping head population method requires a custom designed albeit simple dropping head fixture for each targeted pit pattern. However, the population rate could be much faster. In addition, the dropping population method can work even with a 1:1 ratio between the number of pits and dropping head sites, and therefore has a potentially higher population efficiency compared with the scanning method. Owing to its relative simplicity, the scanning population approach was adopted for the demonstration in our lab.

8.3 Fabrication

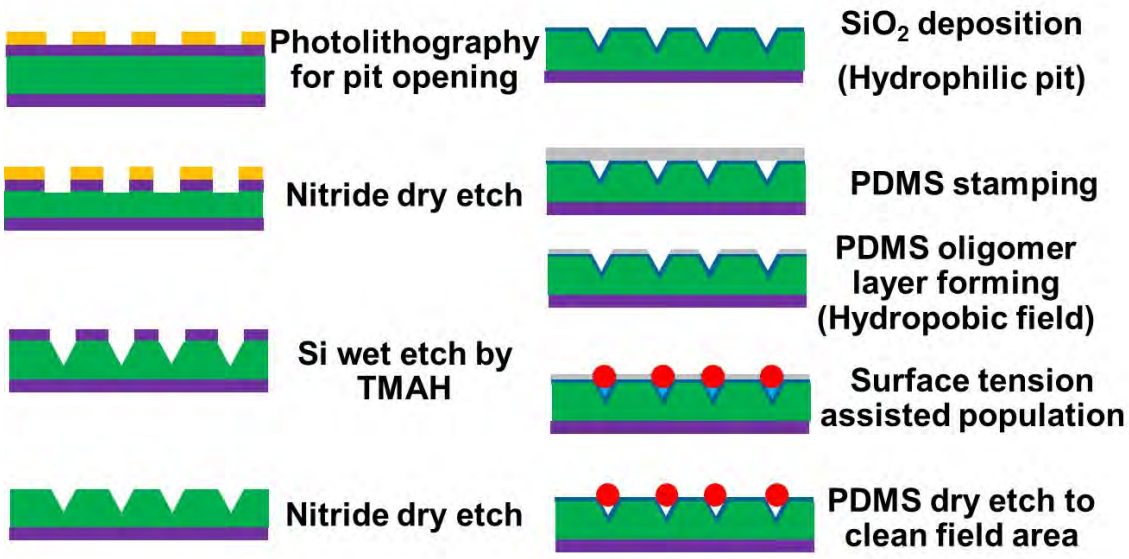


Figure 108: Fabrication process of the pit wafer with hydrophobic/hydrophilic pattern and surface tension assisted population flow.

To demonstrate the self-population concept, a test vehicle was fabricated consisting of a pitted Si wafer bearing hydrophilic pits and a hydrophobic field area. The fabrication of such a dual-zone wafer was achieved via a self-aligned, low-cost

batch-processing method, and is a major contribution of this research. The process is shown in Figure 108. First, a negative photoresist is spun onto a Si wafer with a silicon nitride hard mask on both sides. The front-side is then patterned using lithography, and a nitride dry etch process is used to create the wet etch hard mask pattern. Next, the photoresist is stripped off and pits are etched into the exposed Si via wet etching using Tetramethyl Ammonium Hydroxide (TMAH), a well-known anisotropic etchant of Si. For this process we used a 6.25% TMAH @ 80°C. Following this, the silicon nitride hard mask is removed and a hydrophilic layer, which is 200 nm PECVD SiO_2 here, is deposited on the surface of the wafer as well as on the pit sidewalls. Following this, a hydrophobic Polydimethylsiloxane (PDMS) oligomer layer is transferred onto the surface of the wafer field area by a stamping process [81]. Since all pits are negative structures, the hydrophilic surface inside of pits is not affected during the stamping process. Details of the formation and removal of the hydrophobic layer are discussed in subsection C below. At this point, a wafer with hydrophilic pits and a hydrophobic field area is ready for the STAP process. Once the population process is complete, the PDMS hydrophobic oligomer layer can be removed by a short CF_4:O_2 RIE process [82]. Therefore, the entire exposed wafer field area, including area occupied by bonding pads is clean for any post processing and assembly.

8.3.1 Pitting by Silicon Anisotropic Etching

The pit chip used for ball-in-pit population experiments had 225 μm wide pits on a 500 μm pitch (Figure 109 (a)) which were formed by TMAH Si anisotropic wet etching. As the etch rate on the (111) surface is much lower than the etch rate on the (100) surface during TMAH Si wet etching, this results in an inverted pyramid shape with sidewalls 54.7° below the horizontal. For a shallow Si wet etch, the etching of (111) is negligible. However, in our case, where the etch pit depth could be 160μm,

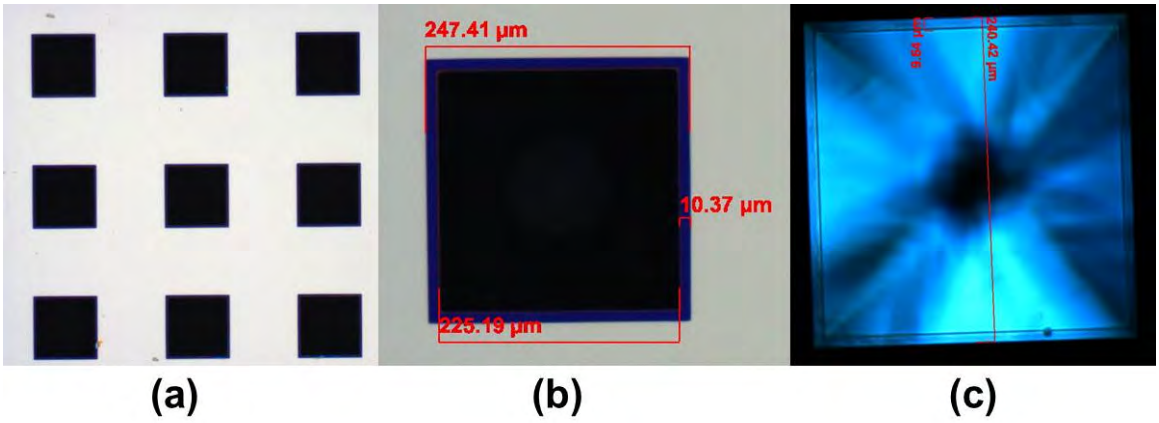


Figure 109: Si TMAH wet etching with Nitride mask.

the undercut beneath the nitride hard mask is fairly large, an example of which is shown as the purple outline in Figure 109 (b). Figure 109 (c) is a dark-field image picture of the pit, and it clearly shows the suspended nitride margin due to (111) undercut etching. There are two issues induced by (111) undercut etching:

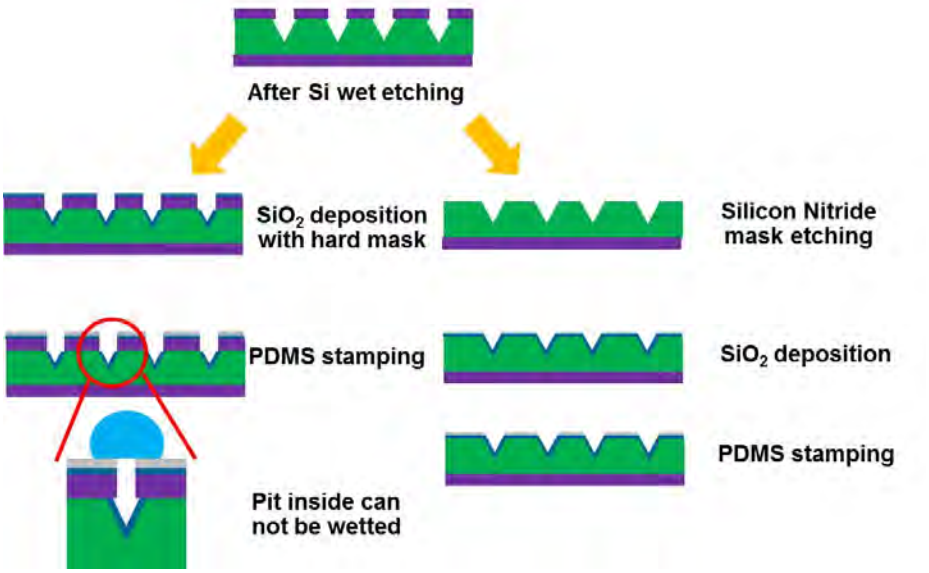
1. the actual pit size is enlarged and therefore it shrinks the assembly gap, and
2. the overhanging nitride film prevents the sidewalls of the pit from being wet by DI water, which is further discussed below.

8.3.2 Hydrophillic Pit

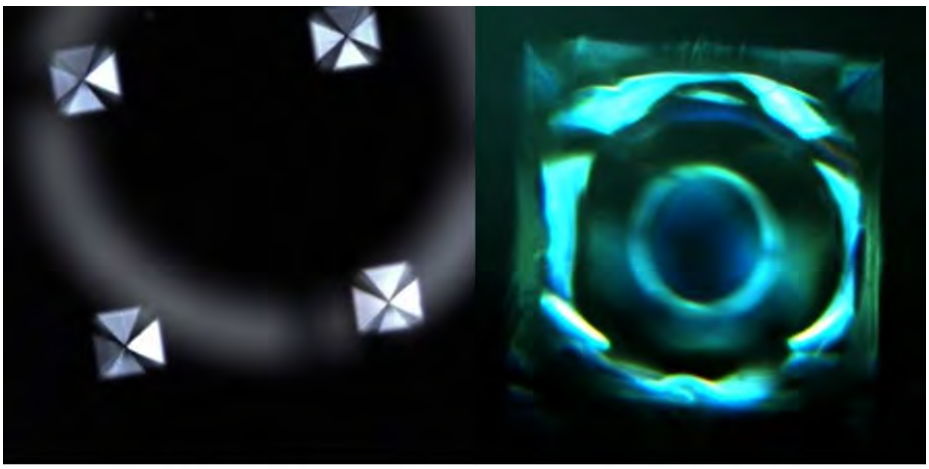
Figure 110(a) illustrates the two methods of fabricating hydrophilic pits to be populated. In both approaches, the pits are lined with PECVD SiO_2 to make them hydrophilic. PECVD SiO_2 has a contact angle of less than 5°. For the approach shown in the left column, SiO_2 is deposited on the pitted substrate with an undercut nitride mask. After PDMS stamping, the field area becomes hydrophobic. However, in this case a water droplet will roll over the pit. Owing to the presence of the suspended nitride layer on the pit edge, the surface tension of water can hold the droplet and prevent wetting of the pit sidewalls. As a result of this structure-induced

hydrophobicity, the pit will not be filled by water and therefore cannot attract a ball during the population process.

To overcome this phenomenon, the nitride mask is removed by a dry etch before



(a)



(b)

Figure 110: Hydrophillic pit: (a) fabrication and (b) wetting capability comparison.

the SiO_2 deposition (see right column of Figure 110(a)). Figure 110(b) illustrates the difference between hydrophobic and hydrophilic pits. In the pictures, both types of pits are covered by water. Hydrophobic pits, with the overhanging nitride mask and structure induced hydrophobicity cannot be wetted and filled with water. As a result, they appear shiny under the microscope. Hydrophilic pits without the overhanging nitride mask are wetted and full of water. As a result the sidewalls don't appear as shiny.

8.3.3 Hydrophobic Field

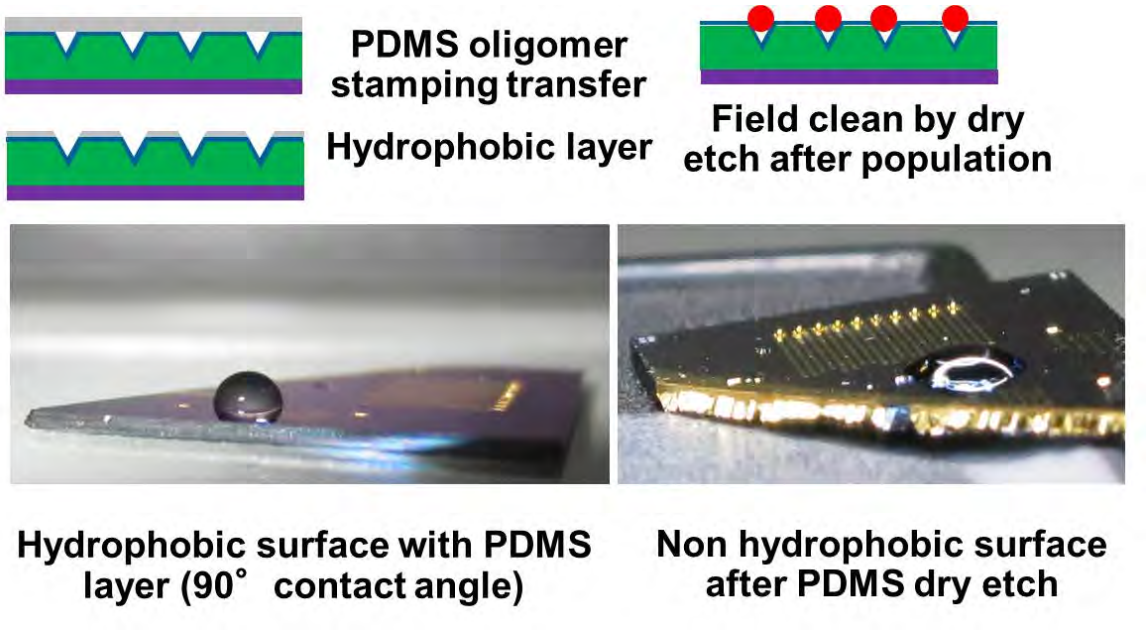


Figure 111: Hydrophobic field formation and removal.

The surface modification to make the field area hydrophobic is achieved by a stamping process that transfers an ultrathin (5-10nm) layer of PDMS oligomer material, with a contact angle of 90° to water (see Figure 111). The combination of a mask-free hydrophilic layer deposition and lithography-free fabrication of hydrophobic/hydrophilic pattern, enabled by the use of a stamping process on a pitted chip, is a key processing innovation. The thin oligomer layer in the field area can be removed

by a short dry-etch process [81]. As this PDMS oligomer layer is only 5-10 nm, and the dry etch rate of PDMS is much higher than the etch rate of Silicon Dioxide and the ball (metal or sapphire), the short timed dry etch process does not have any side effects. Bottom two pictures in Figure 111 shows a comparison of the contact angle of a water droplet on a PDMS oligomer coated surface and on the bare surface after PDMS cleaning. The contact angle of PDMS coated surface is about 90° which shows the hydrophobicity. After PDMS dry etch, the contact angle is much lower and the surface is not hydrophobic any more.

8.4 Demonstration and Results

In order to demonstrate surface tension assisted ball population, an assembly station was built comprising two components: 1) a 4-axis wafer chuck, which is common in most bonding equipment), and 2) a 2D scanning head mount. A photo of this setup is shown in Figure 112. The 4-axis stage includes an XY linear translation stage, Z linear translation and rotation stage; the 2D mount can move in Z and has adjustable tilt. During the population process, the XY linear translation stage is used to scan the pitted wafer underneath the scanning head. The Z linear translation is used to modulate the gap between the pitted wafer and the population head. The 2D tilt adjustable platform is used to make the scanning head parallel to the wafer such that all balls guided by the water column experience a uniform capillary force.

Figure 113 shows ball-in-pit scanning population process in greater detail. The scanning head in this demonstration is a glass slide (hydrophilic) with a thin PDMS membrane (hydrophobic) attached a very short distance from the edge, as shown in Figure 113 (a). Placement of the PDMS strip as shown in Figure 113 (b) creates a very narrow hydrophilic strip on the tip of scanning head, which is confined by the PDMS hydrophobic zone (Figure 113 (b)). A small volume of the water and balls mixture is first dispensed on the pitted wafer. The wafer is then raised up to the

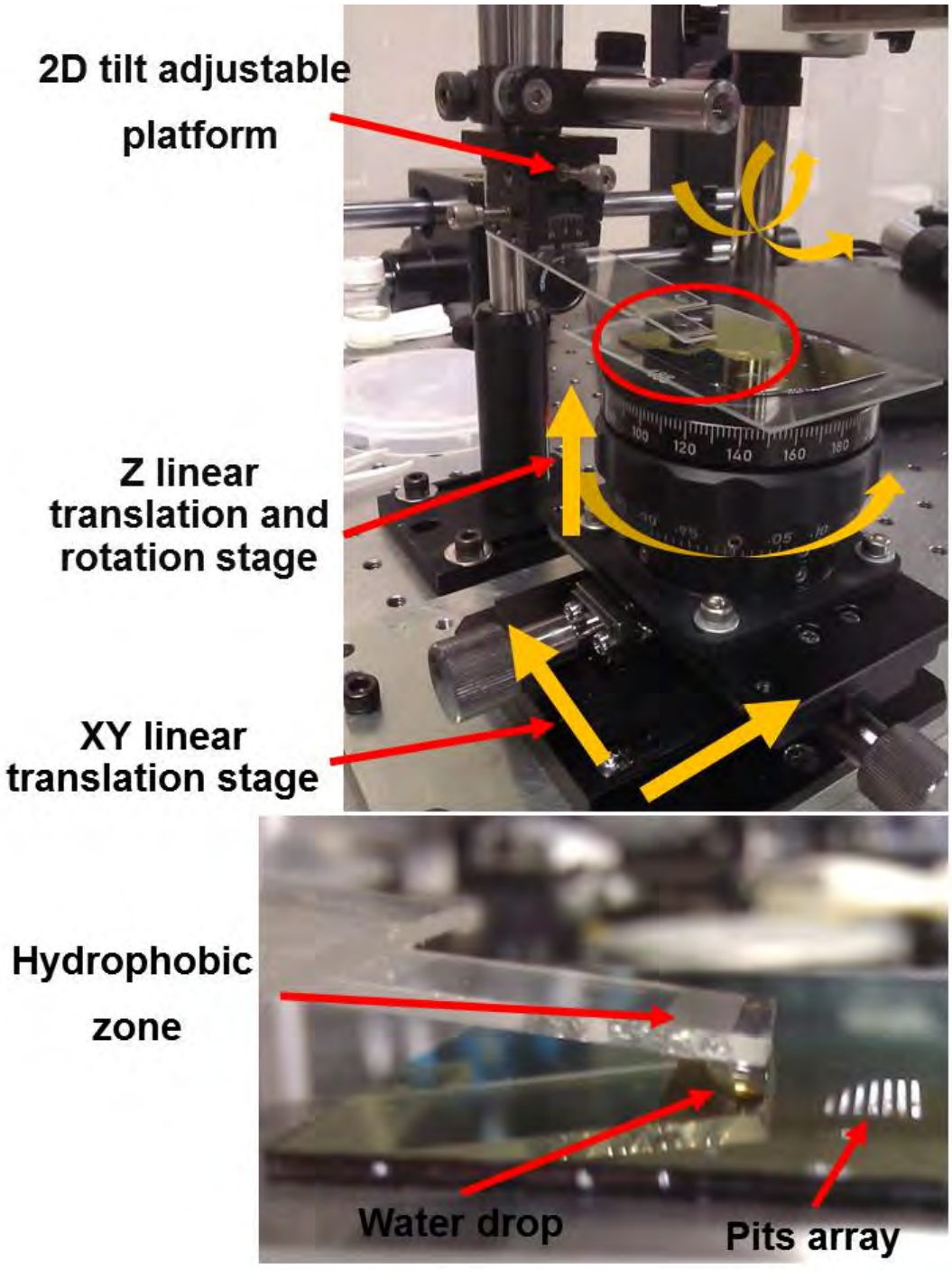


Figure 112: Demonstration setup of surface tension assisted ball in pit self population .

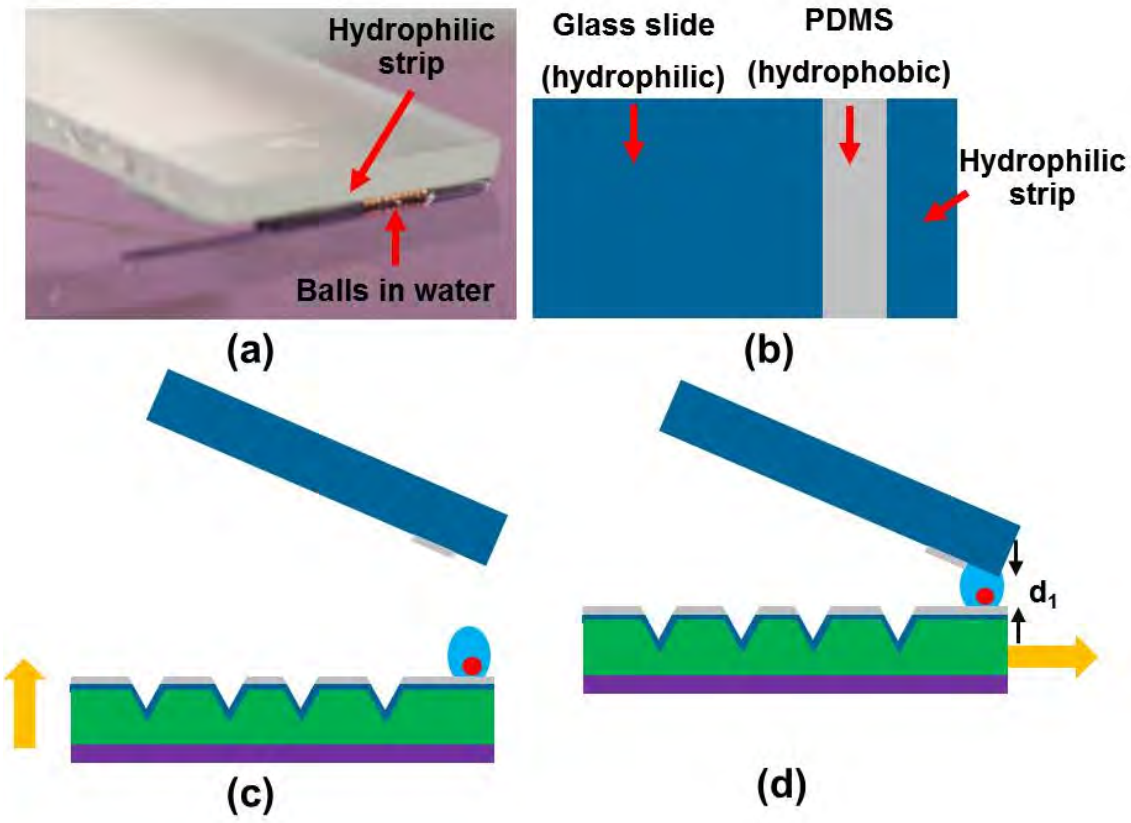


Figure 113: Population guided by glass slide scanning head.

scanning head by the Z linear translation stage until the water droplet contacts the scanning head. The stage is then raised further to achieve a proper scanning gap, i.e. height of the water column (d1 in Figure 113 (d)). The scanning gap between scanning head and pitted chip is about 500 μm for a 200 μm diameter ball population. After that, the water droplet is guided and rolled back and forth over a short distance several times to distribute the balls in the water uniformly. This completes the setup procedure for the population process.

Figure 114 shows picture frames captured from a video of surface tension assisted ball population by scanning a multitude of 188 μm diameter balls across a 5x5 pits array with 500 μm pitch. Within 65s, 24 out of 29 balls are populated into 25 pits. At 00s, the scanning head contacts the water droplet; until 17s, the water droplet is rolled back and forth several times and the balls align to form several lines in the water; at 32s, 44s, 50s, 61s, 65s, the first to fifth rows of pits are populated by balls. All pits are populated except the corner one of the fifth row, which yields a 96% population rate. An advantage of surface tension assisted population approach is its reworking capability. After the first population scan, the 5 unpopulated balls are guided back to the fifth line, and the last pit is successfully filled as shown in Figure 114 (h). At this point, the population yield is 100% (25/25) and the coefficient of utilization is 86.2% (25/29).

8.5 Conclusion

In this chapter, methods of using a hydrophobic and hydrophilic pattern to achieve large-scale ball-in-pit self-population are reported. The populated ball-in-pit structures would be employed for achieving submicron layer-to-layer alignment, for example in a multi-chip package that employs PxC chip-to-chip interconnects. The key features introduced in this chapter are: 1) a process for lithography-free hydrophobic/hydrophilic pattern formation and removal, 2) a surface tension assisted,

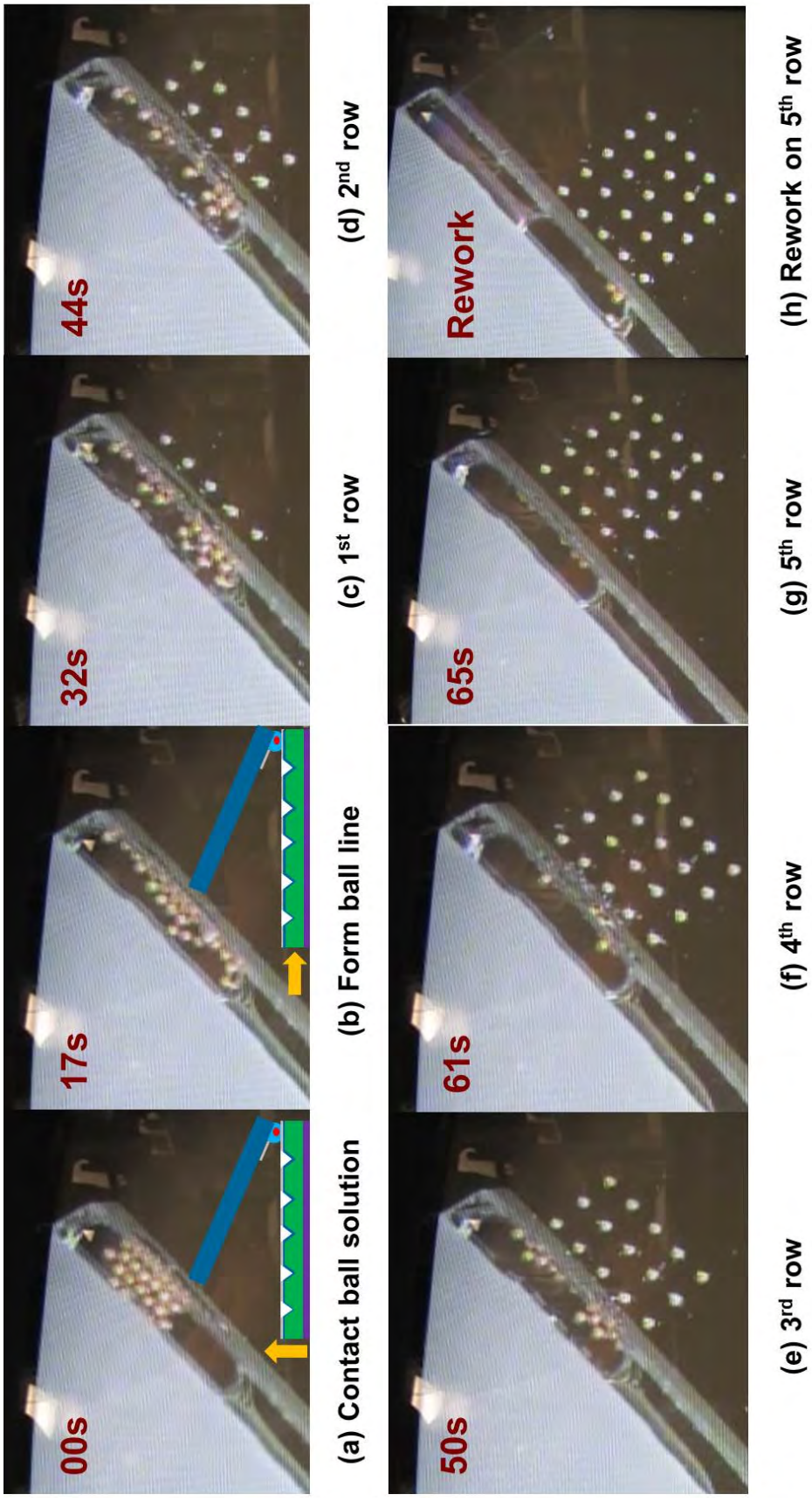


Figure 114: Surface tension assisted ball-in-pit population video.

pit pattern independent, scanning approach for ball-in-pit population, which is also capable of rework.

CHAPTER 9

HETEROGENEOUS SYSTEM III: 3D INTEGRATION WITH MFI ASSISTED THERMAL ISOLATION

9.1 Introduction

As discussed in Chapter 1, MFIs can replace microbumps to realize chip-level dense flexible I/Os and release the thermal stress induced by CTE mismatch. Therefore, the underfill used with microbumps can be eliminated as well. The underfill elimination not only reduces packaging complexity, but also reduces the thermal coupling between the stacked chips. In this chapter, we exploit this feature to develop a thermal isolation technology for 3D ICs.

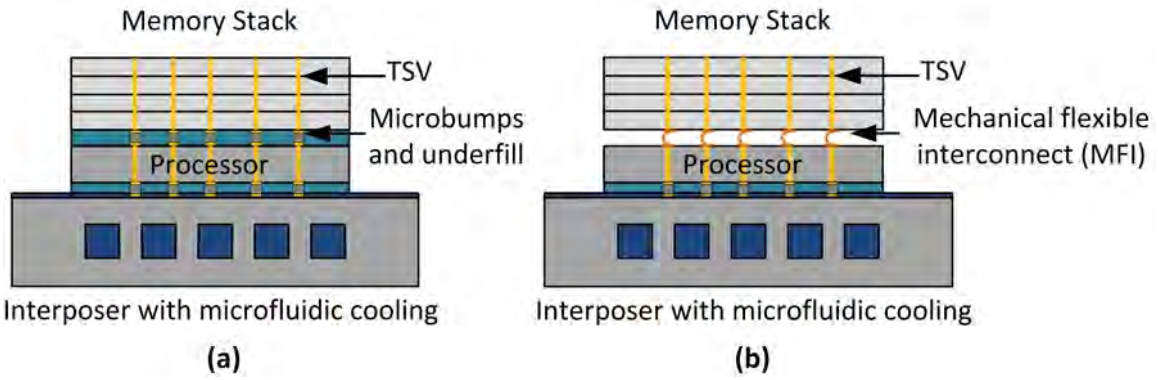


Figure 115: MFIs assisted thermal isolation concept: (a)traditional configuration and (b)MFIs assisted thermal isolation.

FEM simulation results shown in Figure 116 (a) illustrate the DRAM (represented by low power die) is severely thermally coupled to the CPU (represented by high power die) and can be heated to a temperature as high as the CPU. The high temperature on the DRAM leads to performance degradation and power overhead that

might offset some of the benefits obtained by the 3D DRAM/CPU stacking. To address this challenge, we propose the system configuration shown in Figure 115 (b) in which MFIs and microfluidic cooling are used for thermal isolation and cooling, respectively. As shown in Figure 116 (b), MFI assisted thermal isolation technology can thermally decouple the DRAM and CPU, and hence yield a significantly lower DRAM temperature.

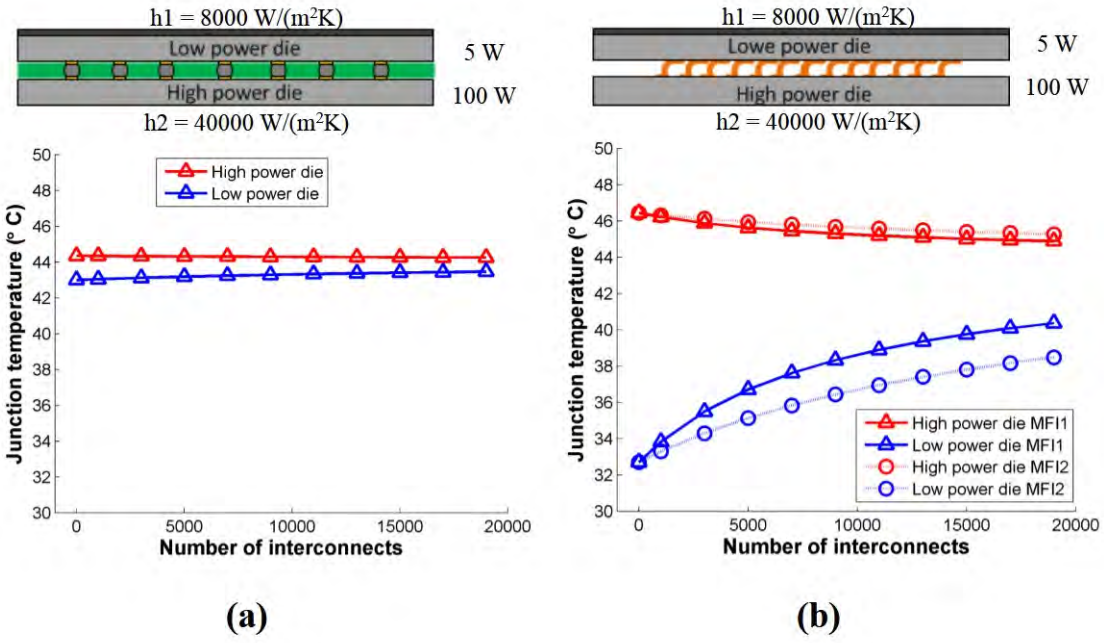


Figure 116: Comparison between MFIs assisted thermal isolation and traditional configuration.

9.2 System Demonstration

A two-tier test bed, as shown in Figure 117, has been designed to demonstrate and verify the concept of MFI assisted thermal isolation. The top low-power tier and the high-high power tier represent the DRAM chip and CPU, respectively. Heaters are fabricated on both tiers to create the designed system power map. These two stacked tiers are separated by 10 μm high spacers, and inter-tier electrical interconnections are realized using MFIs. Microfluidic cooling structures developed in [83]–[87] are

fabricated on the back side of the high power tier for thermal dissipation.

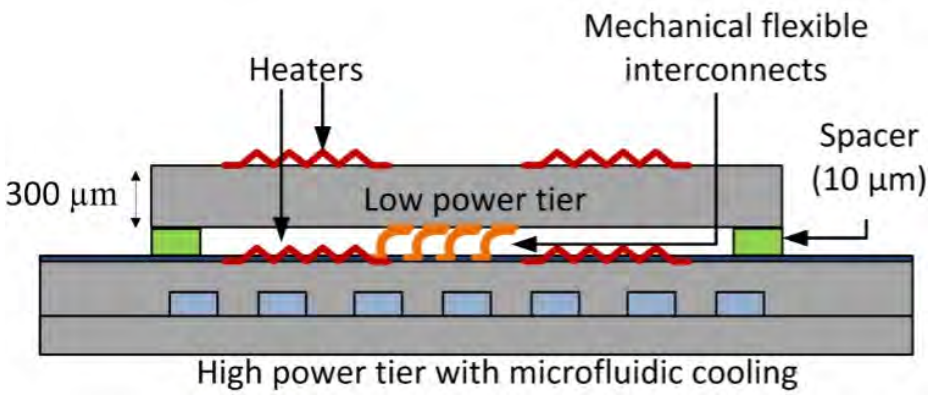


Figure 117: Test bed for MFIs assisted thermal isolation demonstration.

9.2.1 Fabrication

The fabrication process flows for the two tiers are shown in Figure 118:

Low power top tier

For the low-power tier, the process starts with passivating a double-side polished 300 μm thick silicon wafer. Next, the Pt based heaters and resistance temperature detectors (RTD) are formed on the top side using lift-off and then passivated by an evaporated gold layer. Figure 119 (a) shows the image of the RTDs on the top tier. The wafer containing the fabricated heaters is then flipped over and the Au-NiW MFI process developed in Chapters 2 and 3 is performed. The fabricated Au-NiW MFIs are 2.5 μm thick, 20 μm tall and have a pitch of 75 μm by 100 μm. The entire array containing 1,000 MFIs occupies 9940 μm by 870 μm. Besides the high yield strength, NiW is chosen in this demonstration because it has a low-thermal conductivity of 90 W/mK, which yields better thermal isolation between the two tiers compared to copper. The thermal modeling has confirmed that the thermal resistance of a single MFI is 20,000 K/W, which is comparable to a 4 μm diameter solder bump of the same height. Figure 119 (b) and (c) shows the MFIs used for four-point and daisy chain resistance measurements, respectively.

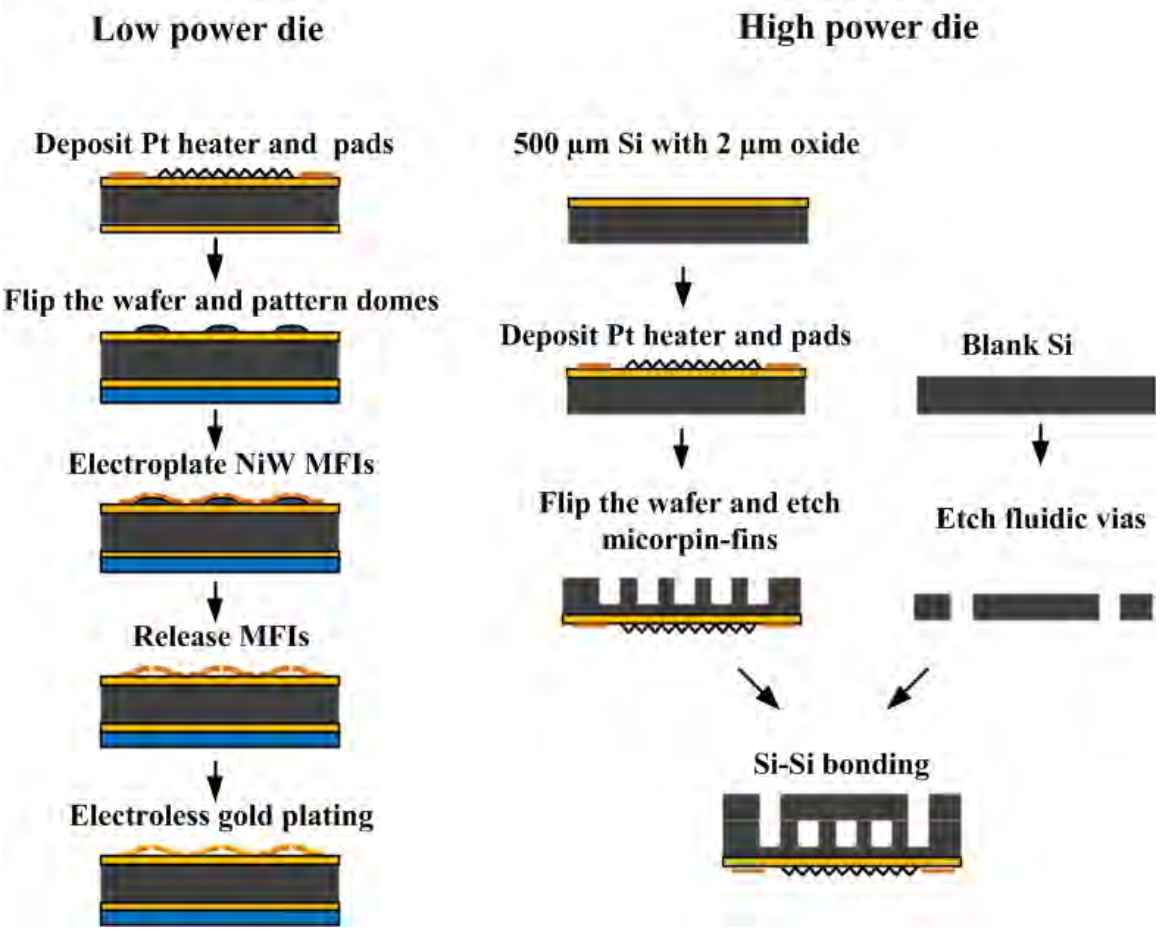


Figure 118: Fabrication process of test bed including low power die and high power die.

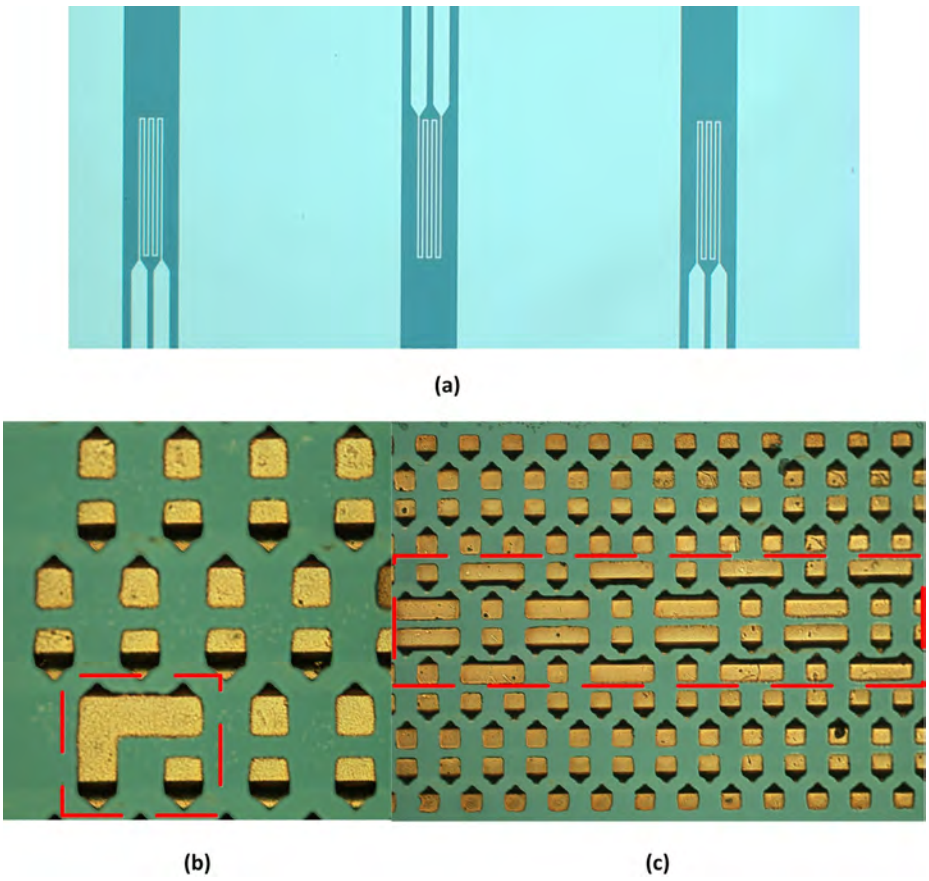


Figure 119: Key components of the top tier: (a) thermal resistance temperature detectors (RTD) on top tier, (b) MFIs for four-point resistance measurement, and (c) MFIs for daisy chain resistance measurement.

High power bottom tier

For the high-power tier, the process starts with a double-side polished 500 μm thick silicon wafer. The wafer thickness is chosen for better mechanical stability after deep silicon micropin-fin etching. Next, Pt heaters and RTDs are formed in the same way as they were in the top tier. Figure 120 (a) shows the fabricated sample with a background heater (left) and a hot spot heater (right). The wafer with heaters is then flipped over and 200 μm deep micropin-fins (Figure 120 (b)) are etched using a standard Bosch etching process. Simultaneously, another 300 μm thick cover wafer is etched through to form fluidic I/Os. The wafer with heaters and the cover wafer are then bonded using Si-Si fusion bonding followed by 24 hours of annealing at 400 °C. Finally, sapcers are formed on the heater side to separate the two tiers with a gap of 10 μm.

9.2.2 System Assembly

The diced low-power and high-power chips are assembled using a flip-chip bonder, as described in Chapter 4. As shown in Figure 121 (top), on the low-power chip, 9 RTDs are located along the center at a pitch of 1 mm to measure the temperature gradient. Each RTD has dimensions of 500 μm x 88 μm and yields a resistance of 200 Ω. As shown in Figure 121 (b), on the high-power chip, the background heater has 1 cm x 1 cm footprint and can be powered up to 100 W/cm^2. The two hot spots are 1 mm by 1 mm and can be powered up to 200 W/cm^2. The temperature is measured using the heater/RTD and compared with the temperature on the low power tier. As shown in Figure 122, X-ray images are used to check the alignment and voids.

9.3 Electrical and Thermal Measurement

The results of electrical and thermal measurements are reported in this section to quantify the MFIs assisted thermal isolation technology.

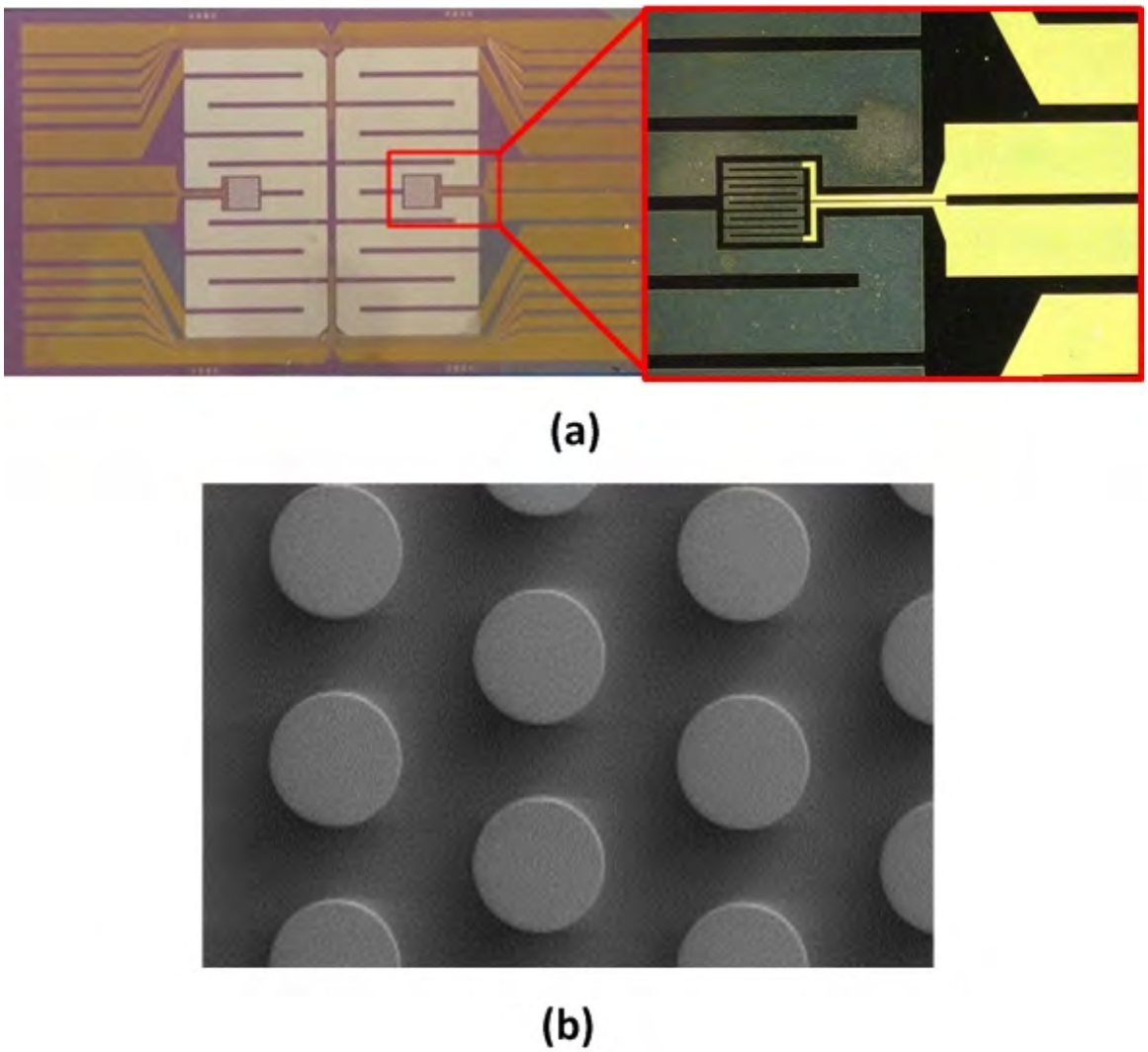


Figure 120: Key components of the bottom tier: (a) background heater and hot-spot heater on bottom tier, (b) micro pinfin structure for liquid cooling.

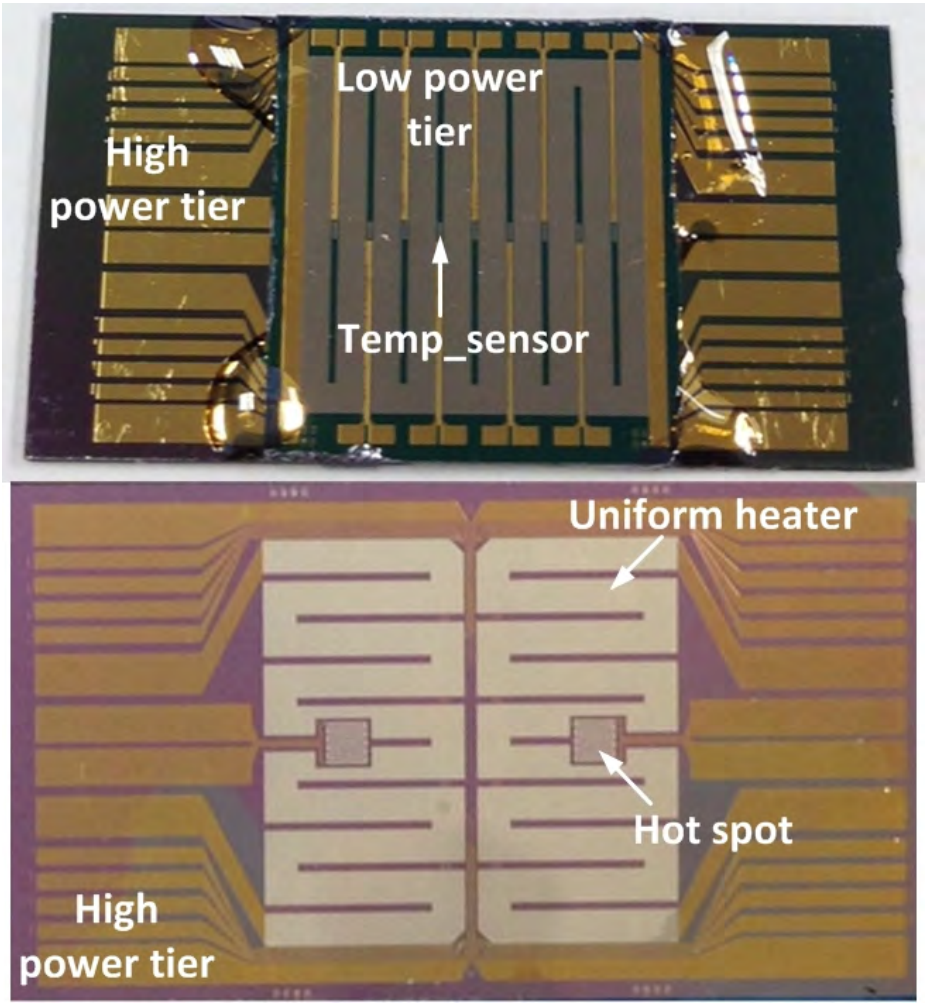


Figure 121: Assembled test bed for MFIs assisted thermal isolation (top) and the high power tier (bottom) before assembly.

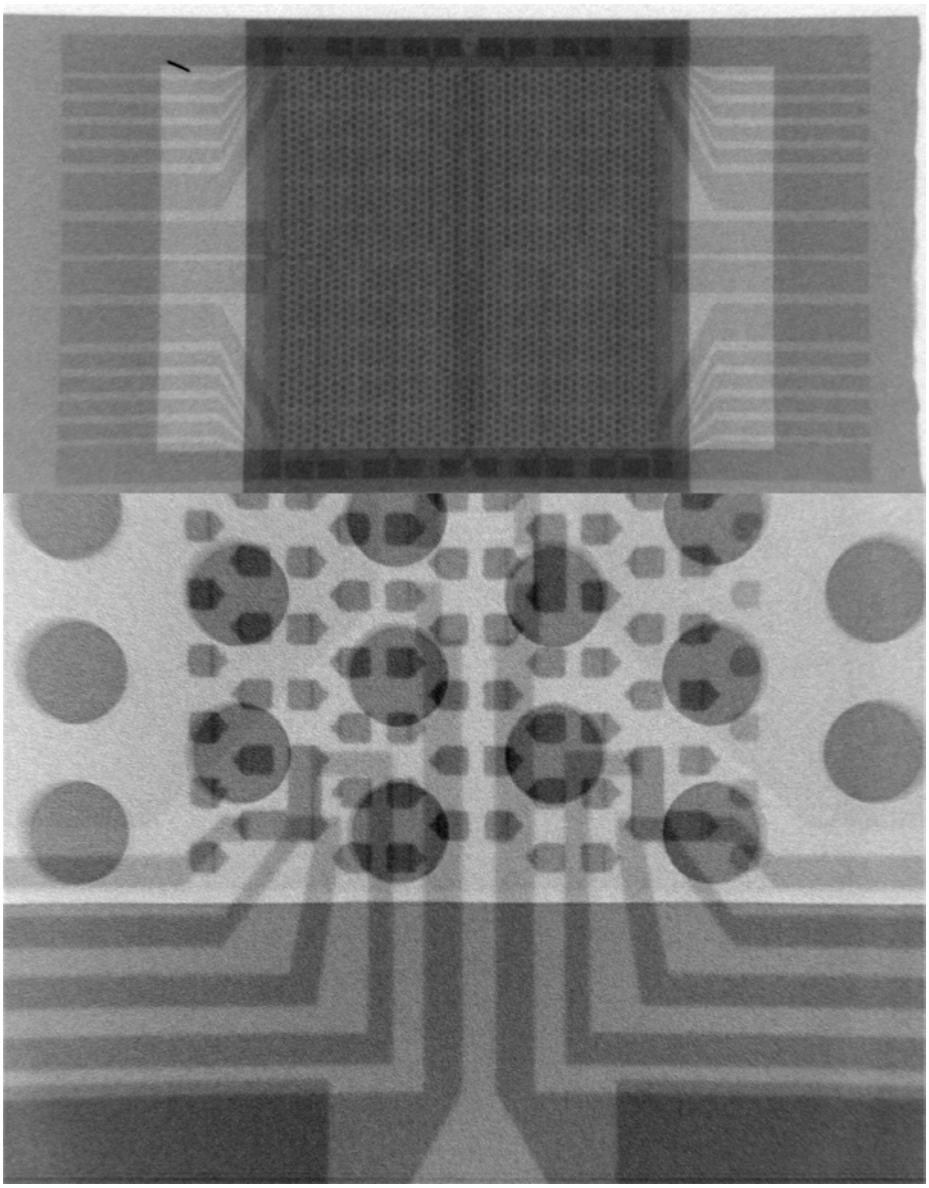


Figure 122: Xray images of assembled test bed for MFI assisted thermal isolation.

9.3.1 Electrical Measurement

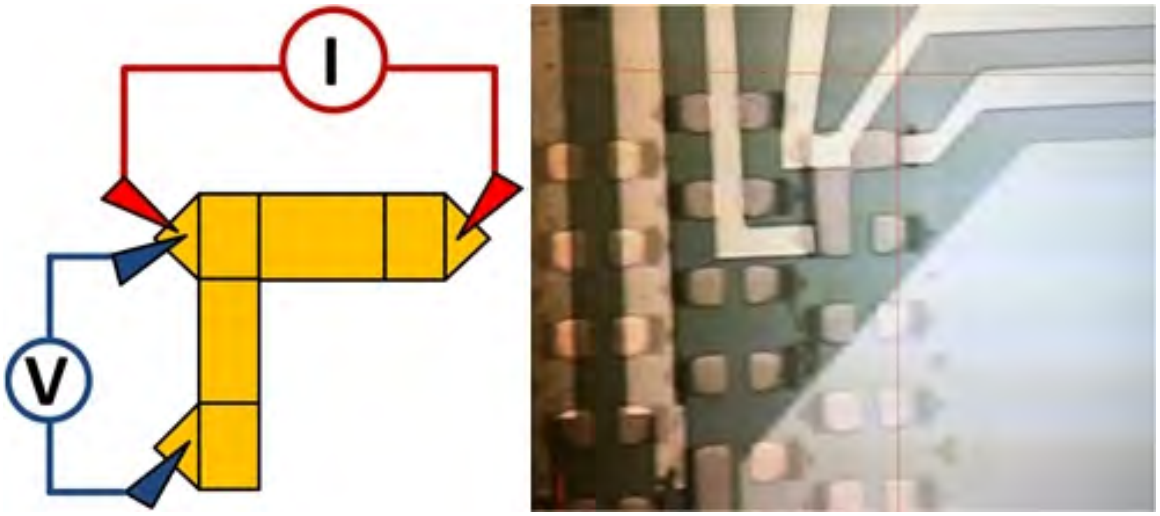


Figure 123: Four point resistance measurement structure.

Resistance measurements of the test bed are conducted to verify the electrical continuity from the top low-power tier to the bottom high-power tier. The average resistance of a single MFI measured using four-point testing (Figure 123) is 51.6 mΩ, and the resistance of a daisy chain containing 38 MFIs is 6.315 Ω.

9.3.2 Thermal Measurement

Thermal measurements are performed as shown in Figure 124. First, the heaters/RTDs in the assembled test bed are calibrated by measuring their resistance as a function of temperature. Using this calibration, the realtime temperature can be measured by recording the heater resistance during the test. Next, the assembled test bed with calibrated heaters is attached on a PCB board using wire bonding. An Agilient N6705B power analyzer with four channels is used to power up the heaters through the PCB board. The realtime current and voltage of each heater are recorded by a data logger. Based on this recorded data, the resistance and temperature of the heaters can be calculated. In addition, when the test bed is powered on, the heat generated by the heaters on high-power tier is dissipated through the microfluidic

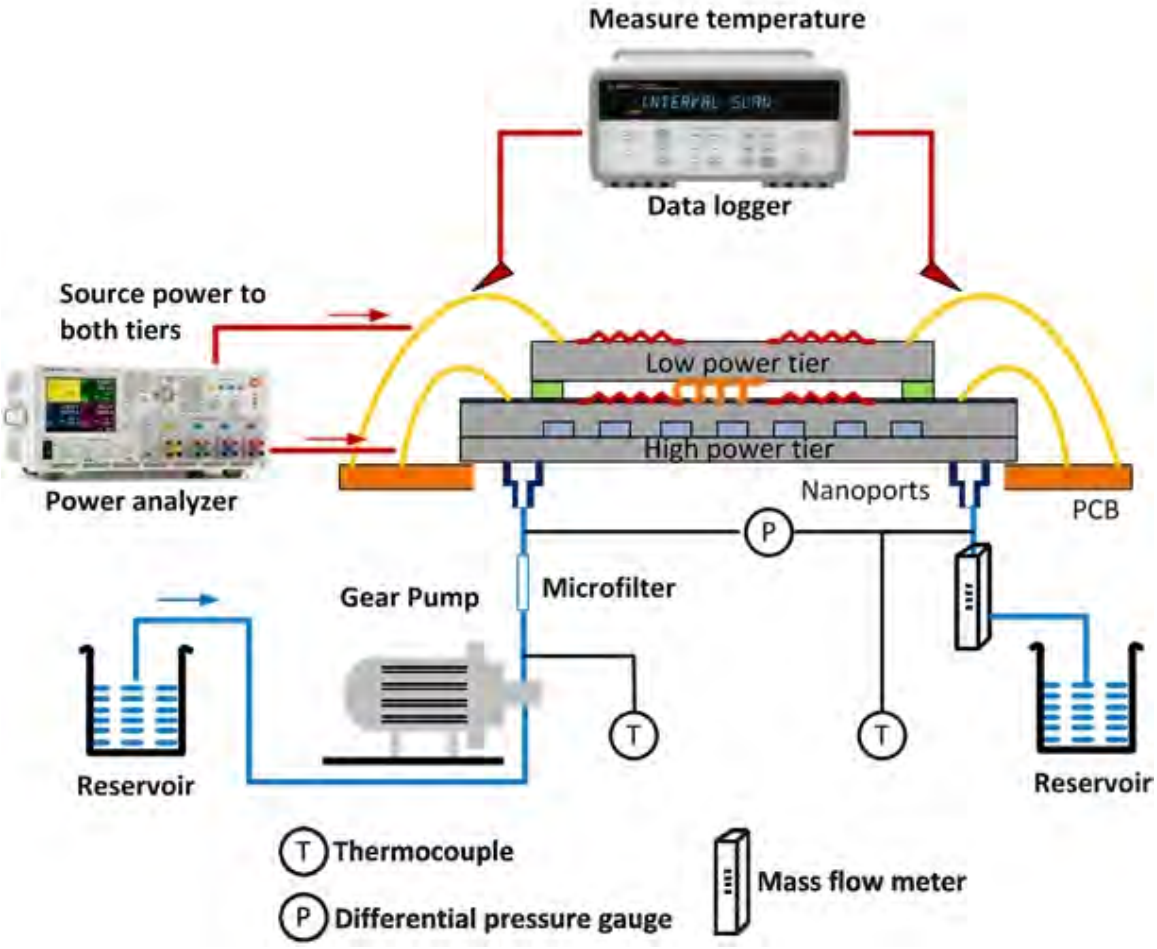


Figure 124: Test system for MFIs assisted thermal isolation demonstration.

system as well. The water is pumped out from a reservoir and into the micro pin-fin channel to cool down the bottom tier from the back side.

Table 15: Power map

	P_{btm} (W/cm^2)	$P_{btmhot}(W/cm^2)$
Uniform Case1	20	20
Uniform Case2	40	40
Hotspot Case1	40	100
Hotspot Case2	60	100

The test bed is powered with four power maps which are summarized in Table 15; P_{btm} is the power applied to the background heater on the bottom tier; P_{btmhot} is the power applied to the hotspot heater on the bottom tier. During the test, the microfluidic cooling system is operated at a flow rate of 50 ml/min. The measured temperature of the top and bottom tiers are plotted in Figure 125. T_{btm} and T_{btmhot} are the temperatures measured by the background and hotspot heaters, respectively. T_1-T_5 are the temperatures measured by the 5 RTDs on the low-power top tier (from the edge to the center, as shown in Figure 121(top)). For comparison, simulation results for a test bed with the same configuration but stacked using microbumps and underfill are plotted in Figure 126. The results are discussed as follows:

Uniform Power Map

Case 1 and 2 are the cases where the test bed is under uniform heating in which case the heaters are operated at the same power density. Two power densities are used: 20 W/cm^2 and 40 W/cm^2. For the measured test bed with MFIs assisted isolation, as shown in Figure 125, several observations can be obtained: 1) the temperature distribution is uniform on each tier; 2) the temperature on each tier increases with increasing power density; 3) there is a temperature difference between top and bottom tier (T_{btm} and T_{btmhot} are higher); and 4) the temperature difference between two tiers increases with increasing power density. Observations 1) and 2) are induced by the

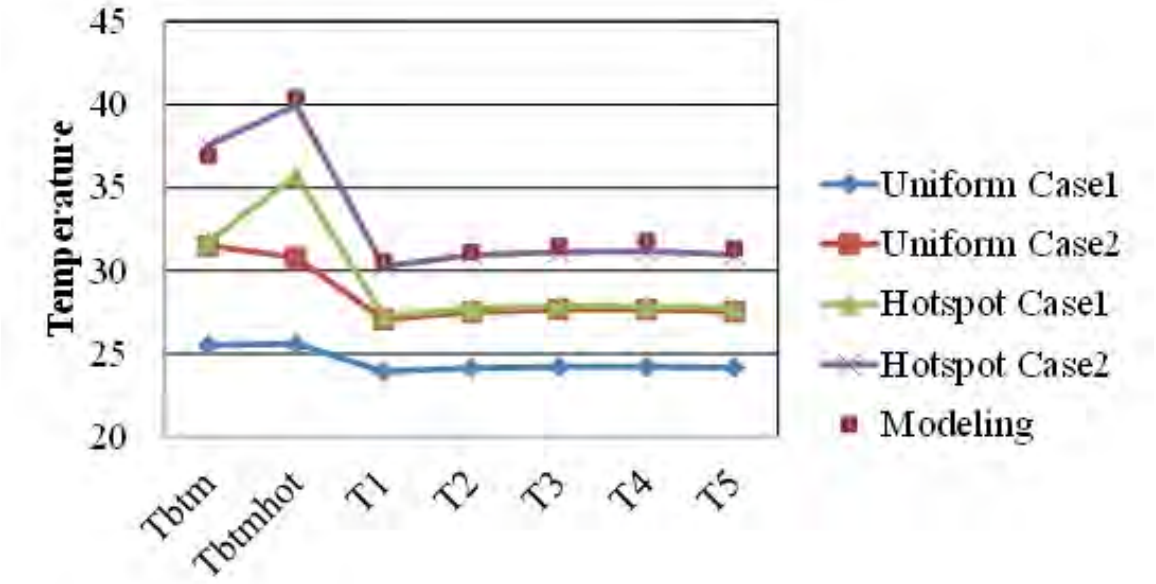


Figure 125: Measured temperature in the system with MFIs assisted thermal isolation.

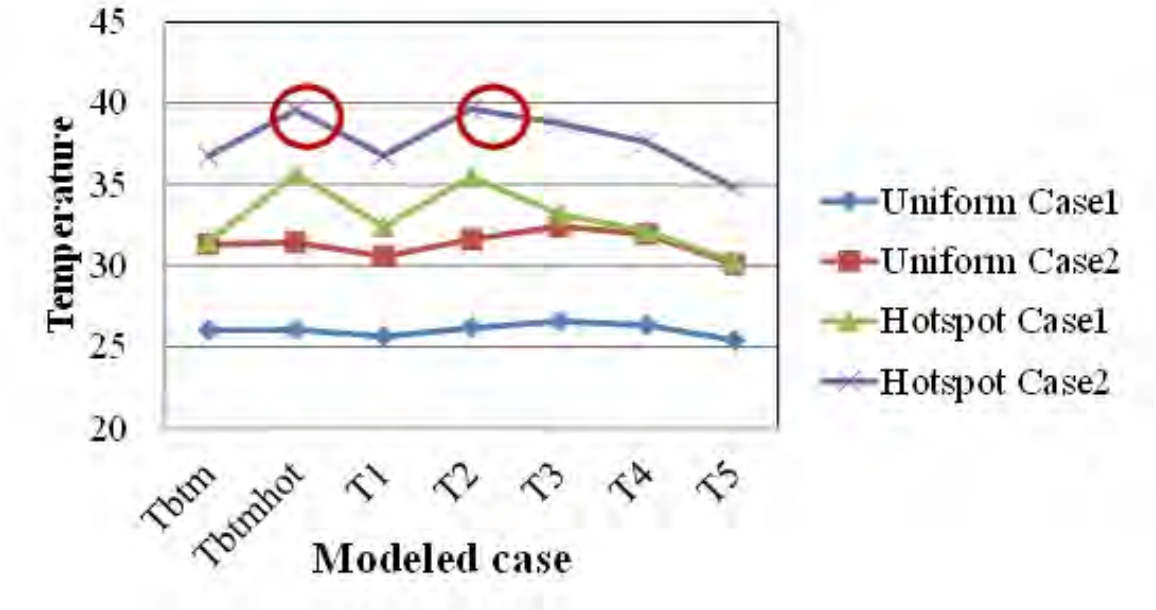


Figure 126: Simulated temperature in traditional system stacked using microbumps and underfill.

applied uniform power map, while observations 3) and 4) are induced by MFIs assisted thermal isolation. The benefits of thermal isolation become even more obvious when we examine the simulation results (Figure 126) of 3D stacks with microbumps and underfill (using same power map). The simulation results plotted in Figure 126 illustrate that there is lack of a large temperature difference between the two tiers, which indicates a strong thermal coupling.

Power Map with Hotspots

Cases 3 and 4 are the cases where the hotspots heater is active and in which case the hotspot heater has a larger power density than the background heater, as shown in Table 15. As shown in Figure 125, several observations are obtained: 1) the hot spot is observed on bottom-tier but not on top-tier ; and 2) there is a large temperature difference (up to 9°C) between $T_{hotspot}$ and T_1-T_5. These observations indicate that the top- and bottom-tiers are thermally decoupled by the MFIs assisted isolation layer. However, the simulation results for hotspot case 1 and 2 (plotted in Figure 126) show that the top-tier has been heated up and a relatively high temperature area (T_2) is observed in the top-tier, which again clearly illustrate the strong thermal coupling between the two tiers.

9.4 Conclusion

In this chapter, an MFI assisted thermal isolation technology is developed to address thermal coupling in traditional stacking approaches that use microbumps and underfill. A test bed with two tiers, separated by an air gap and electrically interconnected using MFIs is demonstrated as a proof-of-concept of MFIs assisted thermal isolation technology. The electrical continuity is verified by DC measurements performed on links connecting the two tiers. Results of the thermal measurements clearly show that the MFI assisted thermal isolation layer successfully decouples the two stacked tiers.

CHAPTER 10

CONCLUSION AND FUTURE WORK

This chapter describes the conclusion and summary of the key results and contributions of this dissertation. Two sets of contributions are accomplished in this dissertation: 1) technology development, fabrication, and characterization of various NiW MFIs technologies for a number of applications; and 2) innovative systems are proposed and demonstrated using various MFIs. In addition, possible future research directions are discussed.

10.1 Contributions

10.1.1 Advanced MFIs technology

10.1.1.1 Au-NiW MFIs

- Other than Cu, which is widely used in the previously reported flexible I/Os, in this dissertation, NiW is adopted as the material for MFIs because of its large yield strength.
- A 3D tapered profile design is optimized based on FEM analysis to ensure the inner stress of deformed MFIs does not exceed the yield strength of NiW.
- A wafer-level low-cost batch fabrication process of MFIs is developed, and the multi-coating process enlarges the sacrificial dome height therefore the vertical gap of MFIs up to 65 μm.
- The electroless gold passivation layer not only lowers the resistance but is also critical to protecting the MFIs from oxidation to preserve their mechanical and electrical characteristics.

- Mechanical properties of Au-NiW MFIs are investigated using indentation tests. The indentation test results verify the Au-NiW MFIs have up to 65 μm vertical range of motion. Four-point probing is used to measure the DC resistance of single MFI.

- Photoresist spray-coating based fabrication process is developed to successfully scale the in-line pitch of MFIs to 50 μm while maintaining a 65 μm high vertical gap.

- Indentation results indicate that at a given thickness, the compliance of the MFI decreases with the scaling of MFI footprint. Therefore, as MFI footprint scales, the optimization of MFI dimensions, especially the thickness, is critical to obtain a trade-off between electrical and mechanical performance of MFI.

10.1.1.2 Au-NiW MFIs with Contact-tip for Rematable Assembly

- Au-NiW MFIs with truncated cone contact-tip were wafer-level batch fabricated and used to demonstrate rematable assembly on various substrates. The contact tip is used to enhance the bonding pad scrubbing for reliable contact.

- Four-point resistance measurements were performed on the sample after single and ten repeated assemblies, and the measured results verify the assembly using MFIs is rematable.

- Daisy chain and current carrying capability measurements indicate that the Au-NiW MFIs form reliable interconnects and exhibit a large current carrying capability of 1 A.

- With the 30 μm high contact tip, the aggregated height of MFI is up to 105μm. Therefore, Au-NiW MFI with contact tip can enable the assembly of a silicon chip on a substrate with up to 45 μm surface variation.

10.1.1.3 Multi-pitch Multi-height Au-NiW MFIs

- The batch fabrication of multi-height dome is developed using double-lithography and double-reflow processes. Compared with the brute-force approach, the process complexity is significantly reduced.

- Multi-pitch MFIs are patterned and electroplated on the substrate with multi-height domes. After MFI releasing, the MPMH MFIs are demonstrated with up to 40 μm height variation while maintaining a scalable pitch from 150 μm to 50 μm.

- The indentation testing and four-point resistance measurements are performed for the mechanical and electrical properties characterization. With a simplified MFI design, the resistance of low profile MFI is lowered to 37.6 mΩ.

10.1.2 Heterogeneous System Demonstrations Using MFIs

10.1.2.1 MFIs Assisted Interposer Stacking

- A novel 3D interposer stacking system is demonstrated using MPMH MFIs technology. Compared with the traditional double-sided interposer based integration, this 3D interposer stacking system could enhance system level testability and substrate robustness, avoid the waste of silicon area and reduce routing length on bottom substrate.

- A substrate with MPMH MFIs is flip-chip bonded onto a substrate with an SU8 chip for proof-of-concept. Electrical links interconnecting the two substrates and substrate-to-SU8 chip are realized using large-profile and low-profile MFIs, respectively.

- DC electrical measurements have been performed on the links to verify the electrical continuity.

- RF probing measurements are performed on two different large profile MFIs, eMFI and mMFI. The eMFI has lower insertion loss, while the mMFI has better rematability.

- RLGC extractions are conducted on eMFI and mMFI. The extracted resistance, inductance, conductance and capacitance are valuable for the RC link design and optimization.

10.1.2.2 Bridged Multi-interposer System

- A novel 2.5D interconnection platform, bridged multi-interposer system, has been proposed to address the need for a large scale high performance heterogeneous system. In this system, multiple interposer tiles are aligned and directly assembled on an organic substrate using PSAS/pit self-alignment. Interconnections between the tiles are provided through bridges which are mounted above two or more tiles. MFIs are used to enable a reliable tile-to-bridge and tile-to-organic substrate interconnection.

- Key enabling technologies are developed: 1) Low cost accurate alignment mechanism, PSAS/Pit self-alignment; 2) MFI/TSV integration and 3) double-sided MFIs.

- A proof-of-concept system with three tiles mounted on FR4 and bridged by two chips is demonstrated. The accurate alignment between tile and bridge are calibrated by IR images. The electrical continuity is verified by DC measurements performed on link of tile/bridge/tile.

10.1.2.3 Surface Tension Assisted Ball Self Population

- Novel methods of using a hydrophobic and hydrophilic pattern to achieve large-scale ball-in-pit self-population are developed.

- The populated ball-in-pit structures would be employed for achieving submicron layer-to-layer alignment, for example in a multi-chip package that employs PxC chip-to-chip interconnects.

- The demonstrated key features are: 1) a process for lithography-free hydrophobic/hydrophilic pattern formation and removal, 2) a surface tension assisted, pit pattern independent, scanning approach for ball-in-pit population, which is also capable of rework.

10.1.2.4 MFIs for Thermal Isolation

- A test bed with two tiers, separated by an air gap and electrically interconnected using MFIs is demonstrated as a proof-of-concept of MFIs assisted thermal isolation technology.

- The top low power tier and the bottom high power tier represent DRAM chip and CPU respectively. Heaters are fabricated on both tiers to create the designed system power map. Micro-fluidic cooling structures are fabricated on the backside of high power tier for excellent thermal dissipation.

- Links connecting the two tiers are enabled by MFIs, the electrical continuity of which is verified by DC measurements.

- Results of thermal measurements clearly show that the MFIs assisted thermal isolation layer successfully decouples the two stacked tiers.

10.2 Future Work

The possible extensions of the research described in this dissertation are described in this section. First, the opportunities to realize a high performance electronic system using the bridged multi-interposer platform and fine pitch MFIs are outlined. In

addition, an advanced testing system enabled by the MPMH MFIs and MFI/TSV integration is proposed.

10.2.1 High performance Interconnection Platform

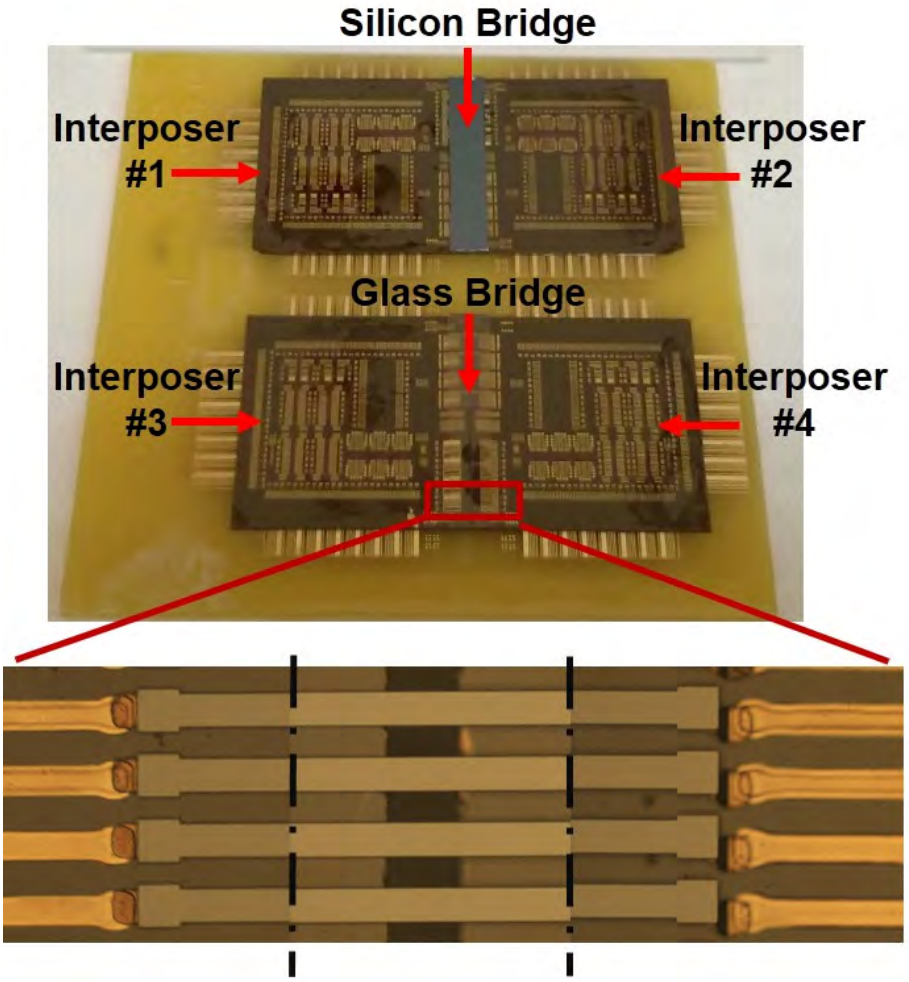


Figure 127: The bridged multi-interposer system using double-sided MFIs.

The proof-of-concept demonstration of bridged multi-interposer system was reported in Section 7.3. However, MFIs are only located on the top side of the interposer tile to demonstrate the bridge concept. Figure 127 shows the assembled bridged-interposer system using double-sided MFIs in which the low profile MFIs with fine pitch are used to enable the interposer tile-to-bridge interconnection, and the large

profile MFIs with coarse pitch are used to enable the interposer tile-to-organic substrate interconnection. The RF measurement results of the tile/bridge/tile electronic link are shown in Figure 128 as well. These RF results demonstrate the electrical continuity through bridge but the link insertion loss is too high. The possible extensions to fully demonstrate the envisioned high performance interconnection platform, as shown in Figure 88, are listed as follows.

10.2.1.1 Co-fabrication of MFIs, TSVs, and Pits

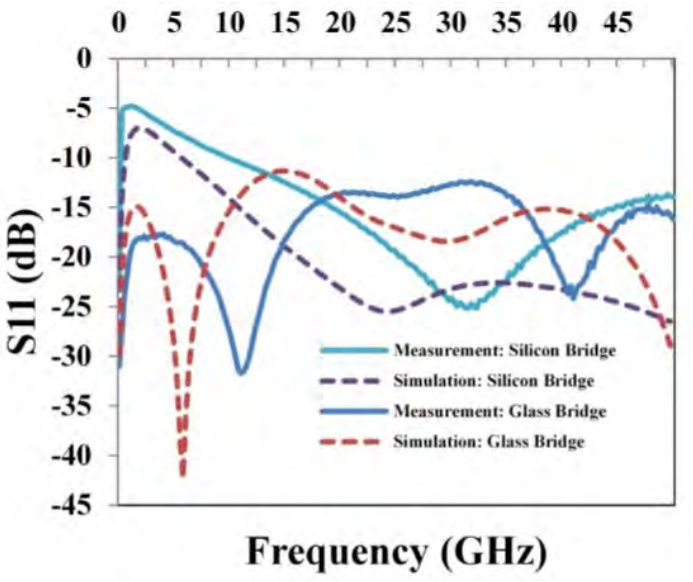
One feasible configuration to demonstrate our envisioned system in Chapter 1 is shown in Figure89. Therefore, the co-fabrication of double-sided MFIs, TSVs and pits is the most critical step. To simplify the fabrication complexity and avoid potential process damage, one possible fabrication process is shown in Figure 129: The most harsh process, double-sided pits etching should be performed first; in addition, TSVs fabrication should be completed; at last, double-sided MFIs processes are performed. Photoresist protection layer could be used to protect the pits during the TSV process such as via etching and chemical mechanical polishing.

10.2.1.2 Low Loss Electronic Link Design

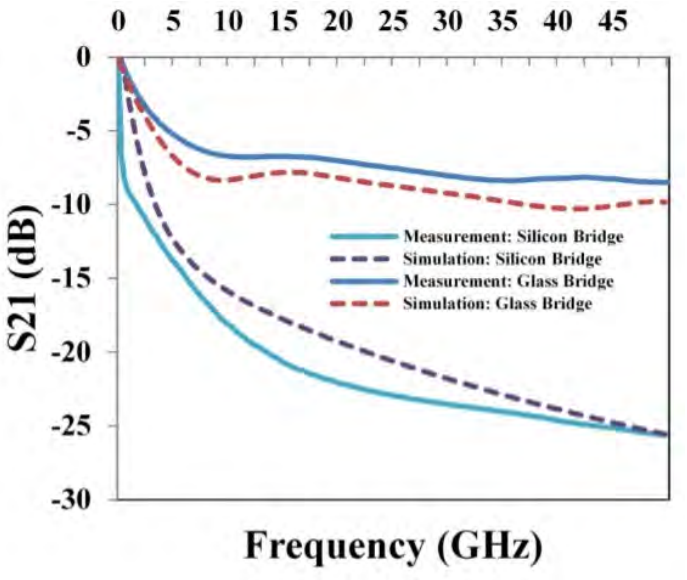
The electric traces used to get the RF measurements are approximately 5 mm long and not optimized for RF tests. In order to demonstrate a low loss electrical link, link optimization especially for the traces is essential. One low-loss transmission line design could be adopted is micro-strip with coplanar ground, as shown in Figure 130. The conductive background layer could significantly reduce the loss by reducing the coupling between the traces and the silicon substrate. In addition, to get the real-time RF characterization of the link, such as the eye-diagram measurement, impedance matched link design is essential.

10.2.1.3 RF Characterization of MFIs

Besides the system-level fabrication challenges and link design issues, the MFI characterization is also important. For example, the precise electrical characterizations of MFIs, especially RF measurement and RLGC extraction, are critical to design a



(a)



(b)

Figure 128: RF measurement of bridged two interposers

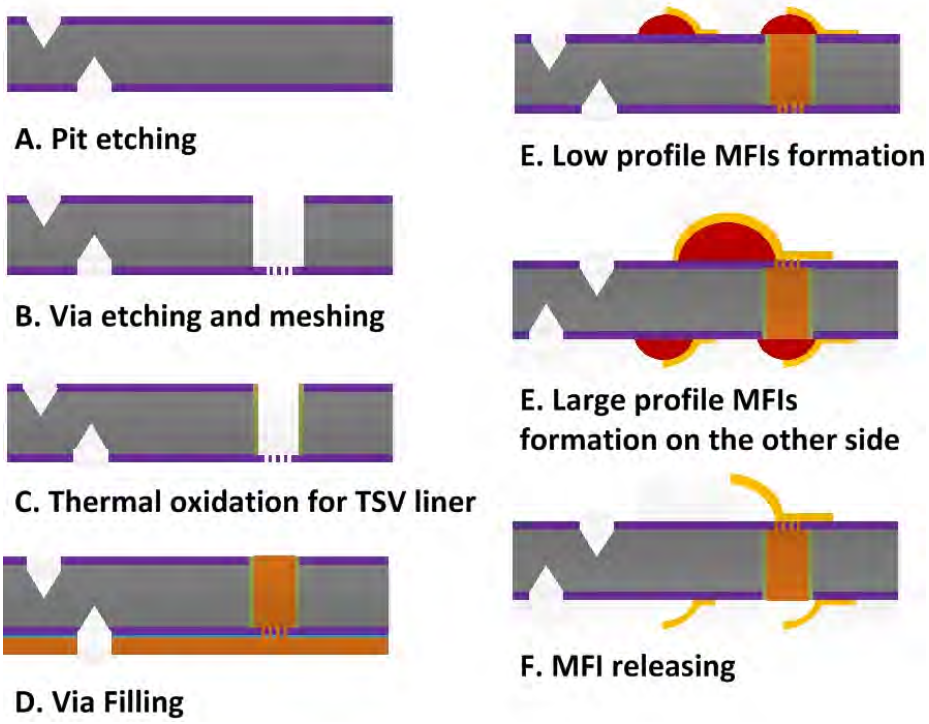


Figure 129: Co-fabrication of MFIs, TSVs and Pits.

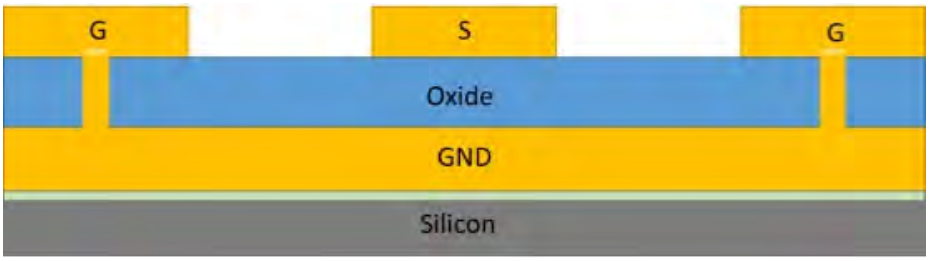


Figure 130: Potential low loss transmission line design: micro-strip with coplanar ground transmission line.

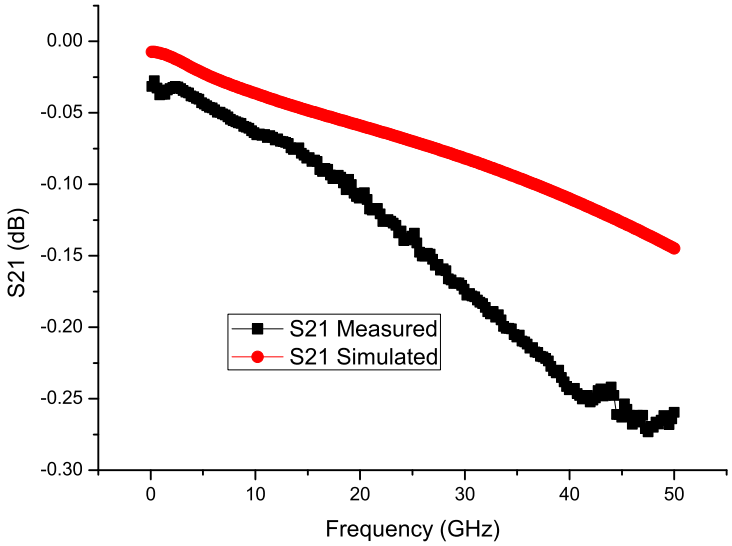


Figure 131: RF probing on fine pitch MFIs (preliminary results).

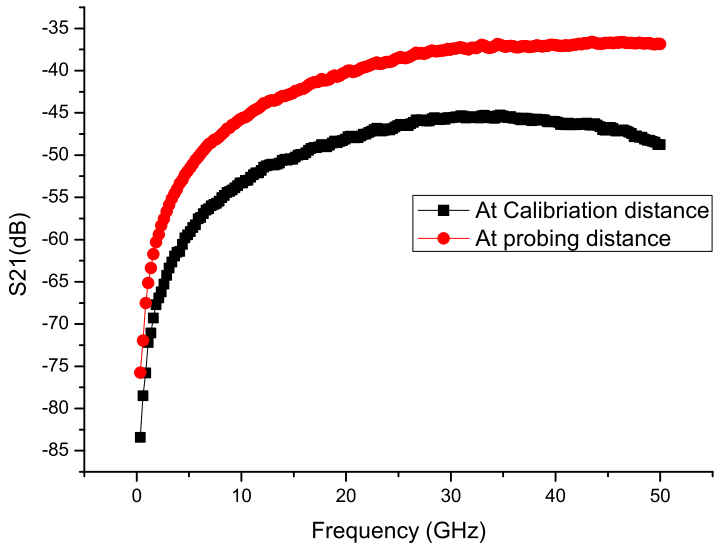


Figure 132: Tip coupling issue for RF probing on fine pitch MFIs.

impedance matched link. As reported in Section 6.4.2, RF probing is used to characterize the RF performance of large profile MFIs. However, as the MFI footprint scales, if the probing distance between two probes is smaller than the calibration distance, which could be true for probing on fine pitch MFIs, the RF probing results might not be accurate due to the strong coupling between the two probes. Figure 131 shows the RF probing results on low profile MFIs on 50 μm pitch. The probing distance between two probes is approximately 50 μm, which is much shorter than the calibration distance. The effect of coupling between two probes as a function of distance is shown in Figure 132, where the measured S21 from two suspending probes at probing distance is much smaller than the the results from the same probes at calibration distance.

10.2.2 Advanced Testing System

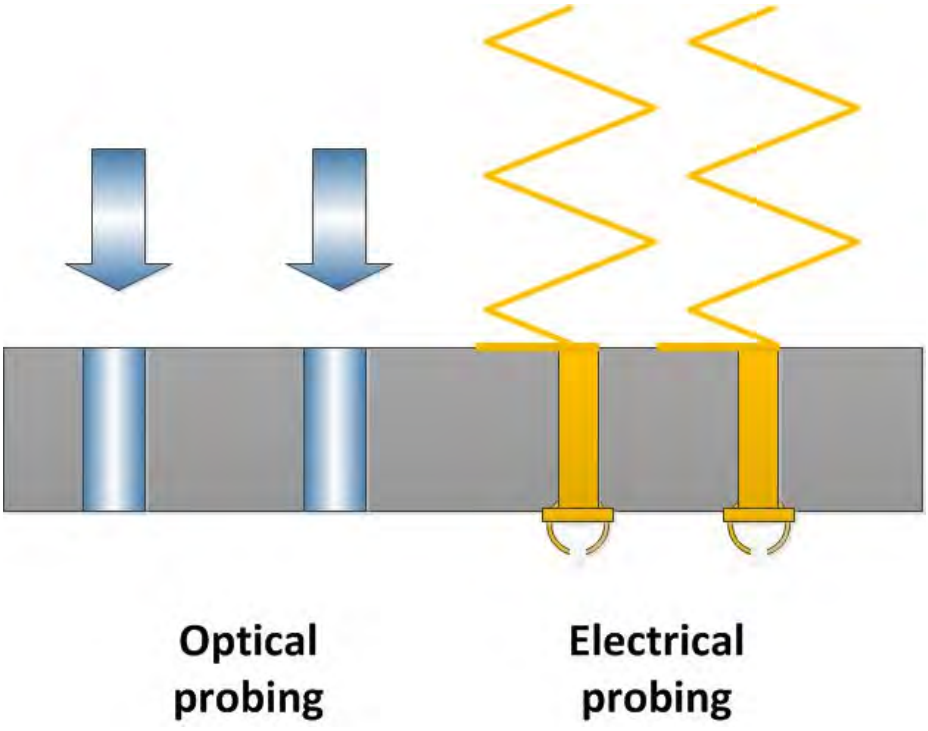


Figure 133: Advanced electrical and optical co-testing system.

Silicon photonics recently has been emerged as a promising low-loss high-bandwidth

interconnection technology for high performance computing system. However, the photonic and electronic portions are traditionally tested separately. There is a huge lack of large scale optical and electrical co-testing capability to improve system yield and performance. Since all MFIs technologies described in this thesis are CMOS compatible, an electrical and optical co-testing system is feasible by integrating optical waveguide and other silicon photonic devices, as shown in Figure 133.

10.3 Conclusion

Wafer-level batch fabricated novel mechanically flexible interconnects (MFIs) have been designed, fabricated and demonstrated in this dissertation. First, because of the large yield strength and low-cost batch deposition capability, NiW is selected as the material for flexible interconnects with a large vertical range of motion. Next, following the principles described in Section 2.3, 3D tapered geometry is optimized using FEM simulation. Moreover, wafer-level batch fabrication process is developed to realize the 3D free standing NiW MFIs. Electroless gold passivation is adopted to lower the resistance as well as protect the MFIs from oxidation. The results of indentation and resistance measurements illustrate that the reported Au-NiW MFI has up to 65 μm vertical range of motion, approximately 10 mN contact force and enhanced life time during field storage. Photoresist spray-coating is introduced to scale the in-line pitch of MFIs from 150 μm to 50 μm while maintaining 65 μm vertical gap. By adding a contact-tip, Au-NiW MFI could realize a rematable assembly on a uniform surface and robust assembly on a surface with 45 μm variation. The last advanced MFI technology reported in this dissertation is MPMH MFIs technology, which can form an MFI array containing MFIs with various heights (up to 40 μm) and various pitches (from 150 μm to 50 μm). MPMH MFIs are fabricated using double-lithography and double-reflow processes which are comparable with uniform MFI fabrication in terms of process complexity and yield.

Using these advanced MFIs along with other advanced packaging technologies, three novel heterogeneous systems have been demonstrated. 3D interposer stacking is demonstrated using MPMH MFIs technology. Bridged multi-interposer system is demonstrated to exceed the reticle and yield limitation of realizing large scale system using current 2.5D integration technology. The high-bandwidth low-loss interconnection within interposer can be extended by using bridge chips. Key enabling technologies and a proof-of-concept demonstration contianing three tiles and two bridges are demonstrated. Finally, MFIs are used as an electrical interconnect in a thermal isolation technology. The thermal measurements clearly show that such MFIs assist isolation can thermally decouple the stacked chips.

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