Novel Doherty Power Amplifier Design for Advanced Communication Systems

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Abstract

As modern communication system demands higher spectrum efficiency and data rate, new communication standard using complex modulation scheme has emerged and led to transmitting signal with ever-increasing Peak-to-Average Power Ratio (PAPR). Moreover, the co-existence of different standards requires RF transceivers to support signal transmission at multiple carrier frequencies. Therefore, wideband operation and efficient amplification of high PAPR signal are prime requirements for base-station PA design.

For efficiency enhancement, the Doherty Power Amplifier (DPA) [1] has been regarded as the most popular approach due to its circuit simplicity and moderate linearity. Three innovative DPA design techniques relating to the enhancement of operating bandwidth, high efficiency range and power utilization factor (PUF) are proposed in this work.

In the first demonstration, a novel DPA configuration with Complex Combining Load (CCL) is presented to extend the high efficiency range of the amplifier. Theoretical analysis of dynamic load span, current ratio and drain efficiency reveals that complex combining load can offer a new degree of freedom to boost the Output Back-off (OBO) of DPA. For verification, a 2GHz, equal-cell, GaN HEMT-based DPA is simulated, prototyped and measured with both complex and resistive combining loads. Under Continuous Wave (CW) excitation, measurement results show that the CCL DPA can attain an OBO of 9.1 dB which is 3.6 dB higher than that of the RCL design. In addition, by the use of single-carrier WCDMA signal with

PAPR of 9.6 dB and at an average output power of 33.2 dBm, the CCL design is found to deliver an average drain efficiency of 57.4%.

The second design presents a novel technique to extend the bandwidth and efficiency range of DPA by the adoption of frequency-varying Complex Combining Load and proper input current control strategy. For verification, a 42 dBm, 1.8-2.2 GHz DPA with OBO of 8.5 dB was designed, built and characterized. Under CW stimulation, a back-off efficiency (8.5 dB) of 55-59% and saturation efficiency of 69-73% were observed over the entire bandwidth. With single carrier WCDMA signal excitation (PAPR of 9.6 dB), an average drain efficiency of 53-58% was obtained at 33.5 dBm average output power and Adjacent Channel Leakage Power Ratio (ACLR) of around -30 dBc.

In the last technique, a novel DPA configuration with auxiliary transformer is presented for broadband operation. Theoretical analysis reveals that the presented design can offer enhanced PUF and wideband Doherty behavior. Based on the proposed theory, a 1.6-2.4 GHz, 20 W DPA with improved PUF is designed, simulated and measured. Under CW excitation, measurement results indicate that the presented DPA can achieve a PUF of 0.94, good Doherty behavior over the entire frequency band with a 6 dB back-off efficiency of 55-64% and saturated efficiency of 68-76%. In addition, by the use of single-carrier WCDMA signal (centered at 2 GHz) with PAPR of 6.6 dB and at an average output power of 37 dBm, an average drain efficiency of 56% is obtained with ACLR of better than – 37 dBc.

摘要

随着无线通信的蓬勃发展，新的通信标准不断出现，频谱利用率和数据传输速率提高的同时，传输信号的带宽和均峰比也不断增加。此外，多种通信标准共存的现状要求收发机能够在多个载波频率，高效率地传输不同格式的信号。因此，宽带运行和高效的放大高均峰比信号成为了基站功率放大器设计的基本要求。

Doherty 功率放大器结构简单，增加效率的同时能保持中等线性度，故而受到了广泛关注。本文囊括了三个有关增加 Doherty 放大器工作带宽、延展高效率区或提高功率利用因子的创新设计。

第一个设计中，复数合路阻抗被用于扩宽 Doherty 放大器的高效率区。关于动态阻抗范围，电流比因子和漏极效率的理论分析说明，复数合路阻抗可以当作新的自由度来增加放大器的高效率区。为了验证有关理论，以 2GHz 为工作频点，我们使用了相同的基于 GaN 工艺的晶体管，分别设计了使用复数合路阻抗和纯实数合路阻抗的 Doherty 放大器。连续波测试结果显示，使用复数合路阻抗的 Dohety 放大器能够提高 9.1dB 的输出回退范围，比基于纯实数合路阻抗的传统设计要高 3.6dB。此外，使用单载波、均峰比 9.6dB 的 WCDMA 信号的测试显示，基于复数合路阻抗的设计在输出功率为 33.2dBm 时，其平均漏极效率高达 57.4%。

第二个设计中使用了随频率变化的复数合路阻抗，通过控制漏极电流，来同时增加 Doherty 放大器的工作带宽和高效率区。为了验证有关理论，我们设计了输出功率 42dBm、工作带宽 1.8-2.2GHz、输出回退区 9dB 的 Doherty 放大器。连续波测试结果显示，在 8.5dB 回退点处，该设计在 8.5dB 回退点和饱和

输出点的漏极效率分别高达 55-59%和 69-73%。使用单载波、均峰比 9.6dB 的 WCDMA 信号的测试显示，该设计在输出功率为 33.5dBm 时，其平均漏极效率高达 53-58%，邻道抑制比也能保持在-30dBc。

最后一个设计中，一种在辅助支路加入变换器的 Doherty 结构被用于宽带放大。理论分析显示了该结构能够增加功率利用因子，并提供宽带 Doherty 特性。为了验证有关理论，我们设计了输出功率 20W、工作带宽 1.6-2.4GHz、功率利用因子得到改善的 Doherty 放大器。连续波测试结果显示，该设计的功率利用因子高达 0.94，所有频点均可得到良好的 Doherty 效率特性，该设计在 6dB 回退点和饱和输出点的漏极效率分别高达 55-64%和 68-76%。在 2GHz 处，使用单载波、均峰比 6.6dB 的 WCDMA 信号的测试显示，该设计在输出功率为 37dBm 时，其平均漏极效率高达 56%，邻道抑制比低于-37dBc。

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CONTENTS

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Design Challenges of RF Power Amplifier

As the key component of transmitter (Fig. 1.1), RF power amplifier has been extensively studied for decades [1]-[3]. Ideally, a traditional PA should amplify the input signal to the desired power level, without consuming too much dc power or sacrifice of signal quality. As modern communication system evolves for higher spectrum efficiency and data transmission rate, the emergence of new communication standards with advanced signal formats lead to two major challenges in PA design, namely: 1) the efficient amplification of signal with high Peak-to-Average Power Ratio (PAPR); and 2) the support of wideband operation (wide bandwidth and multi-carrier).

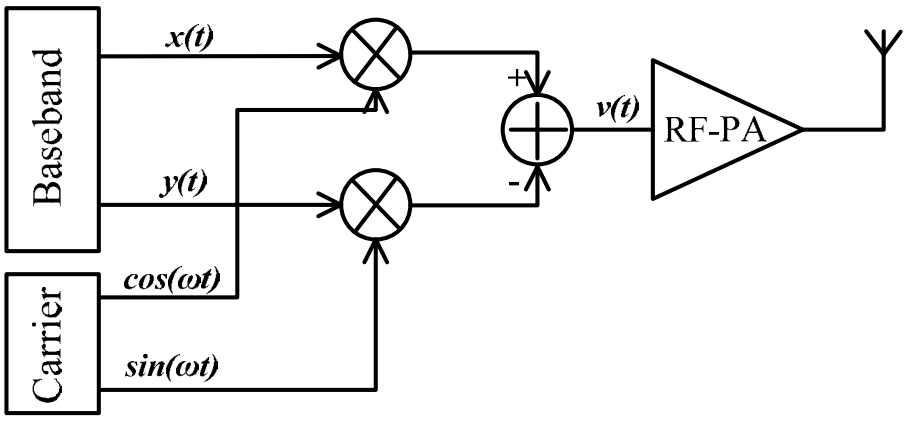


Fig. 1.1 The simplified diagram of transmitter

1.1.1 Peak-to-Average Power Ratio (PAPR)

In the study of RF PA design, one of the most important parameters is the Peak-to-Average Power Ratio (PAPR) of signals, which is defined as the ratio of signal peak power to average power. In general, the modulated signal *v(t)* can be written as:

$$v(t) = A(t) \cdot \cos[\omega t + \theta(t)] \tag{1.1}$$

where *A(t)* and *θ(t)* are the envelope and phase function of the signal. Fig. 1.2 shows the time domain waveform (envelope variation) of a typical WCDMA channel. Since the instantaneous power level (envelope) of a complex modulated signal is changing with time, the Probability Density Function (PDF) is commonly used to illustrate the energy distribution of the signal.

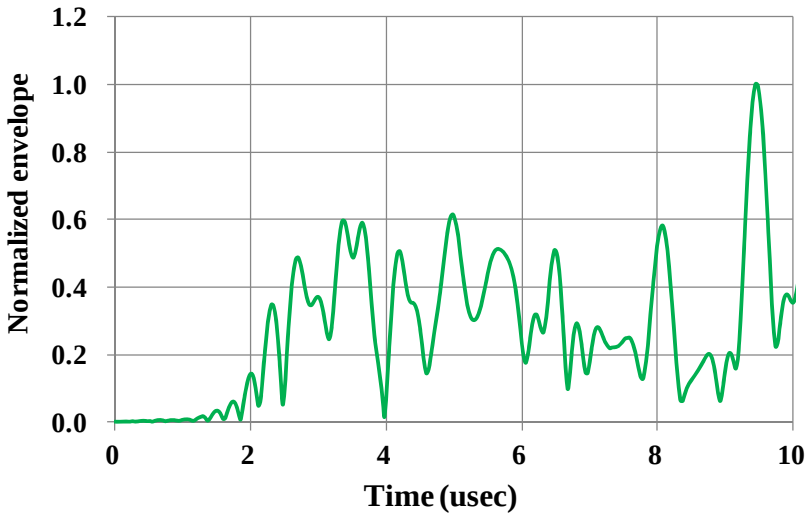
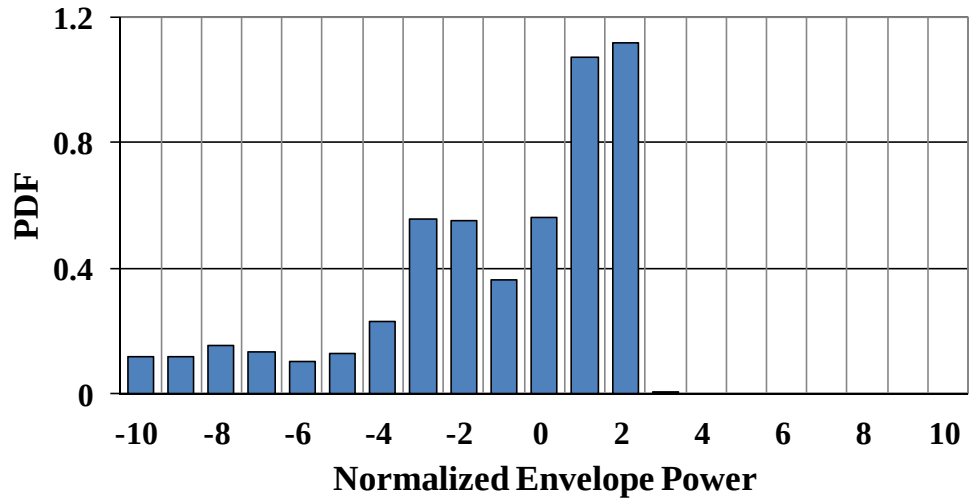
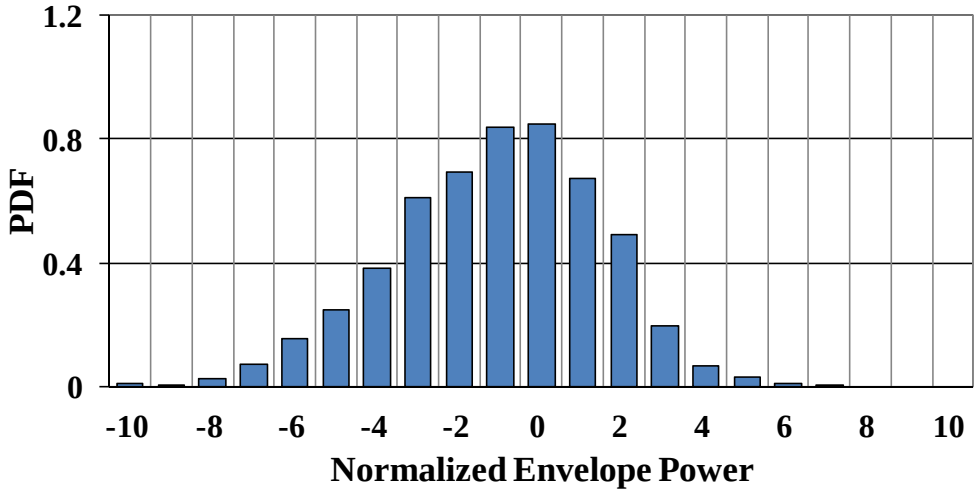


Fig. 1.2 Time domain waveform of the envelope of a typical WCDMA signal

Fig. 1.3 shows the PDF of modulated signals of various formats (EDGE, WCDMA, LTE). Although the use of signal with constant-envelope (i.e. 2G GMSK system) can largely increase the efficiency of RF PA (operating near saturation), the associated



(a)



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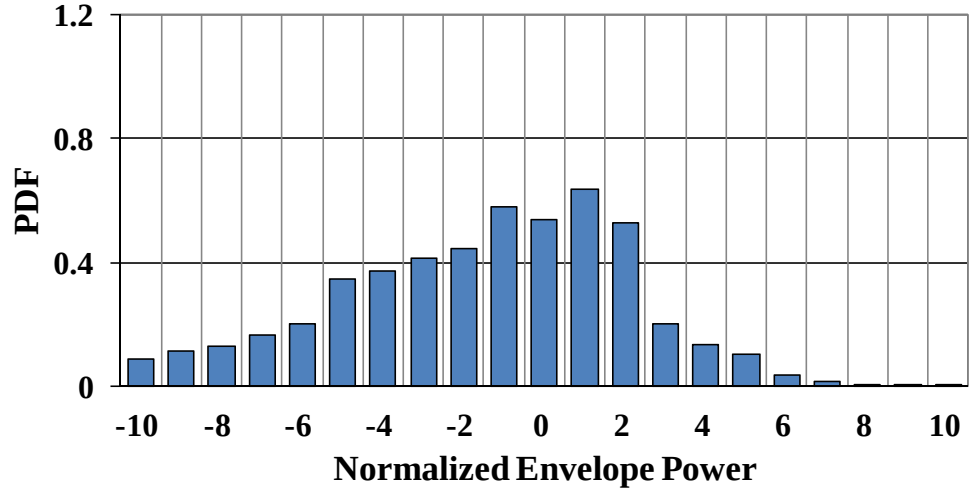


(c)

Fig. 1.3 PDF of modulated signals with various formats (envelope power normalized to average power): (a) EDGE signal; (b) WCDMA signal; (c) LTE signal.

channel capacity is rather poor (low data rate). As the mobile services become popular, the surge in data-rate demands higher spectrum efficiency as well as channel capacity. Therefore, in 2.5G EDGE system and 3G WCDMA system, advanced modulation schemes has been introduced, to improve spectrum efficiency but with the major drawback of non-zero PAPR value (3-6 dB). In the latest LTE system, the introduction of Orthogonal Frequency Division Multiplexing (OFDM) can further increase the data-rate and reduce the impact of multipath fading and interference. However, the multicarrier basis of OFDM significantly raises the value of signal PAPR to almost 10 dB.

The increased PAPR has caused a serious problem: if the modulated signal is amplified by a PA with full rated output power (maximum efficiency), the signal will be largely distorted due to the nonlinearity of PA. However, if the drive power level is backed off from the saturation (eliminate the distortion), the efficiency of PA will drop substantially, which lead to increased heat dissipation. For instance, the amplification of WCDMA signal by the conventional class AB PA (with power back-off) has an overall efficiency of below 20%. Therefore, efficient amplification of high PAPR signal has become a major challenge in PA design.

1.1.2 Wideband operation

It is well known that the available data transmission rate is proportional to signal bandwidth. Besides, the evolution of new communication standards also brings along signal with aggregated bandwidth. For example, in the LTE advanced system, the

Table 1.1
The Service Frequency Band of Various Communication Standard of China Unicom

Generation	Format	Working Band (MHz)
2G	GSM	Up link: 909-915 Down link: 954-960
2G	GSM	Up link: 1745-1755 Down link: 1840-1850
3G	WCDMA	Up link: 1940-1955 Down link: 2130-2145
4G	LTE-FDD	Up link: 1755-1765 Down link: 1850-1860
4G	LTE-FDD	Up link: 1955-1980 Down link: 2145-2170
4G	LTE-TDD	2300-2320
4G	LTE-TDD	2555-2575

signal bandwidth can be as large as 100MHz.

Moreover, due to various reasons, multiple communication standards (2G/3G/4G) will co-exist for some time. Table 1.1 lists the frequency bands of mobile service offered by China Unicom. It is clear that, signals of different formats are transmitted at different frequency bands. Therefore, a wideband PA supporting multiple communication bands can reduce hardware complexity and implementation cost (compared to one PA for each standard).

1.2 Performance Evaluation of RF Power Amplifier

Apart from the major challenges (efficiency and bandwidth mentioned above), other operation factors of PA, including output power, linearity and Power Utilization Factor (PUF), are equally essential in practice. In this section, the performance evaluation of PA is briefly summarized.

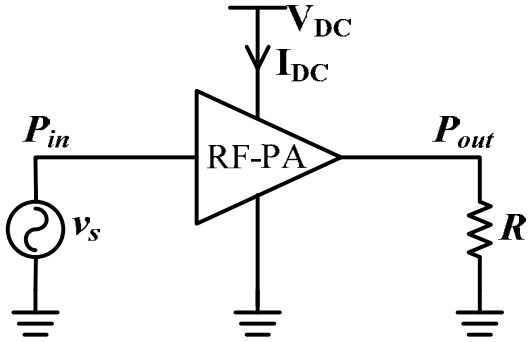


Fig. 1.4 Simplified diagram of RF PA

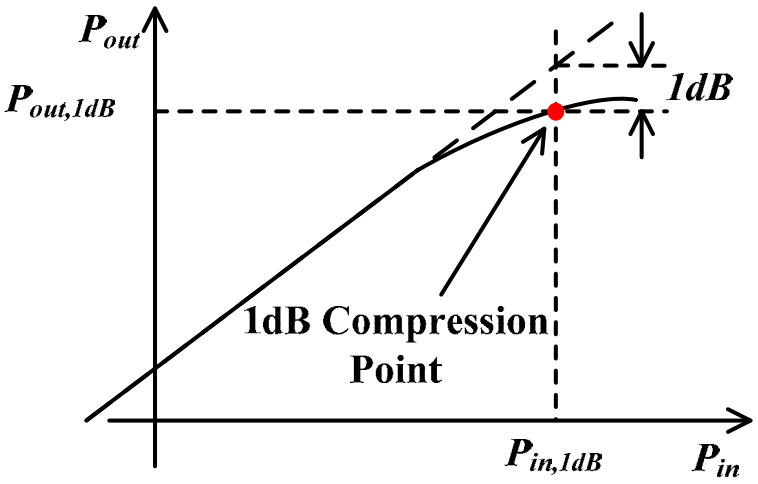


Fig. 1.5 The typical output power performance as a function of input power

1.2.1 Output power

The output power of PA normally refers to the fundamental power or the average power level over the band of interest transmitted to the load (Fig. 1.4). Fig. 1.5 depicts the typical output power performance of PA as a function of input power. The 1dB compression point ($P_{out,1dB}$) is often used to indicate the power handling capacity of PA, and is defined as (all output power are measured in dBm):

$$P_{out,linear} - P_{out,1dB} = 1dB \tag{1.2}$$

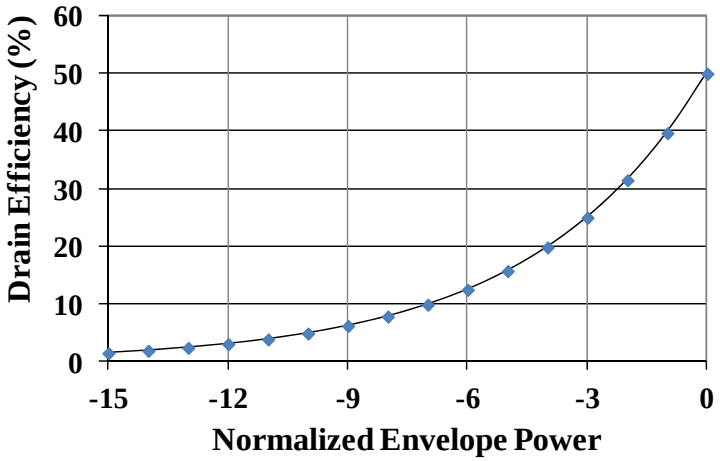


Fig. 1.6 Theoretical drain efficiency behavior of the Class A PA

1.2.2 Efficiency

An efficient PA will not only decrease power consumption, but also lower down the heat dissipation and simplify the cooling system. Therefore, efficiency has been considered as one of the most critical parameters in PA design. Referring to Fig. 1.4, the dc power consumption, Drain Efficiency (DE) and Power Added Efficiency (PAE) can be obtained by the following expressions:

$$P_{dc} = V_{dc} I_{dc} \tag{1.3}$$

$$DE = \frac{P_{out}}{P_{dc}} \tag{1.4}$$

$$PAE = \frac{P_{out} - P_{in}}{P_{dc}} \tag{1.5}$$

Fig.1.6 shows the theoretical drain efficiency behavior of class A PA under CW stimulation. For modulated signal, the average drain efficiency will depend on both efficiency curve of PA as well as the probability distribution function of the transmitted signal:

$$Average\ DE = \int_0^{P_{MAX}} DE(p) \cdot PDF(p) \cdot dp \tag{1.6}$$

As shown in Fig. 1.7, the average drain efficiency of conventional class A PA with WCDMA signal excitation (6dB PAPR) is only 12%.

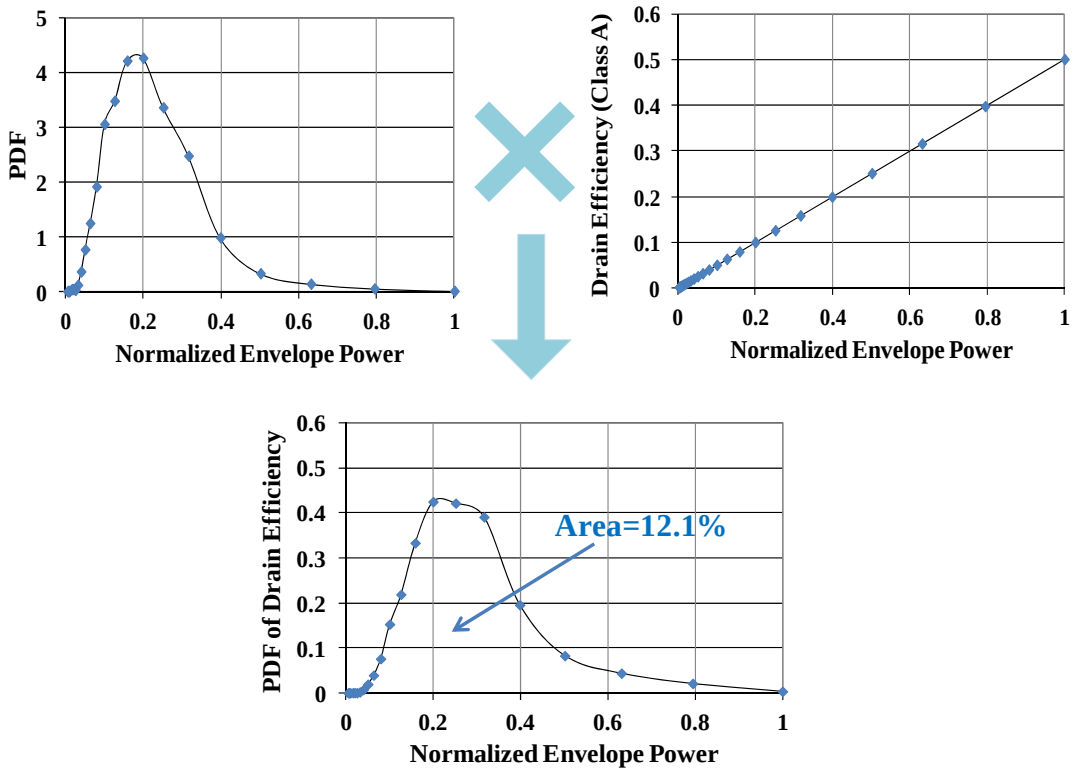


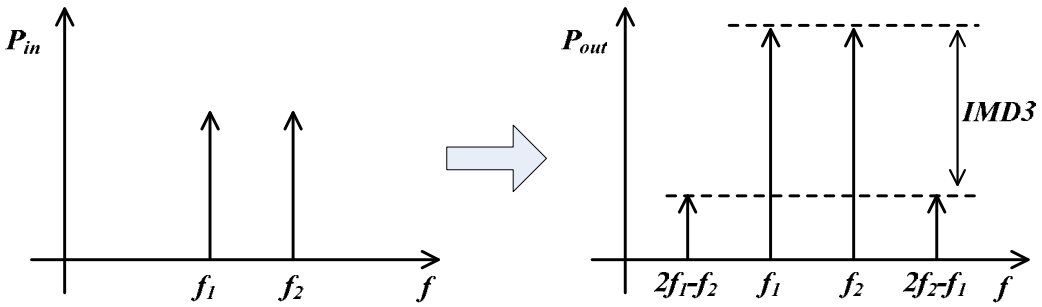
Fig. 1.7 Evaluation of average drain efficiency under modulated signal

1.2.3 Linearity

Due to the nonlinear characteristics of transistors, distortion component (IMD) will be generated at the output of PA. Third order Inter-modulation Distortion (IMD3) is commonly used to characterize the linearity of PA. Under a two-tone input signal (Fig. 1.8), IMD3 is defined as:

$$IMD3_L = P_{out}(f_1) - P_{out}(2f_1 - f_2) \tag{1.7}$$

$$IMD3_H = P_{out}(f_2) - P_{out}(2f_2 - f_1) \tag{1.8}$$



(a) (b)

Fig. 1.8 Input and output spectrum of PA (Two-tone test): (a) Input; (b) Output.

For complex modulated signal test, Adjacent Channel Leakage Ratio (ACLR) is introduced to account for the effect of spectrum re-growth (Fig.1.9). It is defined as the ratio between the regenerated power in the adjacent channel and the power of desired signal:

$$ACLR_{L(H)} = \frac{\int_{L(H)} P_{out}(f) \cdot df}{\int_{B} P_{out}(f) \cdot df} \tag{1.9}$$

Based on the spectrum shown in Fig.1.9, the corresponding values of ACLR (low and upper bands) are evaluated and listed in Table 1.2.

1.2.4 Power Utilization Factor

Since the microwave transistor is usually considered to be the most expensive component in PA construction, the full utilization of device capacity is thus highly desirable. Consequently, Power Utilization Factor (PUF) [1], is introduced as a measure of the effective use of device capacity (with reference to the same device operating in class A mode):

$$PUF = \frac{P_{out(Class\ under\ study)}}{P_{out(Class\ A)}} \tag{1.10}$$

Table 1.2
Calculated ACLR Values (Fig. 1.9)

Offset (MHz)	$ACLR_L$	$ACLR_H$
5	54.9	54.9
10	64.3	64.4

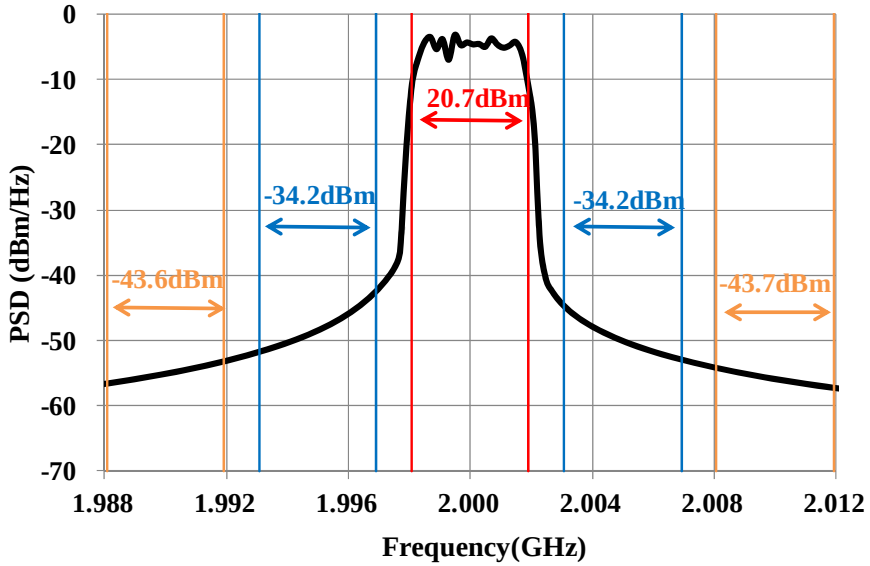


Fig. 1.9 Output Spectrum density of typical PA under complex modulated signal

P_{out} is determined by the breakdown voltage (V_{max}), the fully open-channel drain current (I_{max}) and the operation mode of the device. For Class A operation, the maximum available power is simply given by (maximum fundamental voltage and current swing of $V_{max}/2$ and $I_{max}/2$):

$$P_{out(Class\ A)} = \frac{V_{\max} I_{\max}}{8} \tag{1.11}$$

For cost effectiveness, the PUF should be made as large as possible by proper selection of bias point as well as the optimal control of drain voltage and current waveforms.

1.3 Motivation and outline of this work

As introduced in Section 1.1, wideband operation and efficient amplification of high PAPR signal are prime requirements for base-station PA design. It is well known that conventional PA architectures suffer from poor overall efficiency and thus generate excessive heat dissipation. Various techniques have been proposed for efficiency enhancement, and Doherty Power Amplifier (DPA) [4] has been regarded as the most popular approach due to its circuit simplicity and moderate linearity. Although the adoption of DPA for narrowband applications with low PAPR signal has been successfully demonstrated in the past decade, two major limitations are still required to be solved for advanced communication systems:

1. Classical Doherty amplifier can offer high efficiency range of 6 dB only, which is considered to be inadequate as many modern communication standards are having signal formats with ever-increasing value of PAPR. Therefore, the high efficiency range of DPA needs to be extended for further efficiency enhancement.

2. In theory, the classical DPA configuration can achieve high efficiency at saturation over wide frequency band. However, the back-off efficiency degrades substantially due to the narrowband nature of simple quarter-wavelength transformer. In [5], a modified configuration was suggested to extend the bandwidth of DPA, but at the expense of PUF (0.5). Therefore, a wideband DPA configuration with improved PUF is highly attractive.

In this thesis, three novel ideas relating to DPA designs with extended high efficiency range or bandwidth are presented. In the first work, DPA design with

Complex Combining Load (CCL) is presented to extend the high efficiency range of DPA. With the replacement of conventional resistive combining load by complex combining load, the high efficiency region of DPA can be extended without multi-cell or asymmetrical implementation. As the fixed CCL method is not favorable for wideband operation, a new DPA design using frequency-varying CCL is exploited with special input current control. Finally, to improve PUF performance, a new DPA configuration using band-pass auxiliary transformer has been investigated. For comparison purpose, the broadband performance of the proposed and conventional topologies are analyzed and simulated. Issues relating to the realization of matching networks and optimum phase control are also addressed.

The contents are organized as follows: In chapter 2, the classical theory on high efficiency PA design is introduced. Chapter 3 reviews some resent DPA design methodologies for the enhancement of high efficiency range or bandwidth. The complex combining load method which can boost high efficiency range without the need of asymmetrical or multi-cell configuration is introduced in Chapter 4; This method is extended in Chapter 5 to include frequency varying complex combining load for improvement in the operating bandwidth; In Chapter 6, a band-pass auxiliary transformer is introduced to the design of broadband Doherty amplifier with attained PUF of almost unity. Finally, conclusions are drawn in Chapter 7 with topics for future research.

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Chapter 2

Classical Theory on High Efficiency Power Amplifier Design

This chapter covers some basic theories of traditional PA configuration, high efficiency operation modes and some commonly used efficiency enhancement techniques.

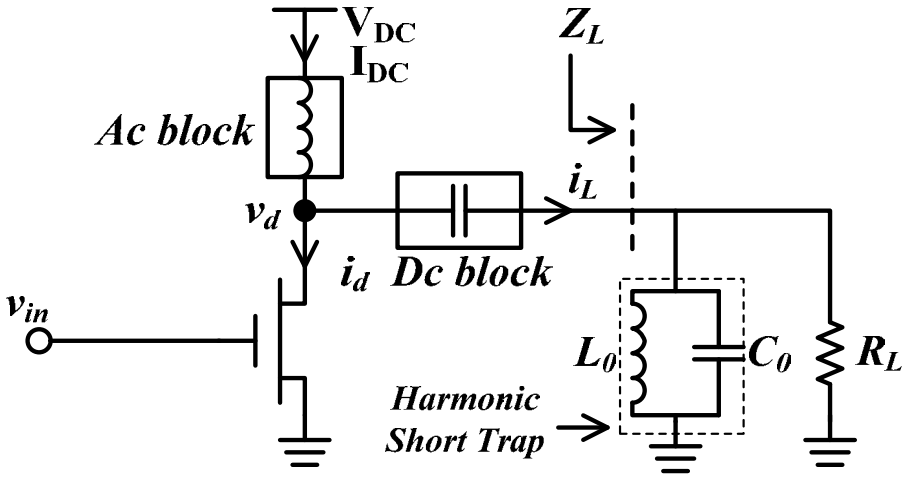


Fig. 2.1 Simplified diagram of PA

2.1 Traditional operation modes: Class A, AB, B and C

Fig. 2.1 shows the simplified circuit diagram of RF PA. The shunt LC tank is used as the harmonic trap to create a low impedance (short-circuit) for the proper drain load termination at all harmonic frequencies. As a result, we have

$$Z_L = \begin{cases} R_L & f = f_0 \\ 0 & f = 2f_0, 3f_0 \cdots \end{cases} \tag{2.1}$$

For the sake of simplicity, the following assumptions are used:

1) The drain source breaddown voltage V_{max} and fully opened channel drain current I_{max} are normalized to be 1;

2) The threshold gate voltage is assumed to be 0. The maximum drive level V_{inmax} (corresponds to saturation current I_{max}) is assumed to be 1;

3) The transistor is modeled as a voltage controlled current source with unity transconductance ($i_d=v_{in}$), zero output conductance and zero knee voltage;

Referring to Fig. **2.**2, the conventional operation modes of PA is classified by the conduction angle which represent the relative conduction time of device inside a RF cycle. For an input signal with the form of:

$$v_{in} = V_q + V_{pk}\cos(\theta) \tag{2.2}$$

where V_q, V_{pk} are the gate quiescent bias and RF swing of the input signal respectively. If the gate drive signal is always above the threshold voltage (Fig. 2.2(a)), then the transistor will conduct all the time with the conduction angle $\alpha=2\pi$. If $V_q < V_{pk}$, over a certain period of RF cycle, the gate voltage could fall to below the threshold voltage (the transistor is cut off with zero drain current). Based on the value of conduction angle, the amplifier can be classified as: class A with $a=2\pi$ (Fig. 2.2(a)), class AB with $\pi<a<2\pi$ (Fig. 2.2(b)) , class B with $\alpha=\pi$ (Fig. 2.2(c)) and class C with $a<\pi$ (Fig. 2.2(d)), and the drain current of the reduced conduction angle modes can be written as:

$$i_d = \begin{cases} I_q + I_{pk}\cos(\theta) & -\alpha/2 \le \theta \le \alpha/2 \\ 0 & \pi < \theta < -\alpha/2 \;;\alpha/2 < \theta < \pi \end{cases} \tag{2.3}$$

in which $I_{q(pk)}=V_{q(pk)}$, and $\cos(a/2)=-I_q/I_{pk}$. The gerenal expression for drain current

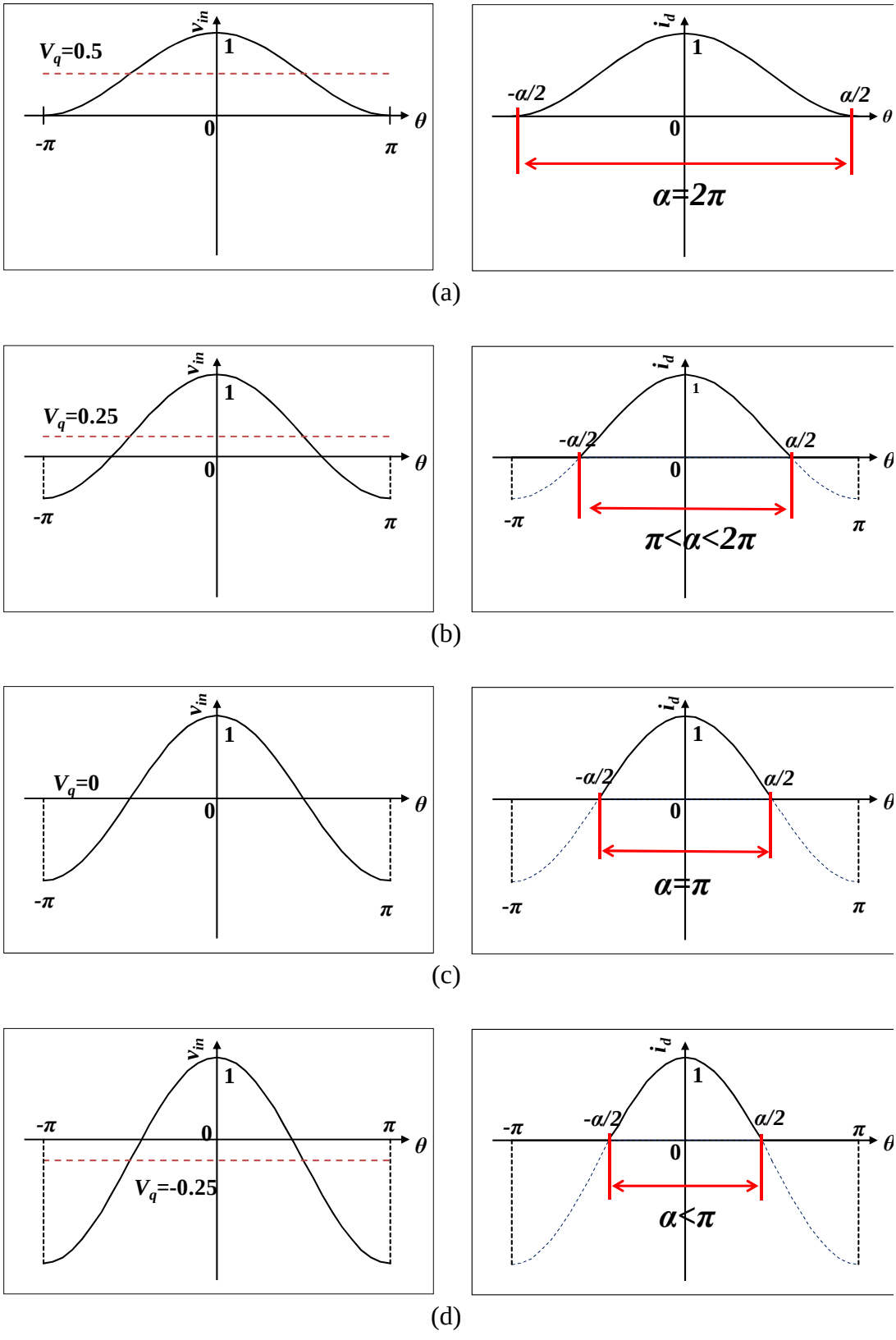


Fig. 2.2 Traditional operation modes: (a) Class A; (b) Class AB; (c) Class B; (d) Class C

(inside conduction period) can therefore be written as:

$$i_d = \frac{I_{\max}}{1-\cos(\alpha/2)}(\cos(\theta)-\cos(\alpha/2)) \tag{2.4}$$

For class A operation, it is obvious that $I_{dc}=I_1=I_{max}/2$. For the other reduced conduction angle modes, the time domain waveform of i_d are truncated sinewave, and the dc componnet, fundamental and high order harmonic component have to be extracted with Fourier Analysis:

$$I_{dc} = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2}\frac{I_{\max}}{1-\cos(\alpha/2)}\cdot(\cos(\theta)-\cos(\alpha/2))d\theta \tag{2.5}$$

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2}\frac{I_{\max}}{1-\cos(\alpha/2)}\cdot(\cos(\theta)-\cos(\alpha/2))\cdot\cos(n\theta)d\theta \tag{2.6}$$

Fig. 2.3 shows the plots of I_{dc} and I_n (n=1, 2, ⋯ 5) as a function of α. Subsequently, the drain voltage can be expressed as:

$$v_{ds} = V_{DC} - i_d Z_L = V_{DC} - I_1 R_L \cos(\theta) = V_{DC} - V_{d1}\cos(\theta) \tag{2.7}$$

where V_{d1} is the fundamental drain voltage swing. Consider that v_{ds} should be confined in [0, V_{max}], to maximize output power we have:

$$V_{DC} = V_{d1} = V_{\max}/2 \tag{2.8}$$

Subsequently, the optimum drain load for maximum output power is given by:

$$R_{opt} = V_{DC}/I_1 \tag{2.9}$$

Finally, the output power, dc consumption and drain efficiency can be calculated as follows:

$$P_{out} = V_{d1}I_1/2 \tag{2.10}$$

$$P_{dc} = V_{DC}I_{DC} \tag{2.11}$$

$$DE = P_{out}/P_{dc} \tag{2.12}$$

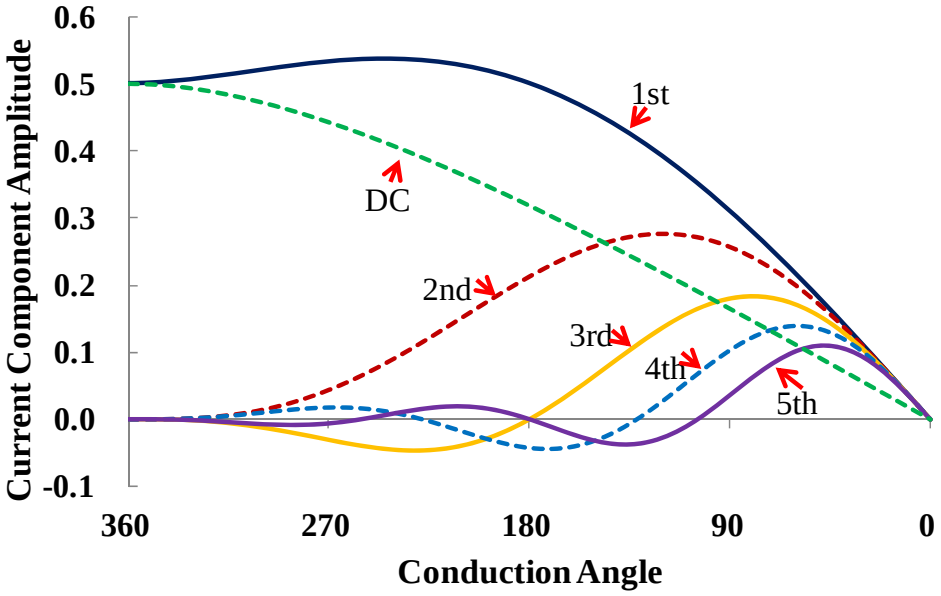


Fig. 2.3 Fourier analysis of drain current

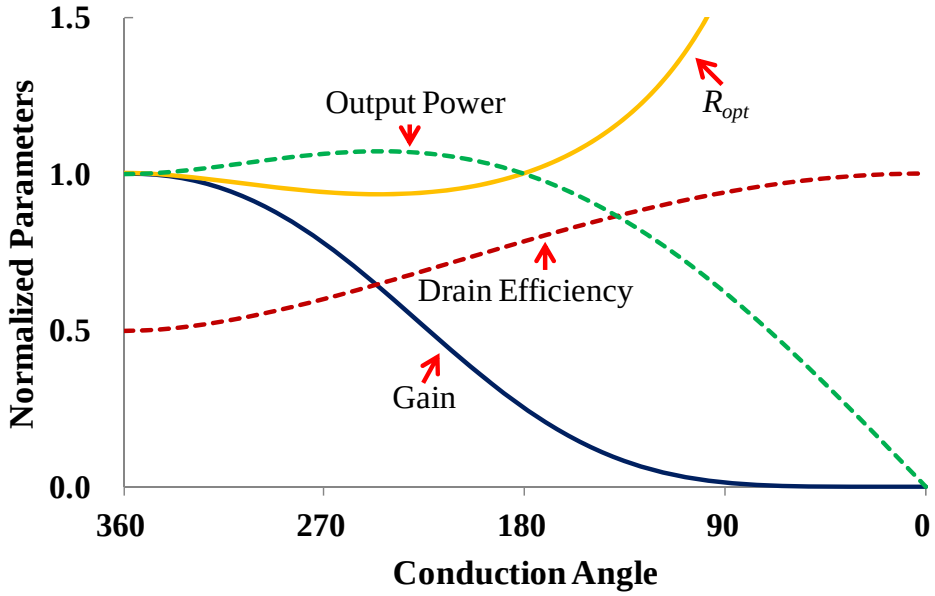


Fig. 2.4 Calculated maximum output power, drain efficiency , optimum drain load and gain as the function of conduction angle

For comparison purposes, a normalized gain (=P_{out}/P_{in}) is also evaluated under the assumption of $P_{in} = 0.5V_{pk}^2$. Fig. 2.4 shows the variation of maximum output power (normalized with respect to class A mode), drain efficiency, optimum drain

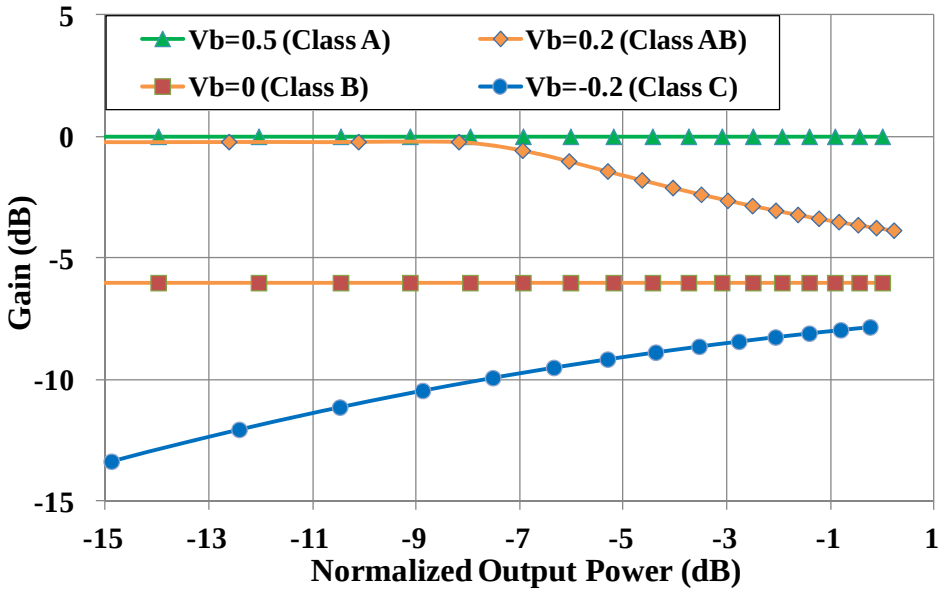


Fig. 2.5 Theoretical gain performace as a function of normalized output power under different operation mode

load and gain as the function of α. It is clear that as α decreases, drain efficiency increasses monotonically with substantial reduction of gain. The output power slightly increases initially (class AB region), and falls back to class A level with class B operation, and drops sharply under class C operation.

Fig. 2.5 shows the gain performace as a function of normalized output power under different operation mode. In the ideal case, class AB mode will exhibit gain compression while class A and B modes have entirely linear response. However, with real devices, the low quesicent bias of device in class AB mode can generate a certain amount of gain expansion [1] which cancells out the gain compression, and eventually lead to linear operation similar to class A mode. In summary, class AB mode can provide the best tradeoff between effficiency, gain, output power and linearity, thus is the most frequently adopted mode in practice.

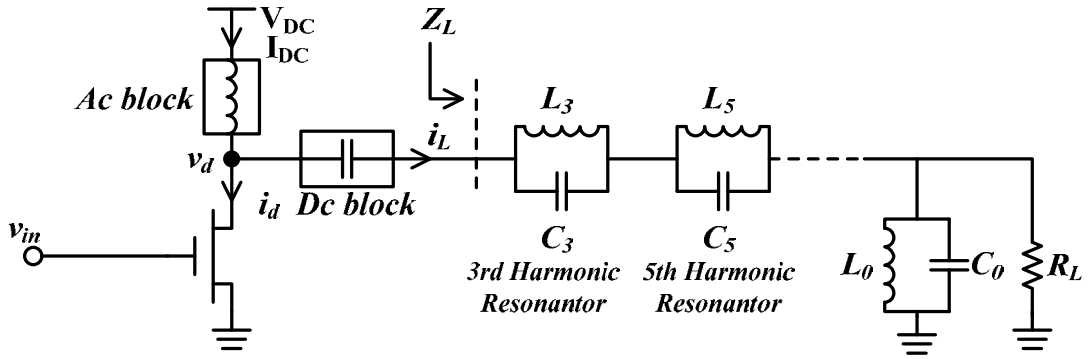


Fig. 2.6 Simplified diagram of Class F amplifier

2.2 High Efficiency mode: class F

In the previous section, several operation modes of PA has been analysed under the condition that all harmonic components of the drain voltage are set to zero. For the partipular class B mode of half-period conduction time, the efficiency can be improved to 78.5%. This section introduces class F operation which employs odd harmonic voltages to enhance both efficiency and output power. As the drain voltage is reshaped from sinewave to square wave, the drain efficiency can achieve a theoretical value of 100%.

Fig. 2.6 shows the simplified diagram of class F amplifier. The parallel renonators are inserted to create the required odd harmonic voltage. Hence, the drain voltage can be writen as:

$$\begin{aligned} V_d &= V_{dc} - V_{d1}\cos(\theta) + V_{d3}\cos(3\theta) - V_{d5}\cos(5\theta) + \cdots \\ &= V_{dc}[1 - k_1\cos(\theta) + k_3\cos(3\theta) - k_5\cos(5\theta) + \cdots] \end{aligned} \tag{2.13}$$

The flattening process of drain voltage waveform is shown in Fig. 2**.7**. If a small amount of third harmonic (with positive k_3) is introduced under class B operation (Fig. 2.7 (a)), the peak-to-peak swing of the composite waveform would be reduced

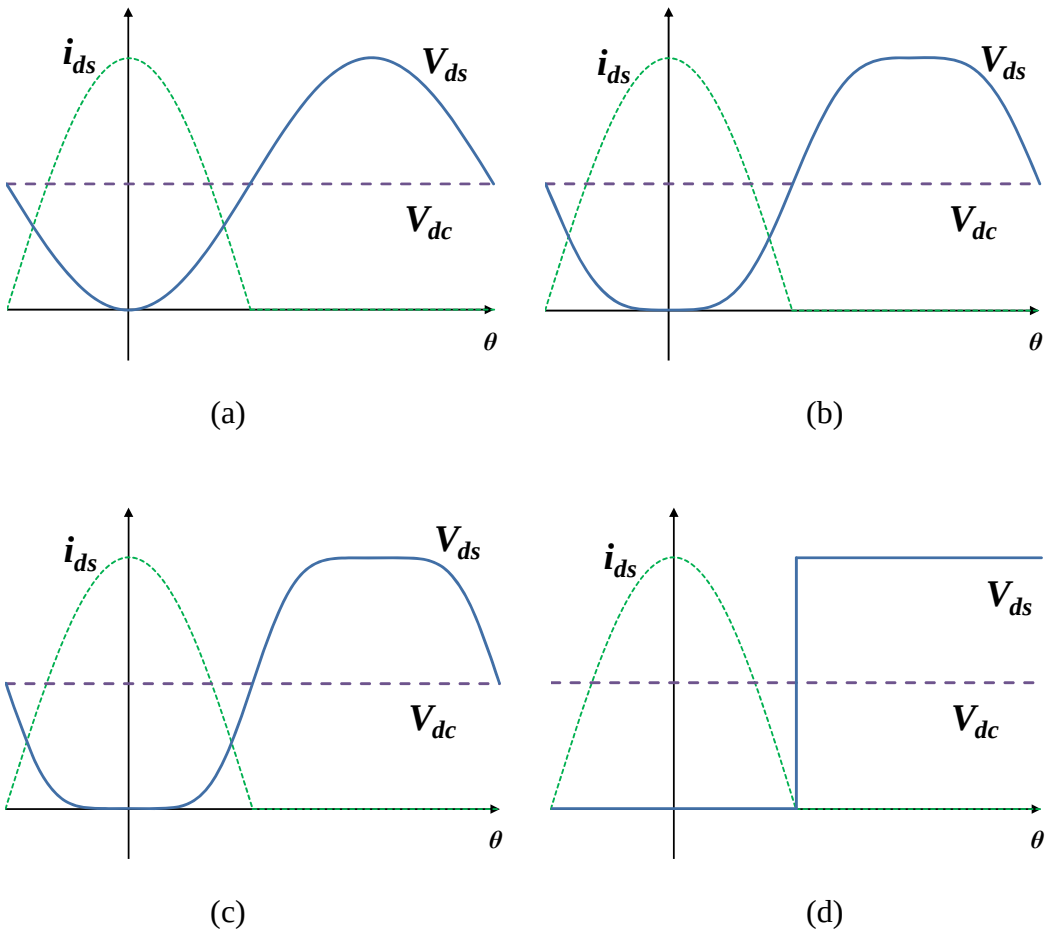


Fig. 2.7 Drain voltage flatting process from Class B to Class F: (a) Class B; (b) Class F with 3rd harmonic peaking; (c) Class F with 3rd and 5th harmonic peaking; (d) Class F with infinite odd harmonics

from the orginal value of V_{max}. Therefore, the presence of third harmonic allows the increase of fundamental ampliftude from $V_{max}/2$ to a higher level, thus enhancing the output power. On the other hand, the reshaped waveform also reduces the heat dissipation (higher drain efficiency) as the overlapping (time-domain waveforms) between the drain voltage and current (Fig. 2.7(b)) is reduced. The addition of fifth harmonic has a similar effect on the shaping of voltage waveform (Fig. 2.7(c)). Finally, with infinite odd harmonics, a square wave (Fig. 2.7(d)) can be formed (with zero overlap between voltage and current), which implies 100% conversion between

Table 2.1
Summary of voltage component amplitudes and the corresponding enhancement

Class	k1	k3	k5	Peak DE (%)	Normalized Pout
B	1	—	—	78.5	1
F3	9/8	1/8	—	88.4	1.125
F5	75/64	25/128	3/128	92.0	1.172
F∞	4/π	4/3π	4/5π	100	1.273

dc power to rf power with zero heat dissipation, zero harmonic power and 100% drain efficiency. Table 2.1 summarizes the amplitude coefficient extracted by the maximum flat condition [2] and the corresponding enhancement performances in power and efficiency.

2.3 The switching mode: Class E

Compared to the previous PA designs, the major feature of Class E PA is the strong nonlinearity due to the switching mode behavior. Although the Class AB and C do not process strictly linear gain performance, amplitude of the input and output signals are still related. In Class E operation, the transistor is modeled as a switch, thus the standalone Class E PA is not suitable for amplifying AM signal. However, for constant envelope signal with only phase information, Class E PA can be applied with theoretical drain efficiency as high as 100%. Moreover, Class E PA is commonly employed in the Envelope Elimination & Restoration (EER) Technique (to be covered in Section 2.4).

Fig. 2.8 shows the simplified diagram of class E PA. The series L_0-C_0 resonator is used to suppress the high-order harmonic current in i_{rf} (only the fundamental

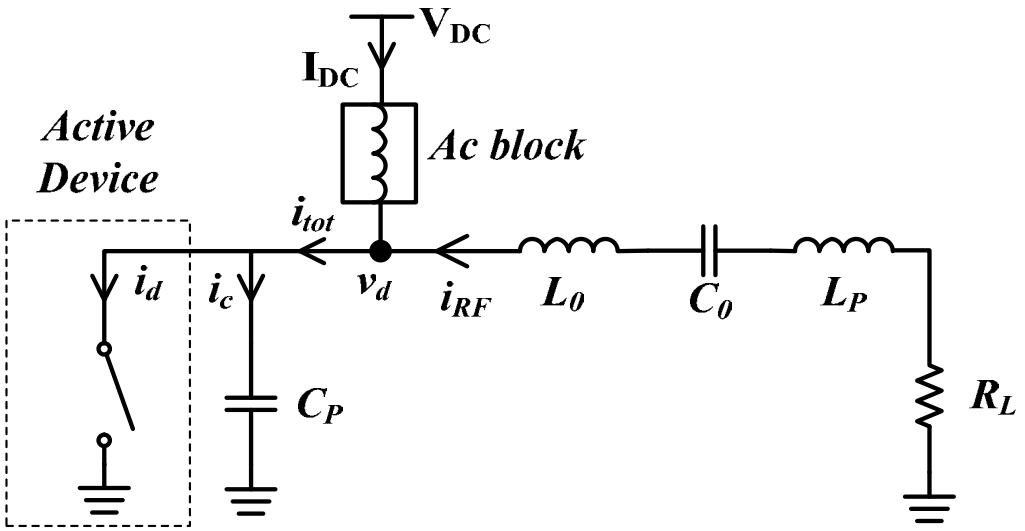
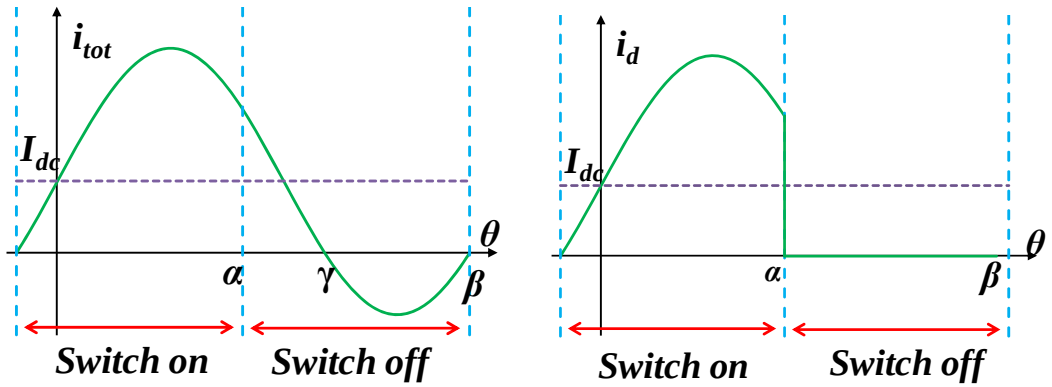
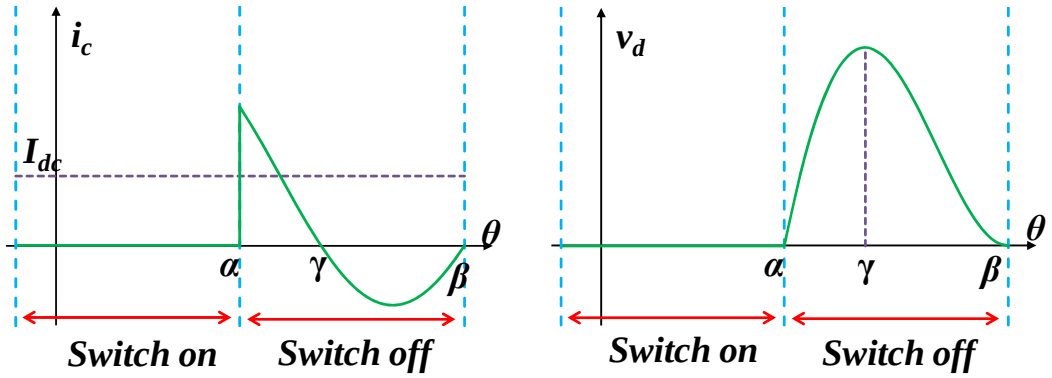


Fig. 2.8 The simplified diagram of class E amplifier



(a)

(b)



(c)

(d)

Fig. 2.9 Theoretical drain current and voltage waveforms of Class E amplifier under 50% duty cycle

component is kept):

$$i_{RF} = I_{RF}\sin(\theta) \tag{2.14}$$

Therefore, the total current (Fig. 2.9(a)) flows to the switch and capacitor:

$$i_{tot} = I_{DC} + I_{RF}\sin(\theta) \tag{2.15}$$

In the switch-ON period, all the current flows to the device branch with zero current across the shunt capacitor. Reversely, all the current flows to the capacitor in the switch-OFF period. Fig. 2.9(b) and (c) depicts the time domain waveform of i_d and i_c, which can be written as:

$$i_d = \begin{cases} I_{DC} + I_{RF}\sin(\theta) & Switch\text{-}ON\ Period \\ 0 & Switch\text{-}ON\ Period \end{cases} \tag{2.16}$$

$$i_c = \begin{cases} 0 & Switch\text{-}ON\ Period \\ I_{DC} + I_{RF}\sin(\theta) & Switch\text{-}ON\ Period \end{cases} \tag{2.17}$$

Fig. 2.9(d) shows the waveform of v_d which can be calculated from the time domain integration of i_c. Although the device is modelled as a lossless switch, the switching loss would still exist (non-zero drain voltage when the switch is turned on). Therefore, the Zero Voltage Switching (ZVS) is imposed to minimize the switching loss:

$$v_d\big|_{turn-on} = 0 \tag{2.18}$$

On the other hand, in practical case, the switch transition time between on and off state is not zero, and the overlap of voltage and current in this duration would lead to heat dissipation. Therefore, the Zero Voltage Derivative Switching (ZVDS) is also imposed, which helps to minimize the switch current when device turns on:

$$\frac{dv_d}{d\theta}\Big|_{turn-on} = 0 \tag{2.19}$$

Table 2.2
Summary of PA performance under various operation mode (V_{max}=I_{max} =1).

Class	V_{dc}	I_{dc}	Peak DE (%)	Maximum Pout
B	0.5	0.318	78.5	0.125
F	0.5	0.318	100	0.159
E	0.281	0.349	100	0.098

With the conditions of (2.18) and (2.19), circuit parameters (C_p, L_p, R_L) can be calculated for a given output power level [3]. The typical drain current and voltage waveforms shown in Fig. 2.9 (b) and Fig. 2.9 (d) exhibit no harmonic power dissipation, zero overlapping (time-domain) and 100% drain efficiency.

Table 2.2 summarizes the maximum output power and drain efficiency performance of various operation modes. It is clear that class E mode possesses the lowest the output power capability due to the highest voltage peak. Another drawback is that, as class E theory is constructed based on a switching device, normally the standalone class E amplifier is not suitable for handling signal with amplitude modulation.

2.4 Efficiency Enhancement Techniques

As mentioned previously, the conventional PA can only provide peak efficiency at the highest output power level while transmitting signal generally possesses large peak-to-average ratio, which lead to poor overall efficiency. Therefore, various efficiency enhancement techniques have been introduced to efficiently amplify signal with amplitude modulation.

2.4.1 Doherty amplifier

The popularity of Doherty Power Amplifier (DPA) mainly attributes to its ability of providing high efficiency in an extended power range with simply circuitry. As shown in Fig. 2.10, a total of four building blocks are involved: main device, auxiliary device, a quarter-wavelength Transmission Line (TL) and a resistive load R_L.

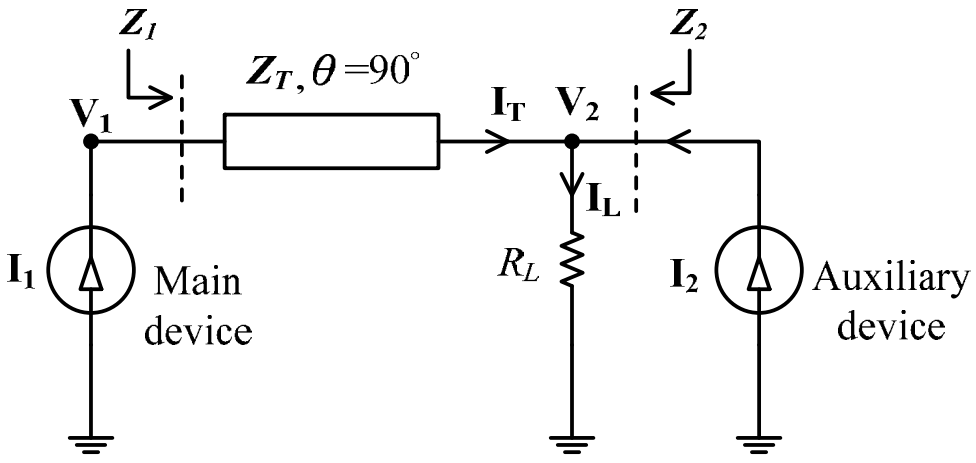


Fig. 2.10 Simplified diagram of the Doherty amplifier

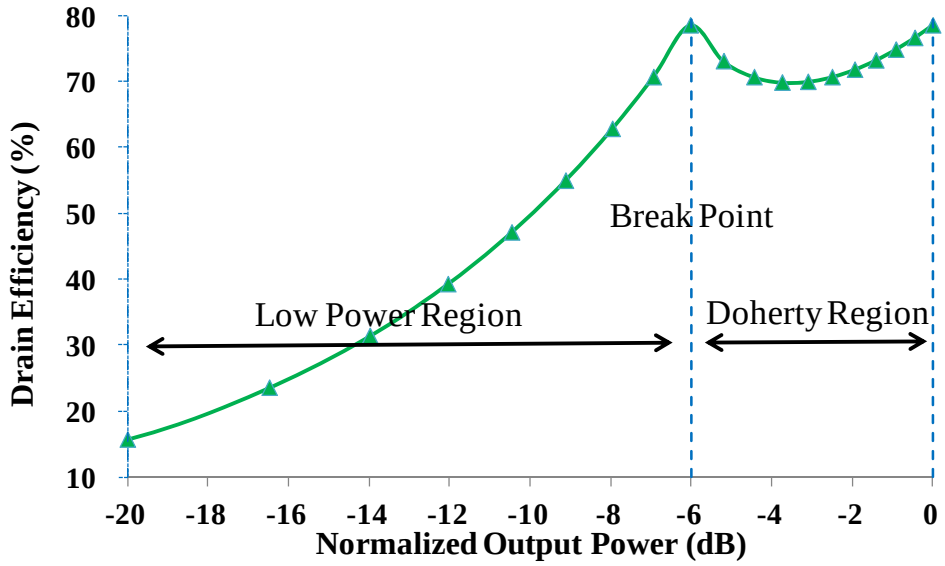


Fig. 2.11 Typical drain efficiency behavior of the Doherty amplifier

As depicted in Fig. 2.11, there are two operating regions for a typical Doherty amplification: the low power region and Doherty region. In the low power region, the auxiliary device is off, and the Doherty amplifier is acting as a conventional PA. As a result, the main device is loaded by a fixed impedance given by:

$$Z_{1cri} = \frac{Z_T^{\ 2}}{R_L} \tag{2.20}$$

The break point denotes the transition of operation regions (turning-on of auxiliary device), and it is also the location of the first efficiency peak (the fundamental drain voltage V_1 should reach its peak value V_{1sat}).

Inside the Doherty region, with the injection current of the auxiliary device, the value of the drain load Z_1 become dynamic and can be modulated to keep V_1 staying at V_{1sat} even for the higher output power level (thus high efficiency is maintained inside Doherty region). The ABCD matrix of the combination of impedance inverter and the load R_L can be written as:

$$\begin{bmatrix} \mathbf{V_1} \\ \mathbf{I_1} \end{bmatrix} = \begin{bmatrix} jZ_T / R_L & jZ_T \\ j / Z_T & 0 \end{bmatrix} \begin{bmatrix} \mathbf{V_2} \\ -\mathbf{I_2} \end{bmatrix} \tag{2.21}$$

Thus we have:

$$\mathbf{V_1} = Z_T(\frac{Z_T}{R_L} \cdot \mathbf{I_1} - j \cdot \mathbf{I_2}) \tag{2.22}$$

$$\mathbf{V_2} = -j \cdot \mathbf{I_1} Z_T \tag{2.23}$$

To extract maximum power, it is obvious that I_2 should be $\pi/2$ behind I_1 in phase. If α_c and α_v are the current ratio ($=I_{2sat}/I_{1sat}$) and voltage ratio ($=V_{2sat}/V_{1sat}$) at saturation respectively, the dynamic drain load Z_1 can therefore be represented as:

$$Z_1 = Z_T(\frac{Z_T}{R_L} - \frac{I_2}{I_1}) = \frac{V_{1sat}}{I_1} \tag{2.24}$$

At saturation, the main device should be terminated by the optimum load R_{opt} ($=V_{1sat}/I_{1sat}$), and hence, we have:

$$Z_{1sat} = Z_T(\frac{Z_T}{R_L} - \alpha_C) = R_{opt} \tag{2.25}$$

$$\alpha_V = \frac{V_{2sat}}{V_{1sat}} = \frac{I_{1sat} Z_T}{V_{1sat}} = \frac{Z_T}{R_{opt}} \tag{2.26}$$

As the auxiliary current increases, the drain load is modulated from Z_{1cri} to Z_{1sat}, where β_d is the dynamic load span defined by:

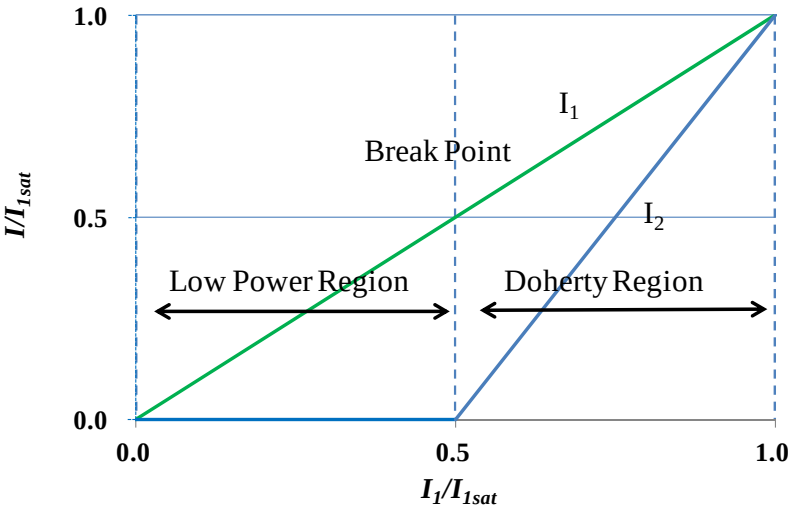
$$\beta_d = \frac{Z_{1cri}}{Z_{1sat}} = \frac{Z_{1cri}}{R_{opt}} \tag{2.27}$$

From (2.25)-(2.27), the following formulas can thus be found:

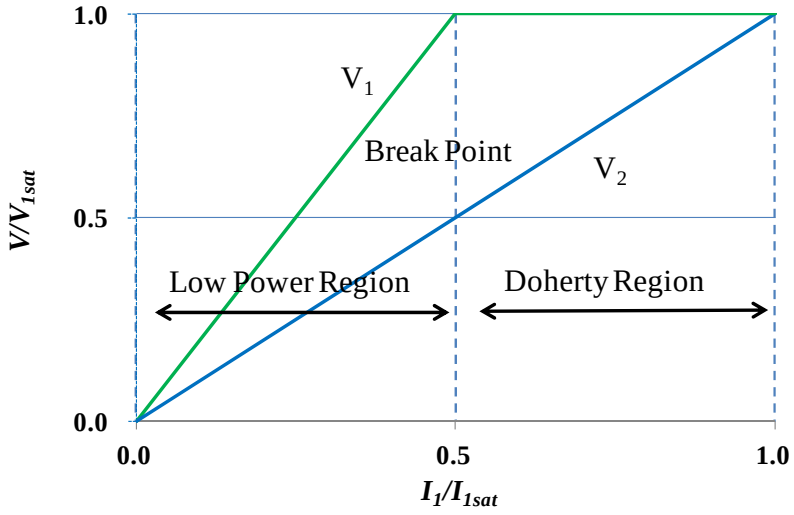
$$\beta_d = 1 + \alpha_C \alpha_V \tag{2.28}$$

$$Z_T = \alpha_V R_{opt} \tag{2.29}$$

$$R_L = \frac{{\alpha_V}^2}{1 + \alpha_C \alpha_V} R_{opt} \tag{2.30}$$



(a)



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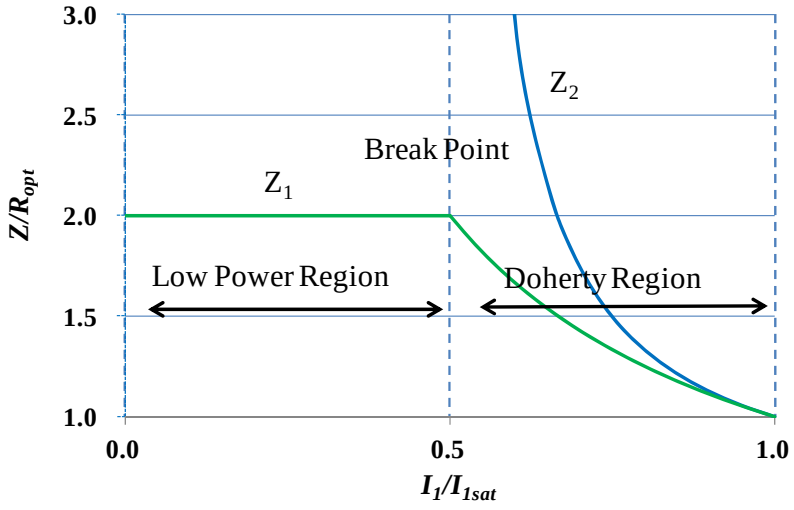


(c)

Fig. 2.12 Parameter Profiles for Doherty operation: (a) Drain current; (b) Drain Voltage; (c) Drain load;

Subsequently, the output power level for the first and second efficiency peak can be expressed as follows:

$$P_{cri} = P_{1cri} = \frac{V_{1sat}^{\ 2}}{2\beta_d R_{opt}} \tag{2.31}$$

$$P_{sat} = P_{1sat} + P_{2sat} = (1+\alpha_C\alpha_V)\frac{V_{1sat}^{\ 2}}{2R_{opt}} \tag{2.32}$$

The Output Back-Off (OBO), which is a measure of the high efficiency range, can be written as:

$$OBO = 10\log(\frac{P_{cri}}{P_{sat}}) = 10\log[\beta_d(1+\alpha_C\alpha_V)] = 20\log(1+\alpha_C\alpha_V) \tag{2.33}$$

In the symmetrical device scenario, both devices process the same saturation current and voltage:

$$\alpha_C = \alpha_V = 1 \tag{2.34}$$

From (2.28)-(2.30), the following relationship can be deduced (β_d =2):

$$Z_T = 2R_L = R_{opt} \tag{2.35}$$

The above is the classical configuration proposed by W. Doherty [4], with a theoretical high efficiency range of 6 dB. From (2.24), the required auxiliary current can be written as:

$$I_2 = \begin{cases} 0 & I_1 < 0.5I_{1sat} \\ 2I_1 - I_{1sat} & I_1 \geq 0.5I_{1sat} \end{cases} \tag{2.36}$$

The drain current, voltage and load profiles are depicted in Fig. 2.12. If both devices are biased in Class B, the ideal Doherty behavior will be created (Fig. 2.11).

In practice, the main device is often biased in class AB mode while the auxiliary device is biased in class C mode, with a slightly reduction of OBO (~5 dB). Moreover, it has been shown that the IMD components of class AB mode and class C mode amplifiers exhibit anti-phase relationship, and therefore, the linearity of Doherty amplifier is far better than expected due to IMD cancellation.

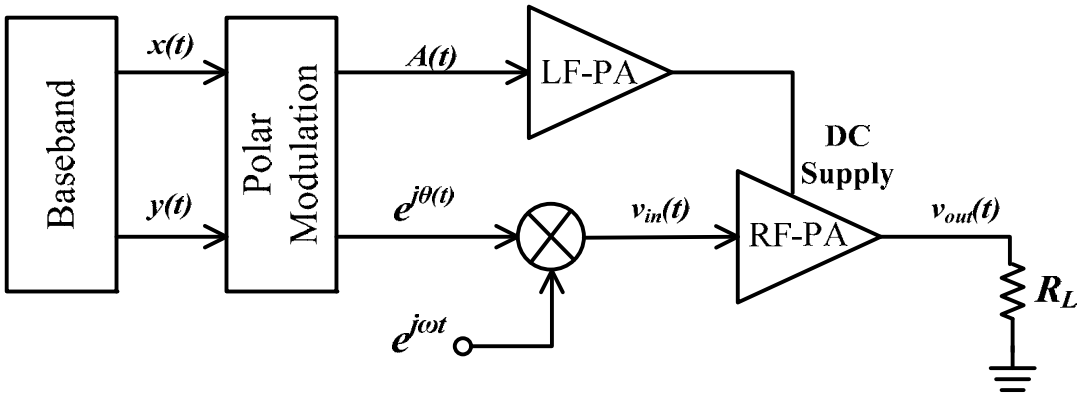


Fig. 2.13 The basic diagram of Envelope Elimination and Restoration (EER) technique

2.4.2 Envelope Elimination and Restoration Technique

Fig. 2.13 shows the basic diagram of Envelope Elimination and Restoration (EER) technique. The polar modulation system separates the baseband signal into the amplitude modulation and phase modulation signal components:

$$A(t) = \sqrt{x(t)^2 + y(t)^2} \tag{2.37}$$

$$\theta(t) = \arctan[\frac{y(t)}{x(t)}] \tag{2.38}$$

The envelope variation is eliminated in the RF path, and the input signal of the RF PA exhibits constant envelope with only phase modulation. Because of this,

switching mode PA, like Class E amplifier can be adopted with theoretically 100% drain efficiency [5]. On the other hand, the output signal of Class E PA is proportional to the drain supply, and therefore, the envelope signal *A(t)*, after amplified by a low frequency PA, can be applied as the DC supply of the nonlinear RF PA to restore the original waveform:

$$v_{in}(t) = \cos[\omega t + \theta(t)] \tag{2.39}$$

$$v_{out}(t) = GA(t)v_{in}(t) = GA(t)\cos[\omega t + \theta(t)] \tag{2.40}$$

Clearly, for the baseband part, the polar modulation system can be easily realized by modern DSP technology. For the RF part, the adoption of nonlinear PA (Class E) is a more efficient solution than linear amplification (Class AB). The single PA design approach takes the advantages of ease of matching and wider bandwidth, in compared with the Doherty amplifier. However, the amplification of the envelope signal (low frequency path) is normally not as efficient as the RF part, which seriously pulls down the overall efficiency. Moreover, the phase relationship between input and output of the RF PA behaves nonlinear when the dc supply is varied, thus extra linearization is required which further complicates the whole design.

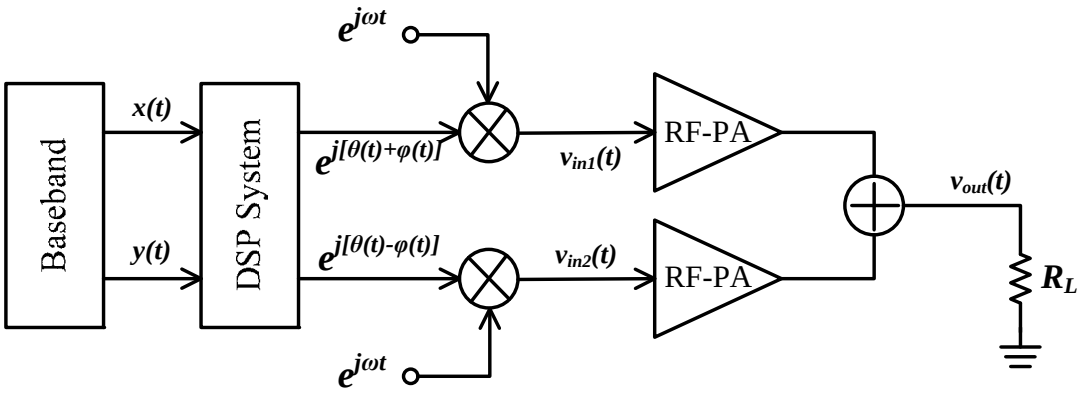


Fig. 2.14 The basic diagram of the conventional outphasing technique

2.4.3 Outphasing Technique

Similar to EER technique, the outphasing technique also adopts constant envelope signal and nonlinear amplifiers. Fig. 2.14 shows the basic diagram of the conventional outphasing technique. The baseband signal is given by:

$$g(t) = x(t) + j \cdot y(t) = A(t) \cdot e^{j\theta(t)} \tag{2.42}$$

where $A(t)$ is the normalized amplitude and $\theta(t)$ is the phase component. A DSP system is used to generate two phase modulated signals (constant envelope):

$$\cos[\varphi(t)] = A(t) \tag{2.43}$$

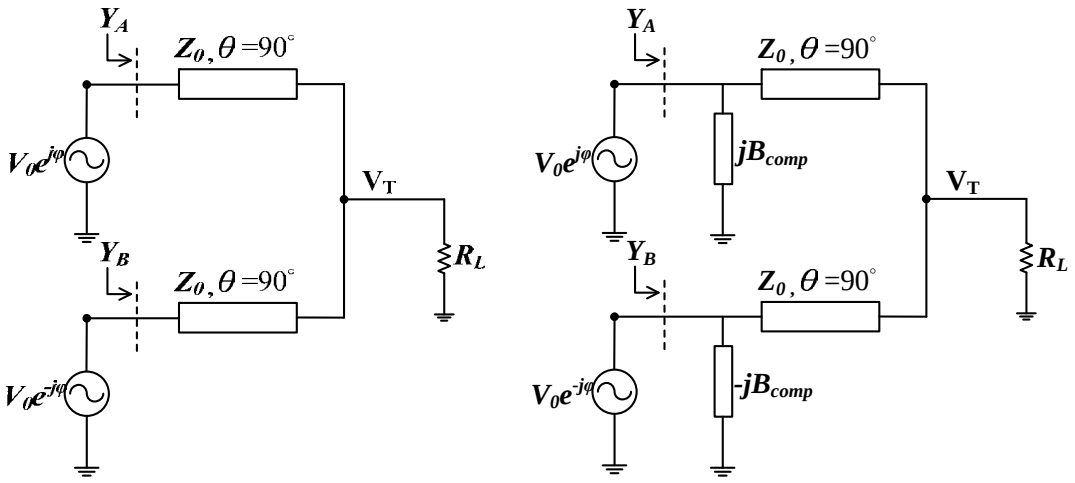
If nonlinear PA (with gain of G) is adopted, the amplitude information can be restored at the output:

$$v_{in1}(t) = \cos[\omega t + \theta(t) + \varphi(t)] \tag{2.44}$$

$$v_{in2}(t) = \cos[\omega t + \theta(t) - \varphi(t)] \tag{2.45}$$

$$v_{out}(t) = G[v_{in1}(t) + v_{in2}(t)] = 2G\cos[\omega t + \theta(t)]\cos[\varphi(t)] = 2GA(t)\cos[\omega t + \theta(t)] \tag{2.46}$$

Obviously, the adoption of nonlinear PA helps to reduce heat dissipation, but it is



(a) (b)

Fig. 2.15 Chireix Outphasing Amplifier: (a) Without compensation for the complex load; (b) With compensation for the complex load.

worth to note that the dc power consumption remains constant regardless of the actual power level. Therefore, the drain efficiency decreases when output power is back off. For average efficiency enhancement, Chireix proposed the usage of a non-isolating combining circuitry [6], as illustrated in Fig. 2.15. Two phase-modulated voltage sources, representing the outputs of the nonlinear PAs, are connected to the combining load (R_L) with quarter wavelength transformers. Like Doherty amplifier, the effective drain load of each device in Chireix amplifier is dynamically modulated by the other device. By circuit analysis, it can be shown that (φ is the outphasing angle):

$$P_{out} = \frac{2R_L}{Z_0^{\,2}} V_0^{\,2} \cos^2(\varphi) \tag{2.47}$$

$$Y_A = \frac{R_L}{Z_0^{\,2}} 2\cos^2(\varphi) - j\frac{R_L}{Z_0^{\,2}} \sin(2\varphi) \tag{2.48}$$

$$Y_B = \frac{R_L}{Z_0^{\,2}} 2\cos^2(\varphi) + j\frac{R_L}{Z_0^{\,2}} \sin(2\varphi) \tag{2.49}$$

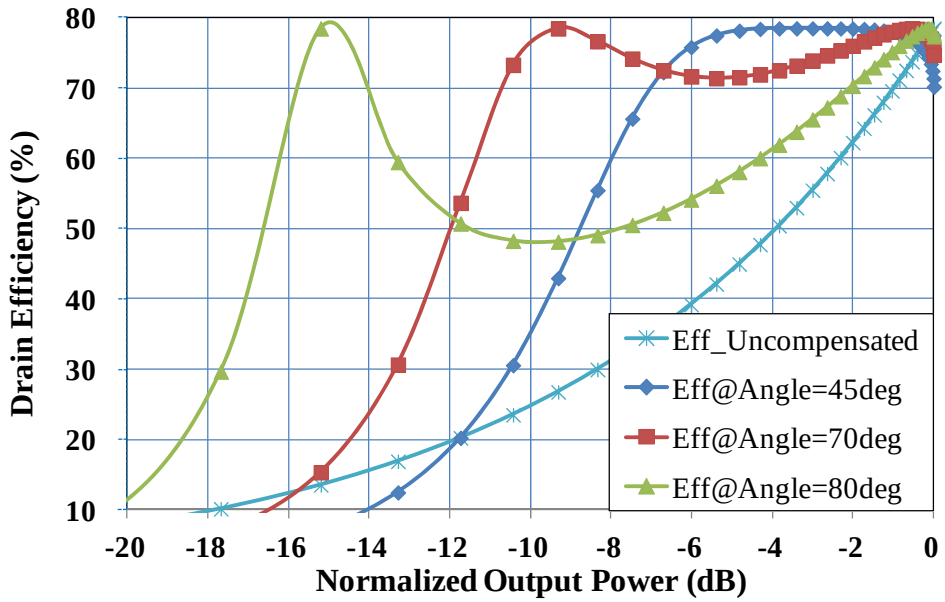


Fig. 2.16 Drain efficiency behaviors of the Chireix Outphasing Amplifier under various compensation angles.

Note that the drain loads are complex admittance with opposite susceptance, since the active device can only present peak efficiency when the load is purely resistive, and therefore, the compensation components (Fig. 2.15 (b)) are added to cancel the susceptance and improve the efficiency at a given outphasing angle. Referring to Fig. 2.15 (b), we have:

$$Y_A = \frac{R_L}{Z_0^{\,2}} 2\cos^2(\varphi) - j\frac{R_L}{Z_0^{\,2}}\sin(2\varphi) + jB_{comp} \tag{2.50}$$

$$Y_B = \frac{R_L}{Z_0^{\,2}} 2\cos^2(\varphi) + j\frac{R_L}{Z_0^{\,2}}\sin(2\varphi) - jB_{comp} \tag{2.51}$$

$$B_{comp} = \frac{R_L}{Z_0^{\,2}}\sin(2\varphi_C) \tag{2.52}$$

In which φ_c is the compensation angle generated by B_{comp}. Assume both devices are operating at saturation (Class B mode) [1], the theoretical drain efficiency behavior of the compensated Chireix out-phasing technique can be derived as:

$$\eta(\varphi,\varphi_C)=\frac{\frac{\pi}{4}}{\sqrt{1+\frac{1}{4}\left(\frac{\sin(2\varphi_C)-\sin(2\varphi)}{\cos^2(\varphi)}\right)^2}} \tag{2.53}$$

Fig. 2.16 shows the drain efficiency behavior of the Chireix Outphasing amplifier versus normalized output power (=$20\log[\cos\varphi]$) under various compensation angle φ_C. In the idealized case, high efficiency can be maintained over 10 dB OBO range, two limitations exist in practical outphasing amplifier design [7]: Firstly, as the input power is modulated to be constant level, gain and PAE drops dramatically when output power reduces by outphasing; Secondly, it can be observed that the signal bandwidth becomes much larger (up to 12 times with outphasing angle=90°) when the baseband signal is converted to the outphasing signal. Therefore, the modulation bandwidth is strongly restricted, and the implementation of the outphasing technique become more complex and costly compared to other techniques.

Reference

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Chapter 3

Literature Review on Advanced Doherty Power Amplifier Design

In the past decades, the Doherty amplifier has drawn much research interest due to the ability of providing high efficiency in an extended power range with simple circuitry and mild linearity performance. In this chapter, recent works concerning the enhancement of high efficiency range and operating bandwidth of DPA are briefly reviewed.

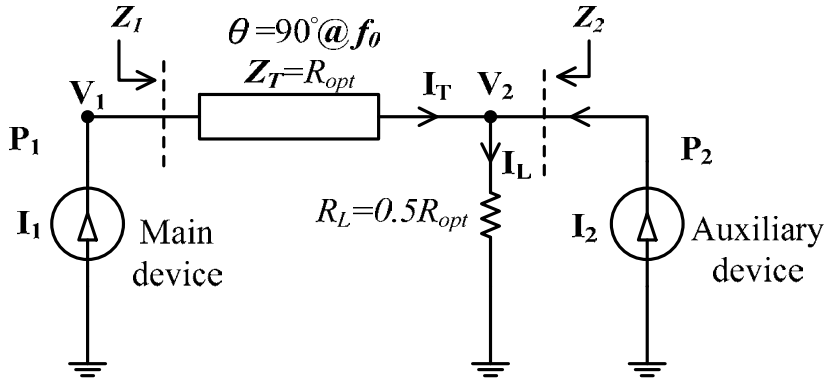


Fig. 3.1 Simplified diagram of classical Doherty amplifier

3.1 Recent works on DPA design with extended high efficiency range

It has been shown in chapter 2.4 that the classical DPA amplifier (Fig. 3.1) can offer 6dB high efficiency range of 6 dB only, which is considered to be insufficient as many modern communication standards are generating signals found with

ever-increasing value of PAPR. According to (2.33), it is found that the high efficiency range is solo determined by the output power ratio (α) at saturation:

$$\alpha = \frac{P_{2sat}}{P_{1sat}} = \frac{V_{2sat} I_{2sat}}{V_{1sat} I_{1sat}} = \alpha_C \alpha_V \tag{3.1}$$

Subsequently, we have:

$$OBO = 20\log(1+\alpha) \tag{3.2}$$

Previous techniques on extending OBO range are mostly based on the enlargement of α. A direct method is to use an auxiliary device with enlarged gate periphery, which is known as asymmetrical DPA [1]-[5]. Usually, the main and auxiliary devices employ the same semiconductor technology with equal drain bias. As a result, the auxiliary device (enlarged gate periphery) can deliver a higher level of auxiliary current and auxiliary power, which results in extended OBO.

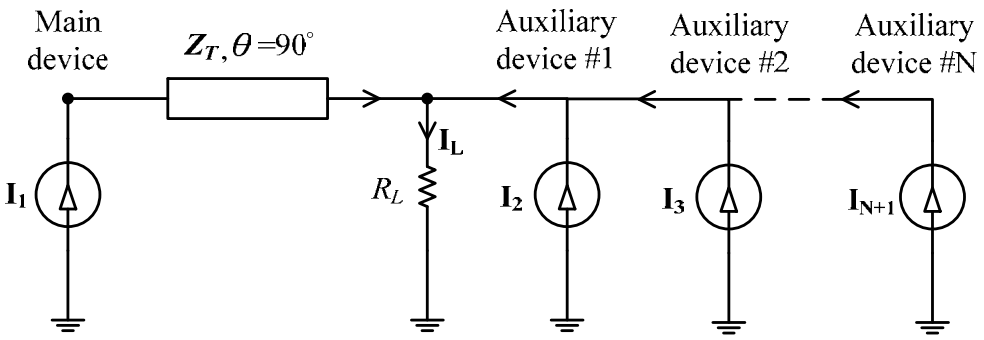


Fig. 3.2 Simplified diagram of multi-way Doherty amplifier

Alternatively, one can also use multiple auxiliary devices to increase the total amount of auxiliary current. Fig. 3.2 shows the diagram of the multi-way DPA [6], which turns on the auxiliary devices simultaneously and act equivalently to the asymmetrical DPA. Fig. 3.3 shows the drain efficiency behavior of asymmetrical DPA and multi-way DPA.

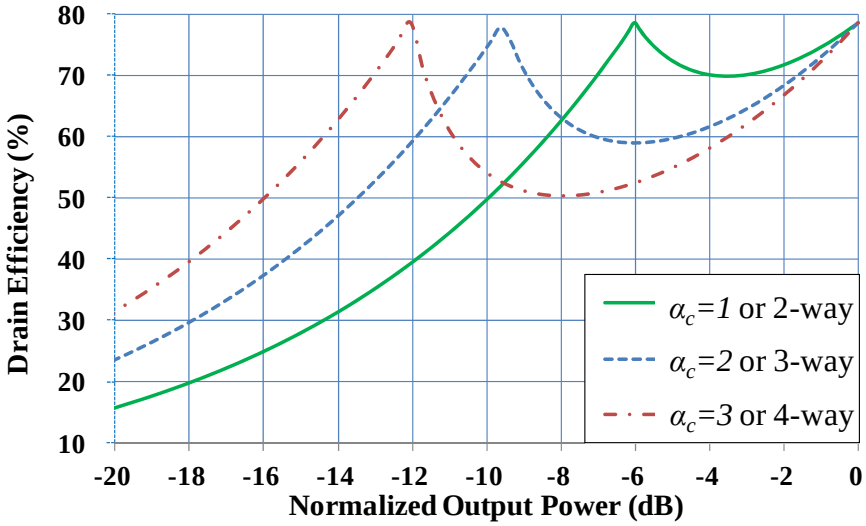


Fig. 3.3 Theoretical drain efficiency behavior of the asymetrical DPA and the multi-way DPA

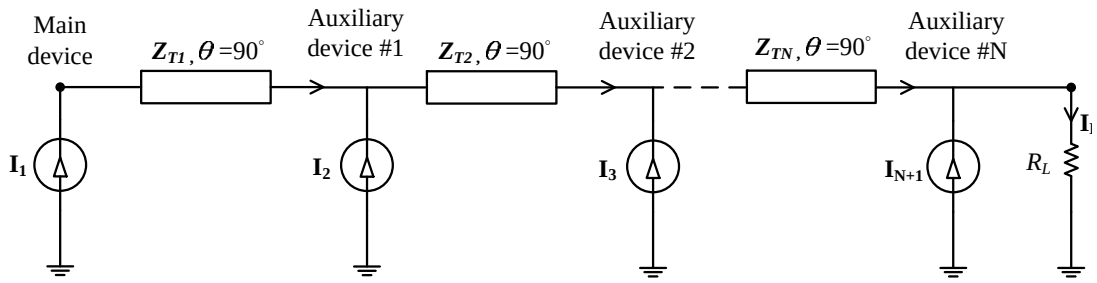


Fig. 3.4 Simplified diagram of multi-stage Doherty amplifier

Another technique is the adoption of multi-stage DPA [7]-[8], as depicted in Fig. 3.4. In this configuration, the auxiliary devices turn on progressively to generate extra efficiency peaks. The drain efficiency behavior of a 3-stage DPA with gate periphery ratio of 1:3:4 is shown in Fig. 3.5. With the same total device periphery consumption, the average efficiency of the multi-stage DPA could outweigh the asymmetrical or multi-way DPA. However, the realization of such efficiency behavior imposes special requirement on current profiles. After reaching the second efficiency peak, the drain voltage of the auxiliary device #1 has to be kept constant for attaining maximum efficiency. Consequently, the main branch current I_m has to

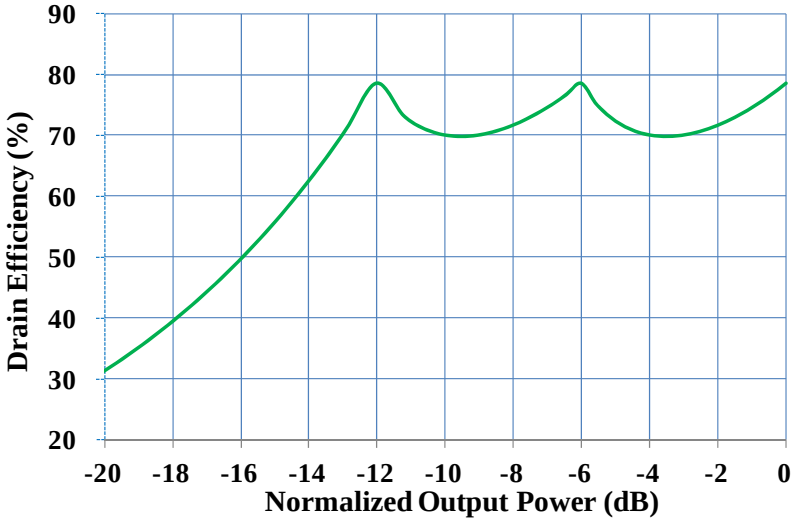


Fig. 3.5 Theoretical drain efficiency behavior of the 3-stage DPA with gate periphery ratio of 1:3:4

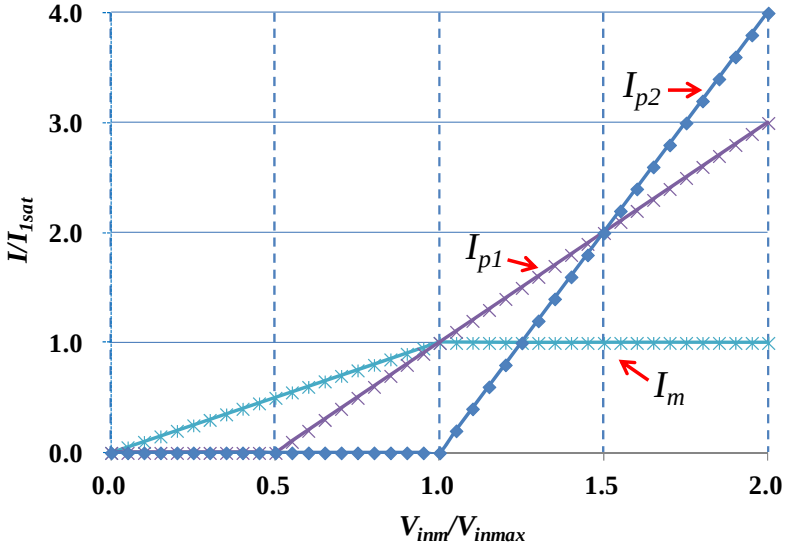


Fig. 3.6 Current profiles of a 3-stage DPA with gate periphery ratio of 1:3:4

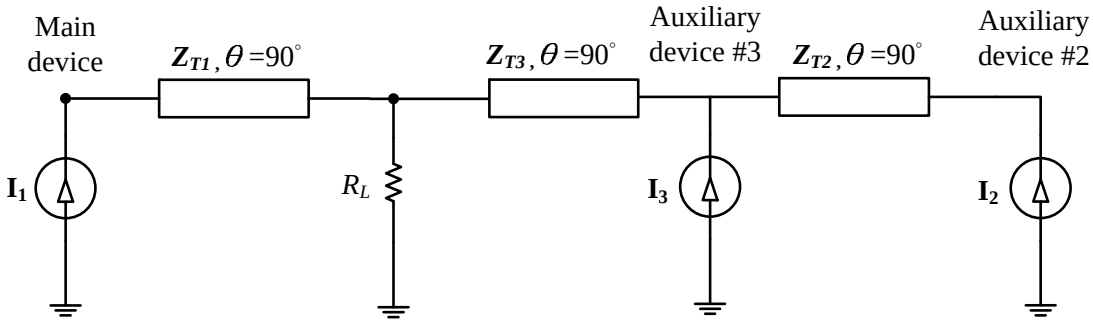


Fig. 3.7 Circuit diagram of the modified 3-stage Doherty amplifier

stay at a fixed level when V_{inm}/V_{inmax} >1 (Fig. 3.6). For linear input circuitry, such nonlinear behavior can only be produced by the overdriven of main device with the cost of generating large amount of distortion. To overcome this problem, a modified 3-stage DPA (Fig. 3.7) is presented in [9], which can generate three maximum efficiency peaks without saturated operation of main device. However, it still suffers from poor load modulation due to the low biases of the peaking PAs [10]. Therefore, gate bias adaptation is usually employed to achieve suitable load modulation for improved gain flatness and back-off efficiency.

3.2 Recent works on DPA design with extended operating bandwidth

The increase of the number of frequency bands and signal bandwidth requires future transmitter to support wideband operation. In recent year, much effort has been devoted to design DPA with extended bandwidth.

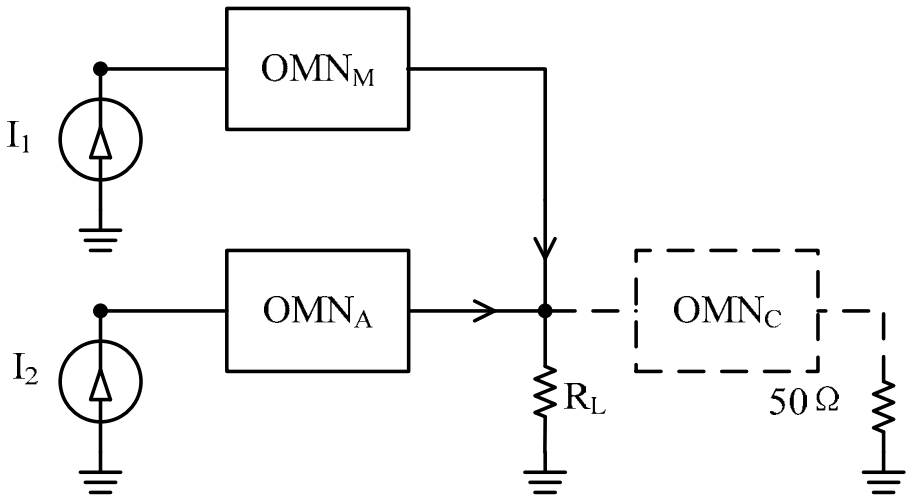


Fig. 3.8 Block diagram of DPA

Fig. 3.8 shows the block diagram of broadband DPA. The Output Combining Matching Network (OMN_C) is used to broadband transform 50ohm to the selected R_L. The Output Matching Network of Auxiliary amplifier (OMN_A) is employed to compensate the device parasitic. The Output Matching Network of Main amplifier (OMN_M) is made to operate as a broadband impedance inverter with θ=90°@f_0 [11]-[13]. The broadband networks can be synthesized with the classical filter theory [12] or Simplified Real Frequency Technique (SRFT) [13]. Based on this approach, DPAs with bandwidth up to 40% have been reported. However, serious degradation

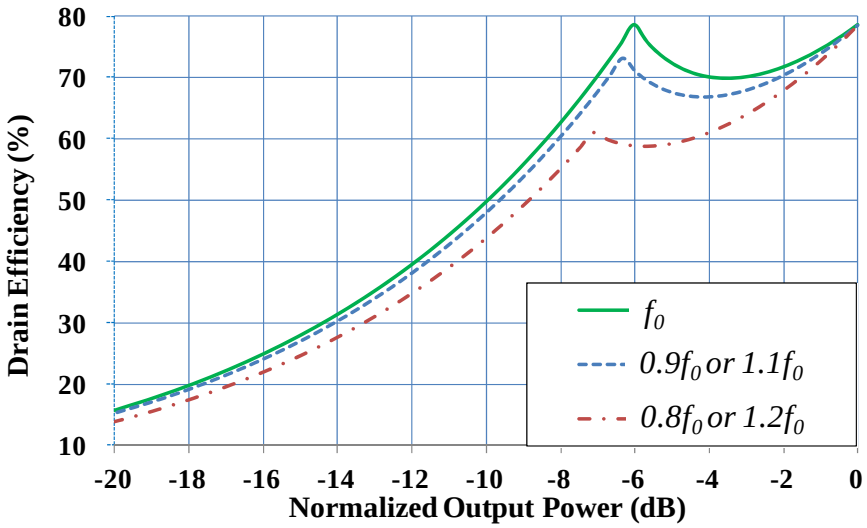


Fig. 3.9 Theoretical broadband drain efficiency behavior of DPA under classical configuration

on the efficiency (first peak) has been observed, which can be explained by the frequency variation of drain load (low power region):

$$Z_{1cri} = Z_T \frac{R_L + j\tan(\theta)Z_T}{Z_T + j\tan(\theta)R_L} = R_{opt}\frac{1 + j\cdot 2\tan(\theta)}{2 + j\tan(\theta)} \tag{3.3}$$

As frequency is offset from the center value, Z_{1cri} would deviate from the optimum load ($2R_{opt}$), which leads to efficiency degradation (low power region). Based on the classical approach, we have:

$$Z_T = 2R_L = R_{opt} \tag{3.4}$$

$$I_2 = \begin{cases} 0 & I_1 < 0.5I_{1sat} \\ 2I_1 - I_{1sat} & I_1 \geq 0.5I_{1sat} \end{cases} \tag{3.5}$$

With the assumption of in-phase combining of I_T and I_2 (Fig. 3.1), the theoretical broadband drain efficiency of classical configuration can be calculated (Fig. 3.9). It can be observed that, the efficiency curves deviates significantly from ideal case (solid line) when fractional bandwidth is extended beyond 20%.

To overcome this problem, a modified configuration is introduced in [14]:

$$Z_T = R_L = 2R_{opt} \tag{3.6}$$

As a result, the drain load (main) is maintained at $2R_{opt}$ (optimum load at 6dB back-off level) over an extended bandwidth (infinite in theory), and the efficiency peak of low power region can be maintained. Under such an arrangement, the current ratio and voltage ratio can be evaluated as:

$$\alpha_V = \frac{V_{2sat}}{V_{1sat}} = 2 \tag{3.7}$$

$$\alpha_C = \frac{I_{2sat}}{I_{1sat}} = 0.5 \tag{3.8}$$

In consequence, the resulted auxiliary current profile can be written as:

$$I_2 = \begin{cases} 0 & I_1 < 0.5I_{1sat} \\ I_1 - I_{1sat}/2 & I_1 \geq 0.5I_{1sat} \end{cases} \tag{3.9}$$

According to [14], it is further assumed that:

$$phase(I_2) = phase(I_1) - 90^\circ \tag{3.10}$$

Subsequently, from (3.9) and (3.10), the theoretical drain efficiency of the modified configuration can be calculated (Fig. 3.10), which shows substantial improvement in efficiency.

Furthermore, referring to Fig. 3.1, under the modified configuration, by the multiplication of ABCD matrices, the relationship between the terminal voltages and currents can be obtained as:

$$\begin{bmatrix} \mathbf{V_1} \\ \mathbf{I_1} \end{bmatrix} = \begin{bmatrix} e^{j\theta} & j2R_{opt}\sin\theta \\ e^{j\theta}/2R_{opt} & \cos\theta \end{bmatrix} \begin{bmatrix} \mathbf{V}_2 \\ -\mathbf{I}_2 \end{bmatrix} \tag{3.11}$$

$$\mathbf{V_1} = 2R_{opt}(\mathbf{I_1} + \mathbf{I_2}e^{-j\theta}) \tag{3.12}$$

$$\mathbf{V}_2 = 2R_{opt}(\mathbf{I_1} + \mathbf{I_2}\cos\theta)e^{-j\theta} \tag{3.13}$$

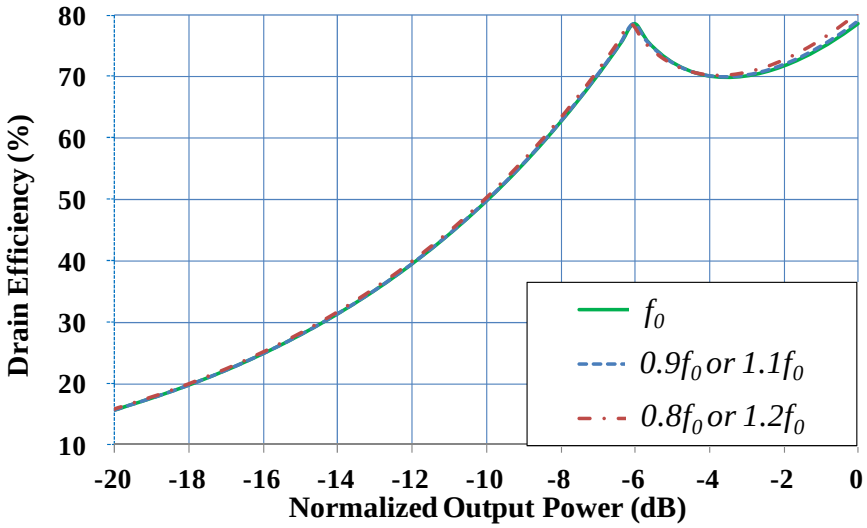


Fig. 3.10 Theoretical broadband drain efficiency behavior of DPA under classical configuration

It is also found that, if wideband conditions of (3.9) and (3.10) are imposed, the magnitude of V_1 and V_2 can exceed the bias voltage as frequency offsets from the center, which limits the available bandwidth under Class B operation. Therefore, in [15] a frequency dependent current relationship is enforced:

$$\mathbf{I_2} = \mathbf{I_1} \cdot k(f, v_{in}) e^{j\theta_d(f, v_{in})} \tag{3.14}$$

The ratio k and phase difference θ_d are function of both frequency and drive level. Clearly, at maximum output power level, the drain voltage V_{1sat} should be maintained at V_{dc} to generate the efficiency peak but without saturating the device:

$$\left|\mathbf{V_{1sat}}\right| = \left|2R_{opt}I_{1sat}(1 + ke^{j(\theta_d - \theta)})\right| = V_{dc} \tag{3.15}$$

$$\left|\mathbf{V_{2sat}}\right| = \left|2R_{opt}I_{1sat}[1 + k\cos(\theta)e^{j\theta_d}]\right| = 2V_{dc} \tag{3.16}$$

From (3.15) and (3.16), k and θ_d can be solved (Fig. 3.11) for each θ ($=f/f_0 \times 90°$). With linear input-output assumption, the analysis can be further extended to the entire Doherty region. Fig. 3.12 shows the optimum value of k and θ_d as a function of I_1 ($=v_{in}$). Complex input circuitry involving digital control system has been used to

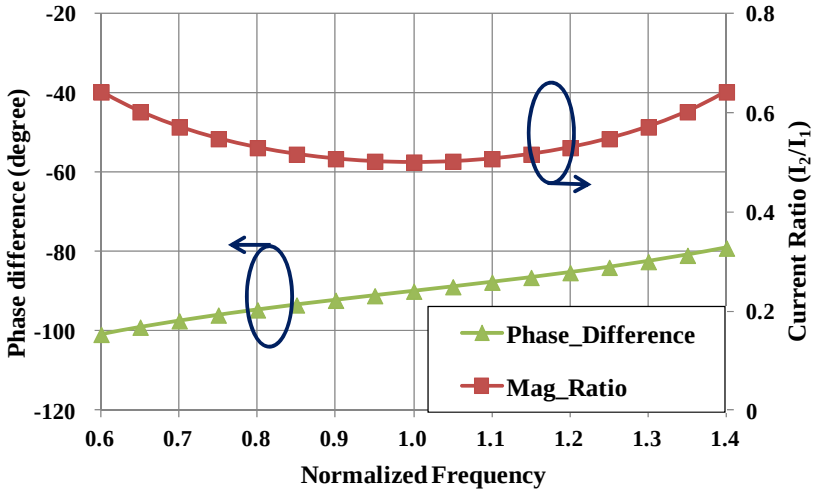
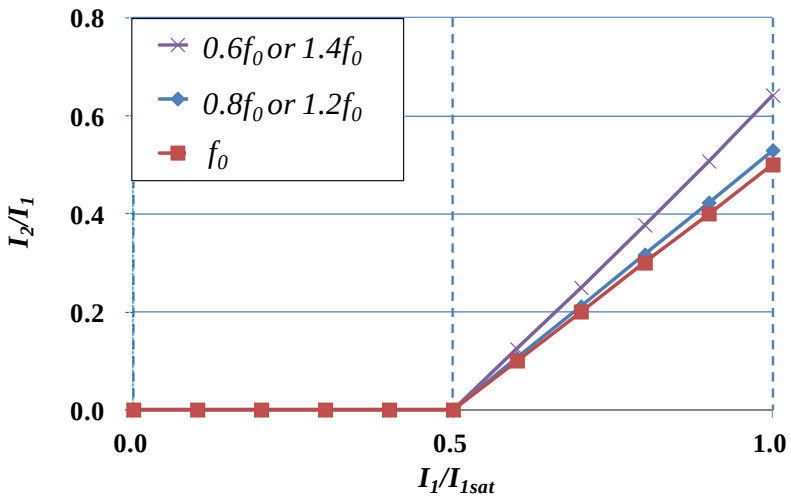
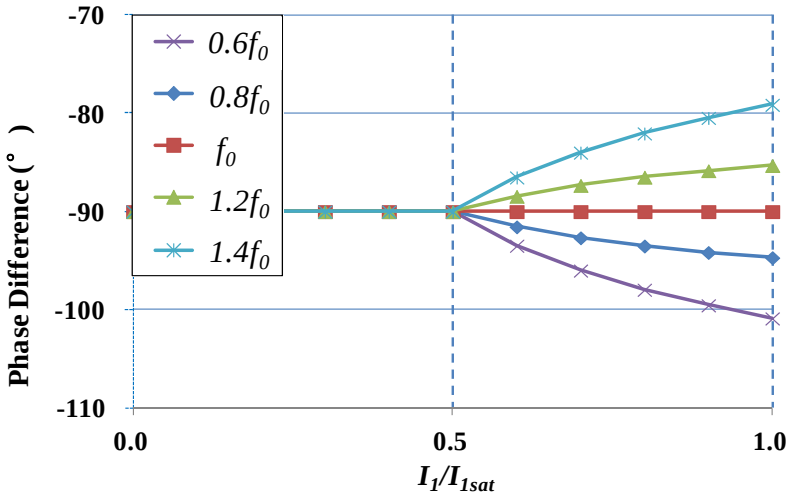


Fig. 3.11 Optimum saturation k and θ_d versus operating frequency



(a)



(b)

Fig. 3.12 Optimum current profiles: (a) magnitude ratio k; (b) phase difference θ_d.

produce the required current profiles, and demonstrated good Doherty performance over fractional bandwidth of 45%.

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Chapter 4

Extension of High Efficiency Range of Doherty Amplifier by using Complex Combining Load

As reviewed in chapter 3, the recent DPA works [1]-[11] related to the high efficiency range extension are mainly based on the increase of relative current ratio. In this chapter, we present a novel DPA configuration that uses complex combining load as a new degree of freedom to boost the range of OBO. It is accomplished by the enhancement of dynamic load span, even in the absence of multiple or asymmetric devices (to supply extra modulation current). This chapter will give the theoretical study of OBO extension in DPA by the proposed Complex Combining Load (CCL). The formulation of different operation parameters and the drain efficiency curve of the proposed design under AB-C configuration are followed. For validation, the simulated and measured performances of GaN-based DPA prototypes (conventional and proposed) are also given.

4.1 Theory of Complex Combining Load (CCL) DPA

The basic principle of dynamic load modulation of DPA has been clearly explained in section 2.1. In this section, we mainly focus on the formulation of OBO, dynamic load span and current ratio of devices, in the presence of complex combining load.

The analysis to be presented is valid for both symmetrical and asymmetrical DPA configurations. For simplicity, the following assumptions are adopted:

1) Ideal device model with zero knee voltage and parasitic. In other words, the optimum drain load for maximum output power is purely resistive;
2) The Main and Auxiliary devices exhibit the same upper limit on drain voltage (V_{MAX});
3) All higher harmonics are neglected and only the fundamental component is retained;
4) All matching networks are lossless and reciprocal.

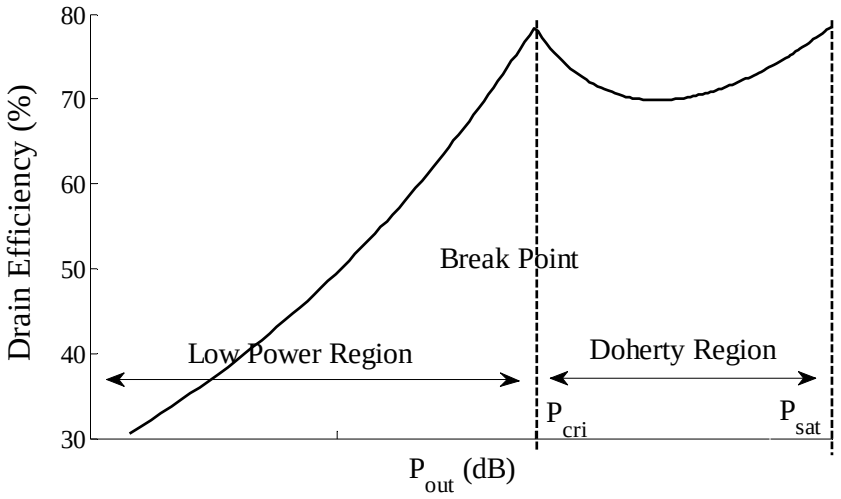


Fig. 4.1 Efficiency behavior of ideal Doherty amplifier

4.1.1 Formulation of OBO under ideal Doherty operation

Fig. 4.1 shows the typical Doherty efficiency behavior. As the breakpoint is approached, the output voltage swing of the Main device attains its maximum value which creates the first efficiency peak. Within the Doherty region, the effective load seen by the Main device is dynamically modulated by the Auxiliary current, while its

drain voltage swing is maintained at a constant level (maximum). Subsequently, a second peak in efficiency is produced when the output power of the Auxiliary device also reaches saturation.

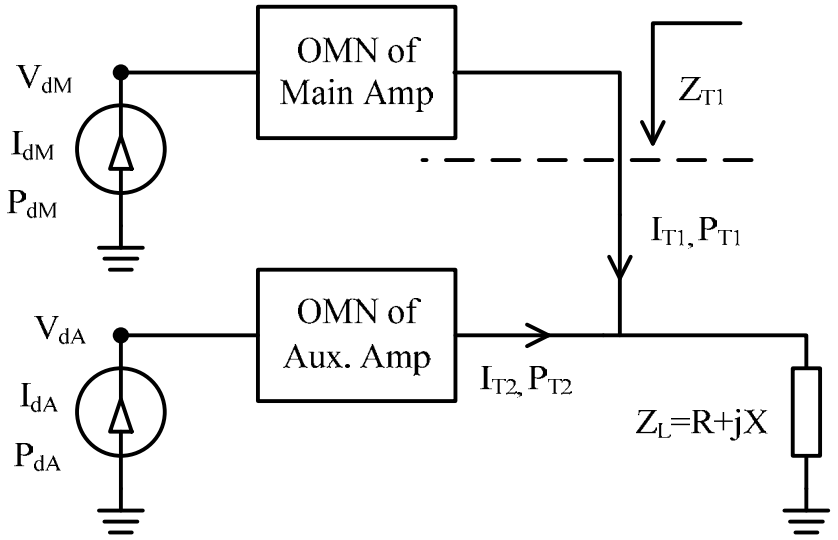


Fig. 4.2 Simplified schematic of DPA with complex combining load

Fig. 4.2 shows the generic structure of the proposed DPA. The Output Matching Network of the Main device (OMN_M) is responsible for impedance transformation; Z_L represents the combining load (= $R + j\,X$) which is usually transformed from the external 50Ω load; $P_{dM,sat}$ and $P_{dA,sat}$ denote, respectively, the saturated output powers of the Main and Auxiliary devices. As indicated from assumption 2), two devices are under small bias with unity voltage ratio (α_v=1). Therefore, in this chapter, the current ratio α_c would also be equivalent to the power ratio, and the saturated output power of DPA can be expressed as:

$$P_{sat} = P_{dM,sat} + P_{dA,sat} = P_{dM,sat}\left(1+\alpha_C\right) \tag{4.1}$$

$$\alpha_C = \left|\frac{I_{dA,sat}}{I_{dM,sat}}\right| = \frac{P_{dA,sat}}{P_{dM,sat}} \tag{4.2}$$

If $R_{dM,cri}$ and $R_{dM,sat}$ denotes, respectively, the optimum drain load seen by the Main device at the breakpoint and saturation level, the ratio of dynamic load span may then be written as:

$$\beta_d = \frac{R_{dM,cri}}{R_{dM,sat}} = \frac{P_{dM,sat}}{P_{dM,cri}} = \frac{I_{dM,sat}}{I_{dM,cri}} \tag{4.3}$$

From above, the measure of the high efficiency region (OBO in dB) is thus expressed by:

$$OBO = 10 \cdot \log\left(\frac{P_{sat}}{P_{cri}}\right) = 10 \cdot \log\left[\left(1+\alpha_C\right)\beta_d\right] \tag{4.4}$$

4.1.2 Dynamic load span under complex combining load

With current injection from the Auxiliary branch, the effective load seen by the Main amplifier, evaluated at the breakpoint and saturation level, are simply given by (4.5) and (4.6).

$$Z_{T1,cri} = Z_L \tag{4.5}$$

$$Z_{T1,sat} = Z_L\left(1+\frac{I_{T2,sat}}{I_{T1,sat}}\right) \tag{4.6}$$

Since $I_{T1,sat}$ and $I_{T2,sat}$ are in-phase components under Doherty operation, the following relations can be established:

$$\frac{I_{T2,sat}}{I_{T1,sat}} = \frac{P_{T2,sat}}{P_{T1,sat}} = \frac{P_{dA,sat}}{P_{dM,sat}} = \alpha_C \tag{4.7}$$

$$Z_{T1,sat} = Z_L\left(1+\alpha_C\right) \tag{4.8}$$

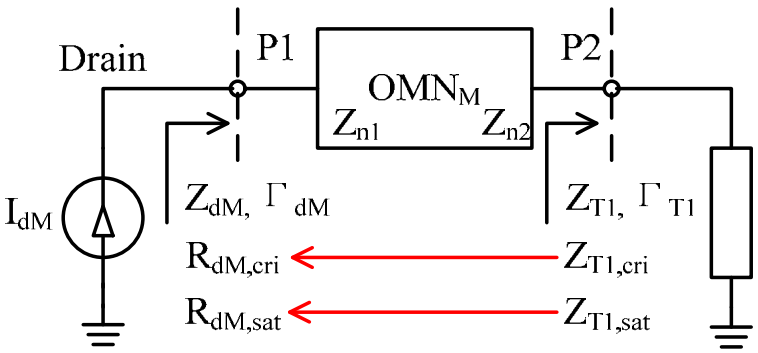


Fig. 4.3 Designated load and input impedances of OMN_M

Fig. 4.3 shows the simplified model of OMN_M in which $Z_{T1,cri}$ is transformed to $R_{dM,cri}$ while $Z_{T1,sat}$ is transformed to $R_{dM,sat}$. Based on the theory of power wave [12] ($Z_{n1} = R_{dM,sat}$; $Z_{n2} = Z_{T1,sat}$), the generalized scattering parameters of OMN_M are simply given by:

$$S_{OMN_M} = \begin{bmatrix} 0 & e^{j\varphi_M} \\ e^{j\varphi_M} & 0 \end{bmatrix} \tag{4.9}$$

Subsequently, the mathematical relationship between the load reflection coefficient and the corresponding input reflection coefficient of OMN_M may thus be written as:

$$\Gamma_{dM} = \Gamma_{T1} \cdot e^{j2\varphi_M} \tag{4.10}$$

$$\Gamma_{T1} = \frac{Z_{T1} - Z_{T1,sat}}{Z_{T1} + Z_{T1,sat}^{*}} \tag{4.11}$$

$$\Gamma_{dM} = \frac{R_{dM} - R_{dM,sat}}{R_{dM} + R_{dM,sat}} \tag{4.12}$$

From (4.5) and (4.8), the above reflection coefficients, evaluated at the breakpoint, can be derived as follows:

$$\Gamma_{T1,cri} = \frac{Z_{T1,cri} - Z_{T1,sat}}{Z_{T1,cri} + Z_{T1,sat}^{*}} = -\frac{\alpha_C + j\alpha x_n}{\alpha_C + 2 - j\alpha x_n} \tag{4.13}$$

$$x_n = \frac{X}{R} \tag{4.14}$$

$$\Gamma_{dM,cri} = \frac{R_{dM,cri} - R_{dM,sat}}{R_{dM,cri} + R_{dM,sat}} = \frac{\beta_d - 1}{\beta_d + 1} \tag{4.15}$$

As $R_{dM,cri}$ and $R_{dM,sat}$ are both pure resistive and $R_{dM,cri} > R_{dM,sat}$, $\Gamma_{dM,cri}$ should be positive real and numerically equal to the modulus of $\Gamma_{T1,cri}$. Hence, we have:

$$\left|\Gamma_{T1,cri}\right| = \sqrt{\frac{\alpha_C^{\,2} + \left(\alpha_C x_n\right)^2}{\left(\alpha_C + 2\right)^2 + \left(\alpha_C x_n\right)^2}} \tag{4.16}$$

$$\beta_d = \frac{1 + \left|\Gamma_{T1,cri}\right|}{1 - \left|\Gamma_{T1,cri}\right|} \tag{4.17}$$

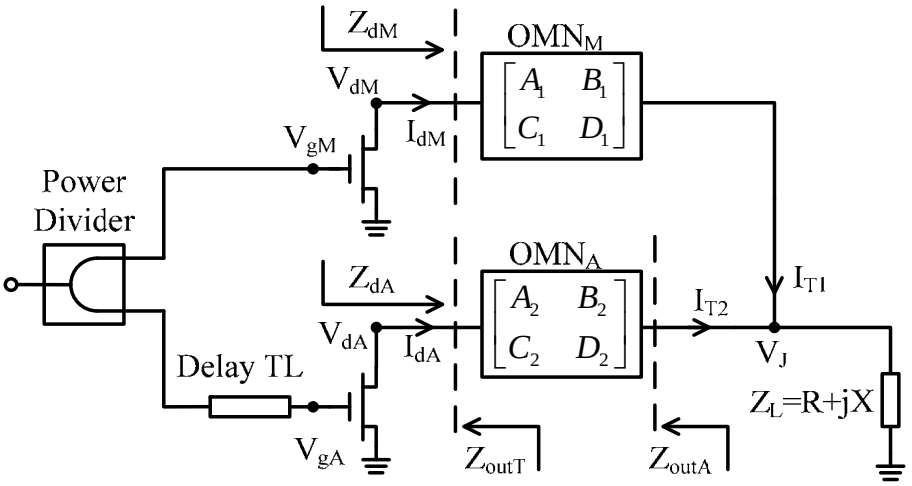
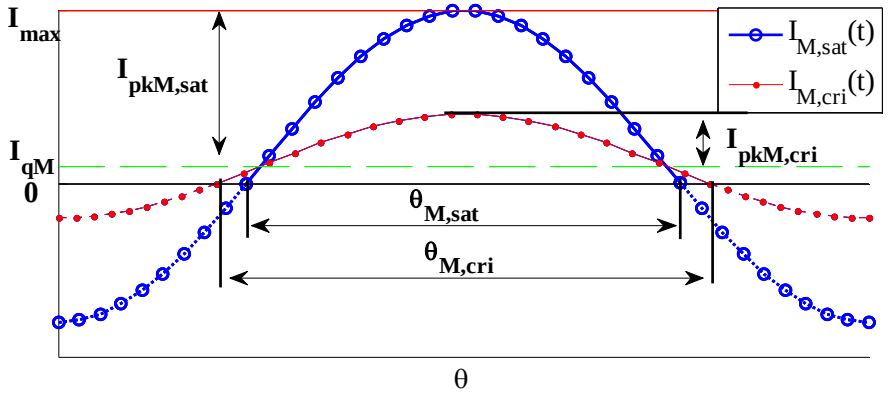


Fig. 4.4 Simplified circuit topology of the proposed DPA

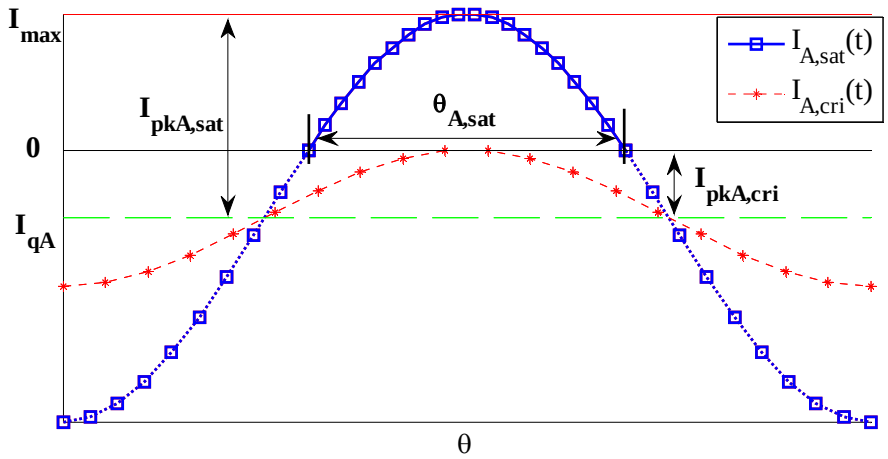
4.1.3 Derivation of operation parameters and drain loads

This study is based on DPA with complex combining load and equal-cell configuration. It is further assumed that the Main device is biased in Class-AB mode

whereas the Auxiliary device is operated in Class-C. As illustrated in Fig. 4.4, the input signal is split into two with a specific Power Splitting Ratio (PSR). A delay line is added to the Auxiliary branch to ensure proper combining of I_{T1} and I_{T2} (in-phase). Moreover, Z_{outT} denotes the output impedance of the Auxiliary device in off-state (infinite for ideal device); and Z_{outA} represents the output impedance of the Auxiliary branch (open circuit is assumed).



(a)



(b)

Fig. 4.5 Drain current waveforms: (a) Main device; (b) Auxiliary device

Fig. 4.5 shows the drain current waveforms of both devices (truncated sine-wave),

where I_{qM} and I_{qA} denote the quiescent currents; I_{pkM} and I_{pkA} are the current swings (which are proportional to V_{gM} and V_{gA}); θ_M and θ_A represent the conduction angles. Meanwhile, the voltage splitting ratio is defined by (4.18).

$$\sqrt{PSR} = \frac{V_{gM}}{V_{gA}} = \frac{I_{pkM}}{I_{pkA}} \tag{4.18}$$

Mathematically, these current waveforms can generally be described as follows ($\theta = \omega t$):

$$I_d(t) = \begin{cases} I_q + I_{pk}\cos\theta & -\frac{\theta_C}{2} < \theta < \frac{\theta_C}{2} \\ 0 & otherwise \end{cases} \tag{4.19}$$

If I_q and I_{pk} are known in priori, the corresponding conduction angle (θ_C), dc level (I_{dc}) and amplitude of the fundamental component (I_1) can simply be evaluated by the following expressions.

$$\theta_C = \cos^{-1}\left(\frac{-I_q}{I_{pk}}\right) \tag{4.20}$$

$$I_{dc} = \frac{\left(I_q + I_{pk}\right)\left(2\sin\left(\frac{\theta_C}{2}\right) - \theta_C\cos\left(\frac{\theta_C}{2}\right)\right)}{2\pi\left(1-\cos\left(\frac{\theta_C}{2}\right)\right)} \tag{4.21}$$

$$I_1 = \frac{\left(I_q + I_{pk}\right)\left(\theta_C - \sin\left(\frac{\theta_C}{2}\right)\right)}{2\pi\left(1-\cos\left(\frac{\theta_C}{2}\right)\right)} \tag{4.22}$$

To ensure Doherty operation and maximum power output [13], the following conditions are further imposed, where I_{MAX} represents the maximum current rating of

the devices.

$$I_{qM} + I_{pkM,sat} = I_{MAX} \tag{4.23}$$

$$I_{qA} + I_{pkA,sat} = I_{MAX} \tag{4.24}$$

$$I_{qA} + I_{pkA,cri} = 0 \tag{4.25}$$

By combining (4.18), (4.24) and (4.25), the following is obtained:

$$\frac{I_{pkA,sat}}{I_{pkA,cri}} = \frac{I_{MAX} - I_{qA}}{-I_{qA}} = \frac{I_{pkM,sat}}{I_{pkM,cri}} \tag{4.26}$$

For pre-specified values of I_{qM} and I_{MAX}, $I_{pkM,sat}$ is first calculated by (4.23). Through (4.20) and (4.22), the fundamental component of the Main current (at saturation) can be extracted ($I_{dM,sat}$). To determine the corresponding values of α_c, *PSR* and I_{qA} for a given x_n, an iteration procedure is applied. With α_c = 1 (initial value), β_d is evaluated via (4.16) and (4.17). Subsequently, $I_{dM,cri}$ is derived from (4.3). Then, $I_{pkM,cri}$ is reversely calculated by solving (4.20) and (4.22). Since $I_{pkM,sat}$ and $I_{pkM,cri}$ are both found, I_{qA} and $I_{pkA,sat}$ may be evaluated by (4.24) and (4.26) while *PSR* is computed using (4.18). Similarly, the fundamental component of the auxiliary current ($I_{dA,sat}$) can be determined via (4.20) and (4.22). And according to (4.2), an updated value of α_c is generated. The above procedure is re-iterated with the new value of α_c until a converged solution is observed. Finally, the OBO range may be calculated by (4.5). If the phase of I_{dM} is set equal to zero, the optimum drain loads (normalized by $V_{MAX}/2I_{MAX}$) for maximum output power are simply given by the following formulas.

$$R_{dM,sat} = \frac{I_{MAX}}{I_{dM,sat}} \tag{4.27}$$

$$R_{dM,cri} = \beta_d R_{dM,sat} \tag{4.28}$$

$$R_{dA,sat} = \frac{R_{dM,sat}}{\alpha_C} \tag{4.29}$$

For illustration, Table 4.1 shows the computed parameters as a function of x_n for $I_{qM} = 0.02 I_{MAX}$. In case of conventional Resistive Combining Load (RCL) DPA ($x_n = 0$), the dynamic load span is solely determined by the current ratio ($\beta_d = 1+\alpha$), and the only way to attain a higher value of OBO is to increase α_c (e.g. by using multiple cells or auxiliary device with enlarged periphery). On the other hand, by the adoption of complex combining load, the current ratio (α_c), the dynamic load span (in particular) and the achievable OBO can be substantially enhanced. Fig. 4.6 summarizes the design targets (impedance levels) of OMN_M and OMN_A which may be synthesized by well-known network theory and fine-tuned using computer optimization.

Table 4.1
Computed Operation Parameters for $I_{qM} = 0.02\ I_{MAX}$

x_n	α_c	β_d	OBO (dB)	$I_{pkM,cri}/I_{MAX}$	$R_{dM,sat}$	$R_{dM,cri}$	$R_{dA,sat}$	θ_{dA}
0	0.73	1.73	4.78	0.555	1.99	3.45	2.71	-90°
1	0.83	2.32	6.27	0.408	1.99	4.61	2.4	-121°
2	0.92	3.93	8.77	0.230	1.99	7.82	2.18	-138°
3	0.95	6.5	11.04	0.129	1.99	12.94	2.09	-148°

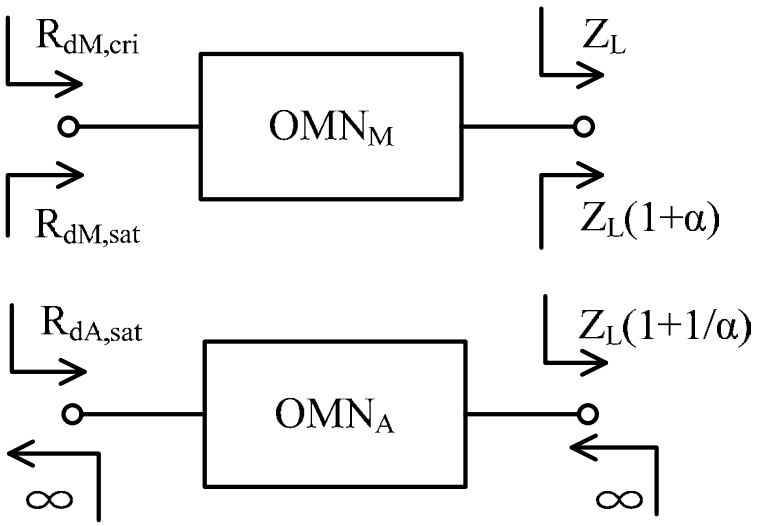


Fig. 4.6 Design targets (impedance levels) of matching networks

4.1.4 Determination of the phase of I_{dA}

With reference to Fig. 4.4, the following matrix equations can be formulated in terms of the ABCD parameters of the matching networks:

$$\begin{bmatrix} V_{dM} \\ I_{dM} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} Z_L & Z_L \\ 1 & 0 \end{bmatrix} \begin{bmatrix} I_{T1} \\ I_{T2} \end{bmatrix} \tag{4.30}$$

$$\begin{bmatrix} V_{dA} \\ I_{dA} \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} Z_L & Z_L \\ 0 & 1 \end{bmatrix} \begin{bmatrix} I_{T1} \\ I_{T2} \end{bmatrix} \tag{4.31}$$

Subsequently, by expanding (4.30) and (4.31), the ratio of drain currents (at saturation level) can thus be derived as:

$$\frac{I_{dA,sat}}{I_{dM,sat}} = \frac{(C_2 Z_L + D_2)\, I_{T2,sat} + C_2 Z_L\, I_{T1,sat}}{(C_1 Z_L + D_1)\, I_{T1,sat} + C_1 Z_L\, I_{T2,sat}} \tag{4.32}$$

By substituting (4.2) and (4.7) into (4.32), the phase of $I_{dA,sat}$ is simply calculated by (4.33).

$$\frac{I_{dA,sat}}{I_{dM,sat}} = \alpha_C e^{j\theta_{dA}} = \frac{(C_2 Z_L + D_2)\, \alpha_C + C_2 Z_L}{(C_1 Z_L + D_1) + C_1 Z_L\, \alpha_C} \tag{4.33}$$

Note that the absolute value of θ_{dA} is numerically equal to the electrical length of the

phase compensation section (delay line in Fig. 4.4). As x_n increases (Table 4.1), θ_{dA} deviates away from the original angle of -90° (Resistive load).

4.1.5 Derivation of drain efficiency curve

In the low power region ($I_{pkM} < I_{pkM,cri}$), the Auxiliary device is off and contributes no output power and dc consumption. Since Z_{dM} is fixed (= $R_{dM,cri}$), V_J and I_{T1} are simply given by:

$$\begin{bmatrix} V_J \\ I_{T1} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}^{-1} \begin{bmatrix} V_{dM} = R_{dM,cri} I_{dM} \\ I_{dM} \end{bmatrix} \tag{4.34}$$

Meanwhile, the fundamental component (I_{dM}) of the drain current waveform (Fig. 4.5) can be evaluated, for any arbitrary level of I_{pkM}, based on procedures mentioned in section II-C. As a result, the output power and dc consumption of DPA (low power region) can easily be calculated as:

$$P_{out} = \frac{1}{2} Re[V_J I_{T1}^*] \tag{4.35}$$

$$P_{dc} = \frac{V_{MAX} I_{dM,dc}}{2} \tag{4.36}$$

Inside the Doherty region ($I_{pkM} > I_{pkM,cri}$), Z_{dM} is dynamically modulated by the Auxiliary current. Similarly, through equation (4.30) and (4.31), I_{T1} and I_{T2} can be expressed as a function of I_{dA} and I_{dM}. Finally, the output power and dc consumption (Doherty region) are evaluated by (4.37) and (4.38).

$$P_{out} = \frac{\left|I_{T1} + I_{T2}\right|^2}{2} \mathrm{Re}\left(Z_L\right) \tag{4.37}$$

$$P_{dc} = \frac{V_{MAX}}{2}\left(I_{dM,dc} + I_{dA,dc}\right) \tag{4.38}$$

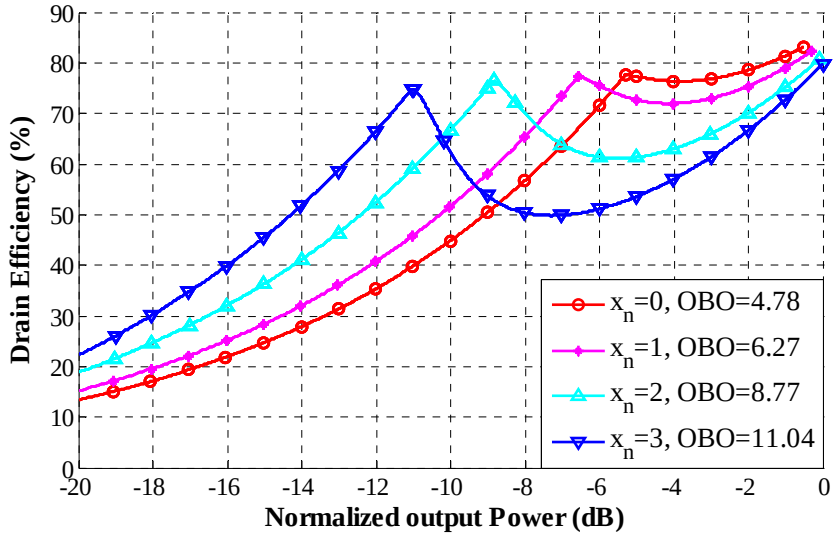


Fig. 4.7 Theoretical drain efficiency behavior

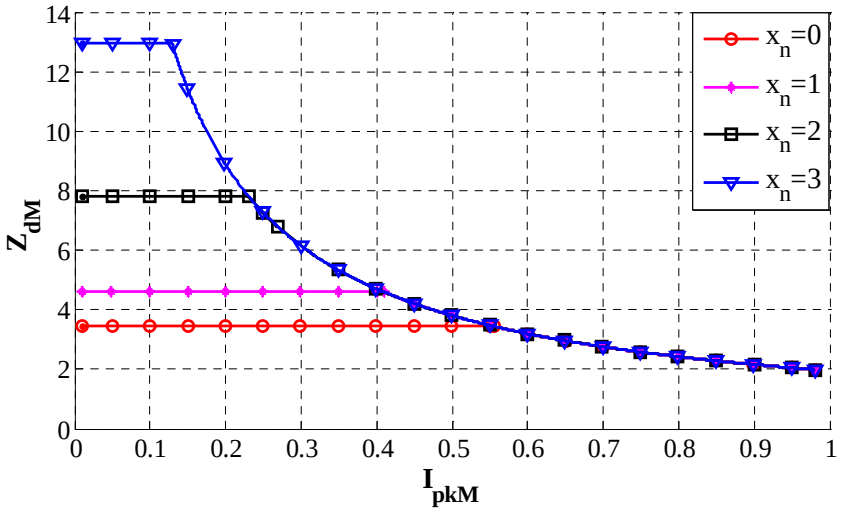


Fig. 4.8 Calculated Z_{dM} versus I_{pkM}

Fig. 4.7 shows the computed drain efficiency ($= P_{out}/P_{dc}$) of DPA which clearly demonstrates the impact of complex combining load on the range of OBO. For further illustration, Z_{dM} was extracted and plotted in Fig. 4.8 as a function of I_{pkM} (which is proportional to input signal strength). With lower level of $I_{pkM,cri}$ (due to the enlarged OBO), a higher Z_{dM} is clearly needed in maximizing the drain voltage swing of the Main device ($= I_{dM,cri} \times Z_{\mathrm{dM,cri}}$) for optimized efficiency. At any rate, a larger span of Z_{dM} will result in an extended value of OBO.

Table 4.2
Optimum Input and Output Loads of Main and Auxiliary Devices (CCL DPA)

Freq. (GHz)			**2**	**4**	**6**
CCL-eff	**Main Dev.**	**Output**	$Z_{dM,cri}$=15.04+60.23j (Pout=33.5 dBm)	67.94j	388j
			$Z_{dM,sat}$ =24.54+30.78j (Pout=39.5 dBm)		
		Input	4+4.6j	-7j	-24.6j
	Aux. Dev	**Output**	19.85+25.9j	209j	280j
		Input	8+6.5j	344.7j	400.9j
CCL-lin	**Main Dev.**	**Output**	$Z_{dM,cri}$=17.2+58.1j (Pout=33.5 dBm)	s.c.	
			$Z_{dM,sat}$ =23.9+30.1j (Pout=39.5 dBm)		
		Input	8+13j	s.c.	
	Aux. Dev	**Output**	19.55+25.7j	s.c.	
		Input	10+7.5j	s.c.	

4.2 Circuit Design and Simulation

For illustration, two CCL versions of Doherty power amplifier with OBO of 9 dB were designed. The first one (CCL-eff) is targeted for maximized efficiency and Power Utilization Factor (PUF), while the other design (CLL-lin) is aiming at a balanced performance of efficiency, linearity and bandwidth. For comparison purposes, a RCL DPA (RCL-eff) with OBO of 6 dB was also simulated, built and characterized. All the DPAs was simulated with the large signal model of Cree's GaN transistor (CGH40006S), and operated at 2 GHz with saturation power of 42 dBm and drain biasing voltage of 28V.

4.2.1 Extended DPA design for maximum efficiency and PUF

In the design of DPA with maximized power efficiency (CCL-eff and RCL-eff), the design strategy of harmonic tuned power amplifier [14][15] was adopted. Table 4.2 lists the optimum input and output loads of the Main and Auxiliary devices.

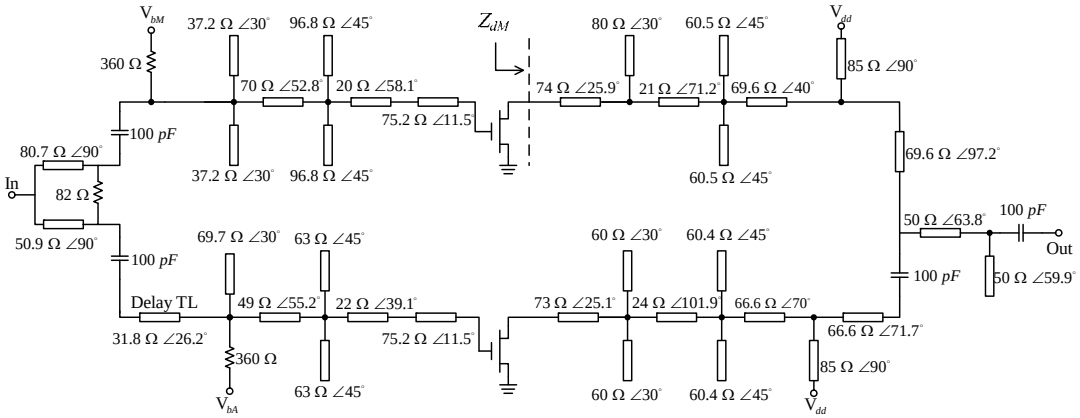


Fig.4.9 Schematic diagram of the proposed CCL-lin DPA

These values were extracted by using Harmonic Impedance Simulation tool, with an aim to optimize the fundamental and harmonic loads for maximum drain efficiency under the targeted output power level. Regarding the Main device, the simulation was conducted at a breakpoint level of 33.5 dBm (OBO = 8.5 dB) and saturation power of 39.5dBm. On the other hand, the Auxiliary device was optimized to give a saturation power of 39.5dBm. For the RCL design (RCL-eff), the optimum load (= 23.5 + 45.5*j*) of the Main device was evaluated at a breakpoint level of 36.5dBm (OBO = 5.5 dB).

Once the targeted impedances are known, we can then extract the required x_n that enable the extended load modulation. Since the optimum loads (Table 4.2) are all complex due to the presence of device parasitic, the resistive targeted loads ($R_{dM,cri}$ and $R_{dM,sat}$) have to be replaced by its complex counterparts ($Z_{dM,cri}$ and $Z_{dM,sat}$). Based on the device model available, the dynamic load span (β_d) seen at the intrinsic drain node may be deduced from the values of $Z_{dM,cri}$ and $Z_{dM,sat}$. With α_c = 1, the estimated value of x_n was found to be around 2.

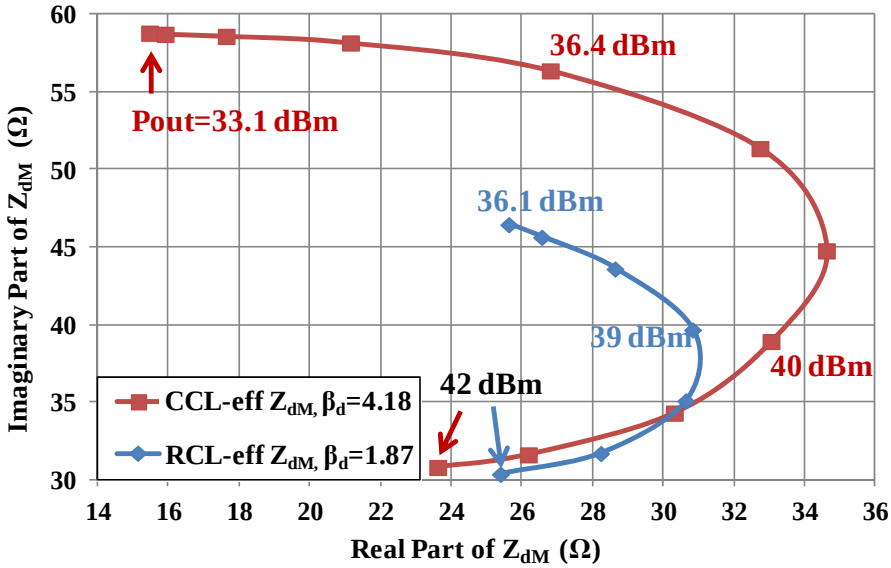


Fig. 4.10 Simulated load trace of Z_{dM} (Doherty region) of the CCL-eff and RCL-eff DPAs

Based on the synthesis method presented in [16], several versions of matching networks were designed with different values of *R*. Finally, *R* was selected to be 17 ohm due to the constraints on circuit size and loss. Fig. 4.9 shows the schematic diagram of the proposed CCL design. Note that the two open-stubs, with electrical lengths of 45° and 30°, are responsible, respectively, for the control of reactive loading of the devices at the 2nd and 3rd harmonic frequencies. For ease of fabrication, the choice of branch-line impedances was further restricted (from 20 to 90 ohm). The achievable α_c was extracted from the initial simulation, and slight adjustment of the circuit was conducted based on the new estimate of α_c. Meanwhile, the circuit was converted to layout and verified by using co-simulation. Fig. 4.10 shows the load trace of Z_{dM} (in Doherty region) for both DPA structures. The larger load span of Z_{dM} in CCL DPA corresponds to an enhanced β_d of 4.18.

Table 4.3
Simulation and Measurement Results of the Proposed and the Conventional DPA

Simulation Results (Continuous Wave)			
	CCL-eff DPA	RCL-eff DPA	CCL-lin DPA
x_n	2.25	0	1.9
α	0.91	0.9	0.92
β_d	4.18	1.87	3.77
OBO (dB)	8.89	5.42	8.7
DE @ Break Point	67.7% @ 33.1 dBm	71.4% @ 36.6 dBm	57.4% @ 33.1 dBm
DE @ Saturation	72.7% @ 42.0 dBm	74.8% @ 42.0 dBm	68.9% @ 41.8 dBm
Measurement Results (Continuous Wave)			
	CCL-eff DPA	RCL-eff DPA	CCL-lin DPA
OBO (dB)	9.15	5.5	8.8
DE @ Break Point	66.0% @ 33.2 dBm	70.7% @ 36.7 dBm	57.5% @ 33 dBm
DE @ Saturation	73.7% @ 42.3 dBm	75.3% @ 42.2 dBm	73.5% @ 41.8 dBm
Measurement Results (Modulated Signal)			
	CCL-eff DPA	RCL-eff DPA	CCL-lin DPA
DE (6.6dB WCDMA)	64.7% @ 37.1 dBm	65.5% @ 36.9 dBm	65.1% @ 37.2 dBm
DE (9.6dB WCDMA)	57.4% @ 33.2 dBm	49.4% @ 33 dBm	54.4% @ 33 dBm

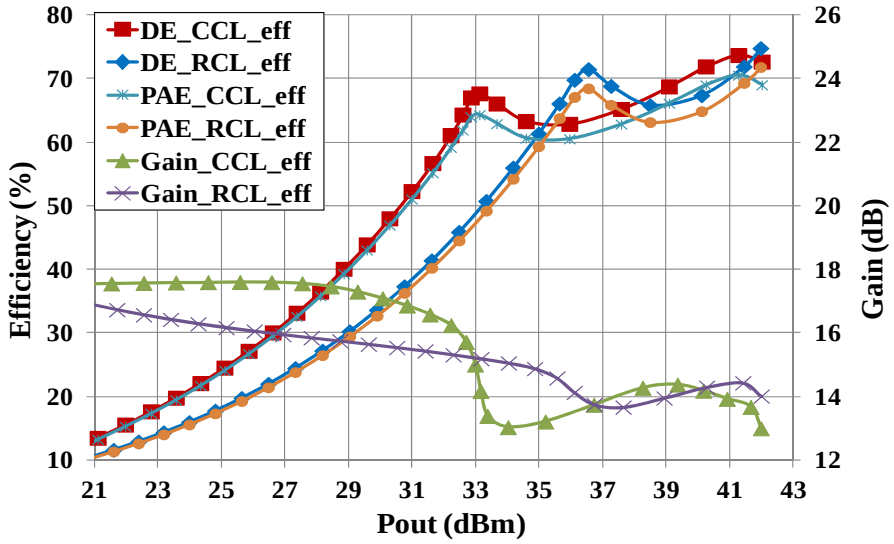


Fig.4.11 Simulated efficiency and gain performance of the CCL-eff and RCL-eff DPAs as a function of output power with CW signal

Fig. 4.11 shows the simulated efficiency and gain of CCL and RCL DPA as a function of output power. By the application of complex combining load, the proposed design was found to offer an extended OBO of 8.9 dB, a higher level of

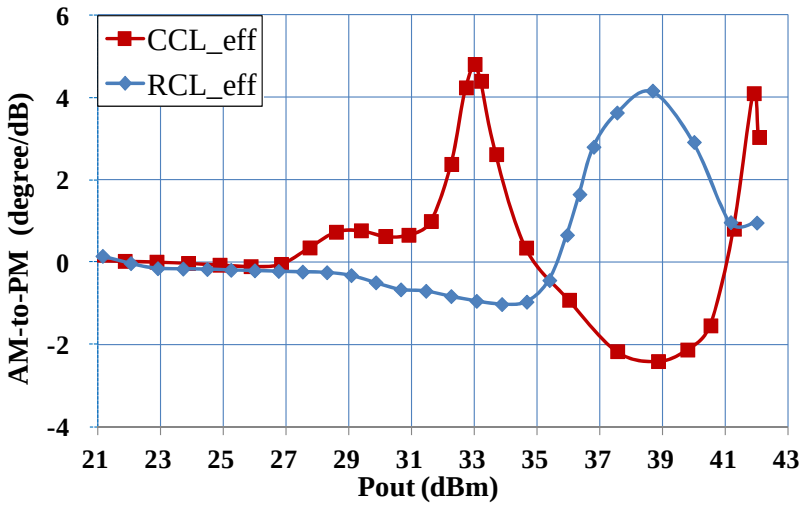


Fig. 4.12 Simulated AM-to-PM distortion of the CCL-eff and RCL-eff DPAs as a function of output power with CW signal

efficiency in the low power region, as well as good Doherty behavior. Regarding to gain performance, both designs exhibit large gain variation and AM-to-PM distortion (Fig. 4.12) inside the Doherty region as the devices are working in saturation to enlarge the first efficiency peak. Table 4.3 compares the simulated performance of these designs. In both cases, due to the adoption of Class C operation which lowers the output current of the Auxiliary device, the achievable value of α_c is limited to around 0.9. Fortunately, with the introduction of complex combining load, the dynamic load span has been remarkably increased from 1.87 to 4.18, and an improvement of OBO from 5.4 dB to 8.9 dB is observed.

4.2.2 Extended DPA design for optimum efficiency and linearity

In the CCL-lin DPA design, the harmonic loading requirement was relaxed and a two-tone load-pull simulation was conducted to obtain the optimum load impedance (fundamental) for a balanced efficiency-linearity performance (Table 4.2).

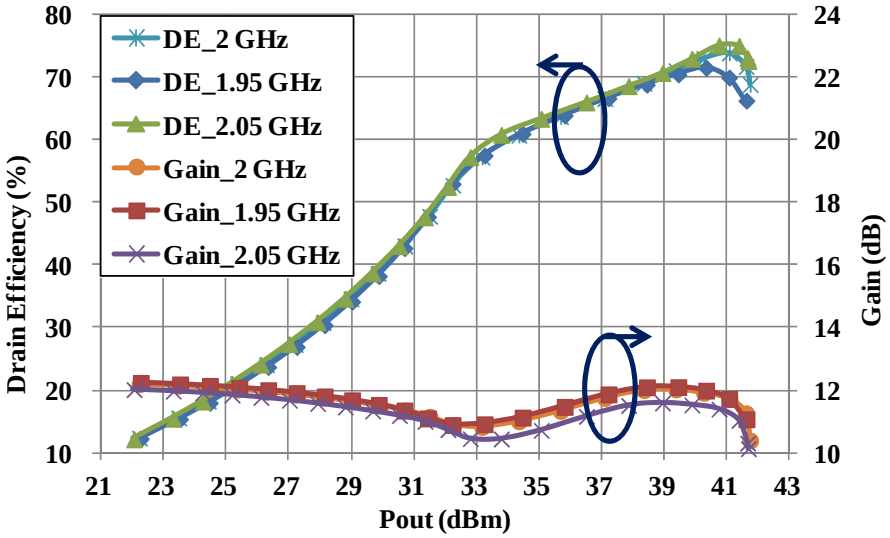


Fig.4.13 Simulated drain efficiency and gain performance of the CCL-lin DPA at multiple frequencies (CW)

Meanwhile, the length of delay line was slightly adjusted to further improve linearity by IM3 cancellation [8]. In order to ensure a proper DPA operation with sufficiently wide bandwidth, all the associated matching networks were synthesized based upon the two-ladder LC prototype and the Simplified Real Frequency Technique [17].

Fig. 4.13 shows the simulated drain efficiency and gain of the DPA as a function of output power at different frequencies (1.95, 2.0 and 2.05 GHz). Typical Doherty behavior with OBO range of about 8.8 dB is clearly observed over the concerned frequency band. The first efficiency peak (Break point) is close to 60% with a saturation power of almost 42dBm.

4.3 Experimental Verification

For experimental validation, the proposed (CCL-eff and CCL-lin) and the conventional (RCL) configurations were all constructed using Rogers substrate

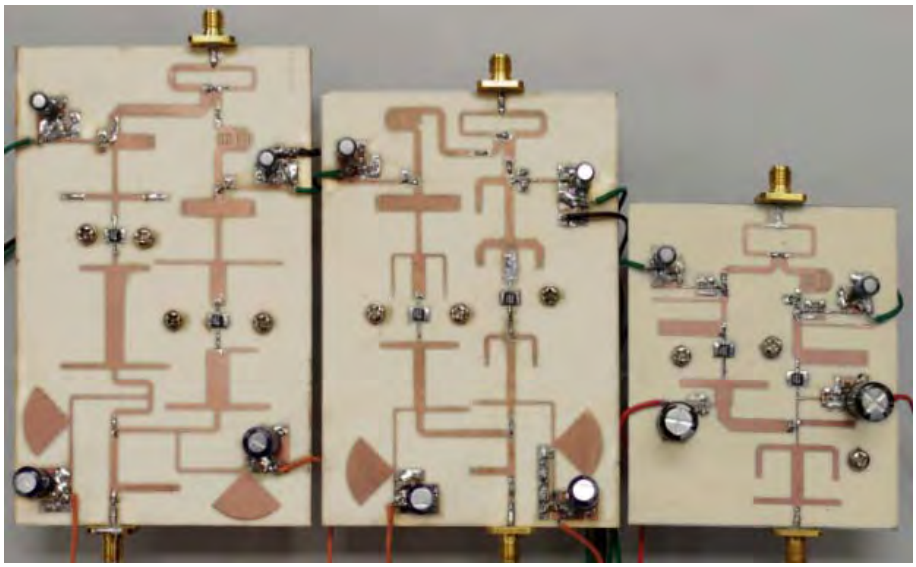


Fig. 4.14 Photograph of the CCL-eff DPA (left), RCL-eff DPA (middle) and CCL-lin DPA (right)

(RO4003C) with thickness of 0.813 mm and $\varepsilon_r = 3.55$. Fig. 4.14 shows the top view of the prototypes. The Main devices of all versions were biased in deep class-AB with a drain quiescent current of approximately 25 mA. According to the specifications [18], with a quiescent current of 100 mA (same operating frequency and drain voltage), this device (CGH40006S) is capable to deliver an output power of about 9W (39.5 dBm) with a gain compression of 3 dB. In order to maximize the first efficiency peak of CCL-eff (RCL-eff) DPA at an OBO of 9 dB (6 dB), a deep gate bias of -7 V (-7.4 V) is chosen for the auxiliary device, while the PSR (input power splitter) was set equal to -2 dB. In the CCL-lin version, for enhanced linearity, an auxiliary gate bias of -6 V was chosen (with PSR = 1) to allow the auxiliary device to be turned on before the main device enters saturation.

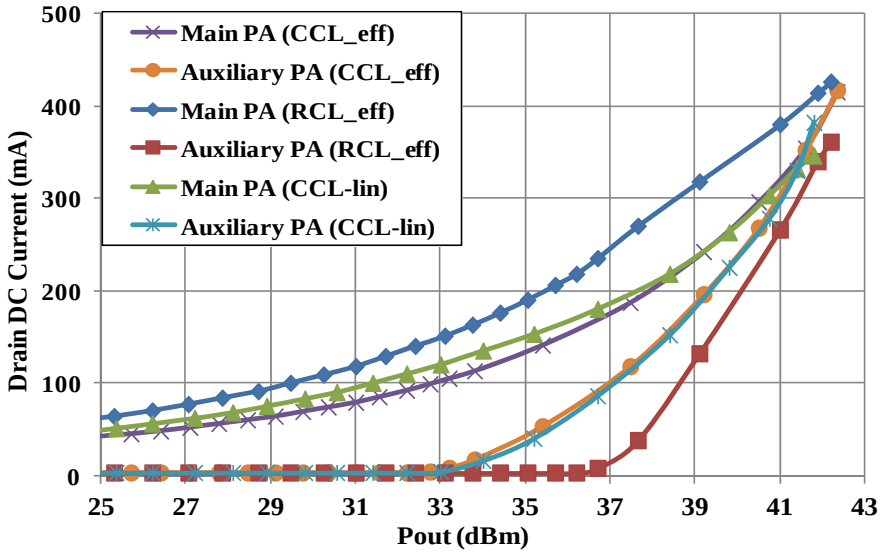


Fig. 4.15 Measured drain dc current consumption versus output power of all designs (CW)

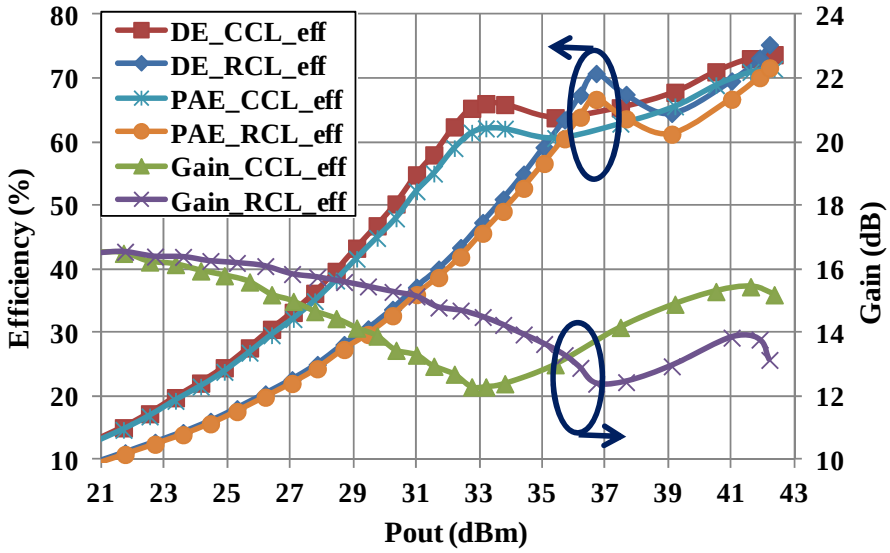


Fig. 4.16 Measured efficiency and gain performance of the CCL-eff and RCL-eff DPAs (CW)

4.3.1 CW Signal Measurement

Fig.4.15 shows the measured dc drain current profiles of the proposed and conventional DPAs under CW excitation. The gain and efficiency curves of CCL-eff and RCL-eff DPAs are given in Fig. 4.16. Note that the high level of gain compression (near breakpoint) is mainly attributed to the adoption of harmonic

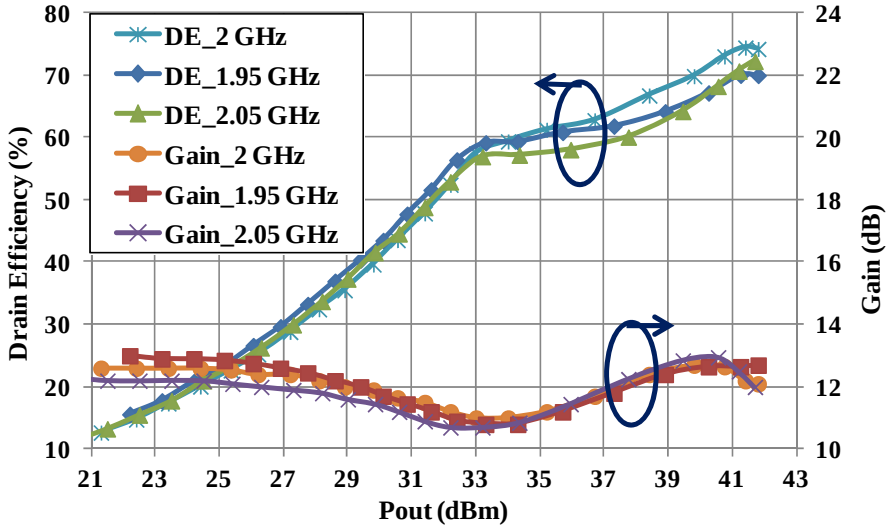


Fig. 4.17 Measured drain efficiency and gain performance of the CCL-lin DPA at multiple frequencies (CW)

voltage shaping technique (class J) for enhanced efficiency [14][15]. In compared to the RCL version, besides having excellent Doherty behavior, the proposed design can offer substantial improvement in overall drain efficiency. These results indicate that the proposed DPA can successfully extend the value of OBO from 5.7 dB (RCL) to 9.1 dB (CCL). Meanwhile, the measured drain efficiency (evaluated at the breakpoint) has dropped slightly from 71% (RCL) to 67% (CCL), which is in good agreement with the simulated results. This phenomenon is mainly caused by the imperfect open condition of the Auxiliary branch. In theory, the output impedance of the Auxiliary branch (Z_{outA}) should act as an open circuit (below the breakpoint). But in practice, it is finite (and has a real component) and consumes a small fraction of the output power. Since Z_{outA} and Z_L are connected in parallel, the amount of power loss in Z_{outA} will increase with x_n. From this point of view, a too large value of x_n (> 3) is prohibited. Nevertheless, the simulated and measured drain efficiencies of both configurations, near saturation (second peak), were all close to 74%. Both designs

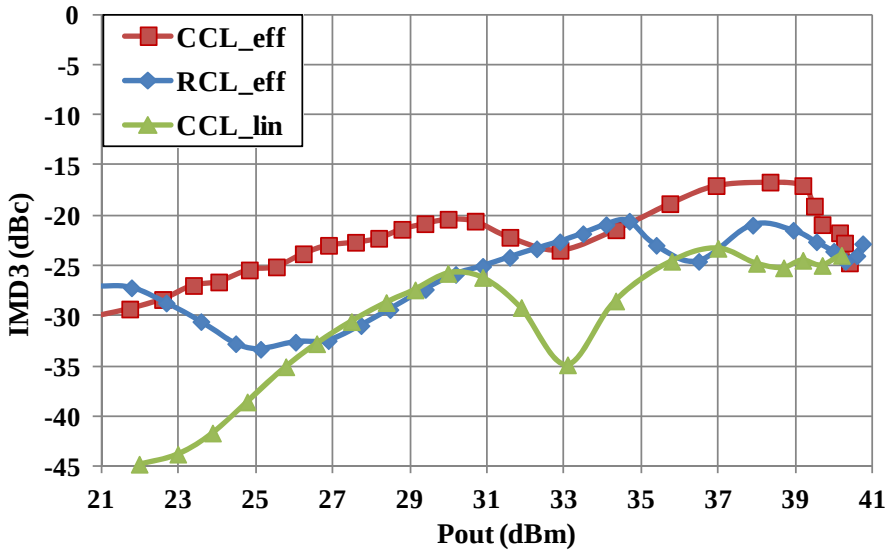


Fig. 4.18 Measured IMD3 performance of all designs (two-tone)

can deliver a saturated output power of approximately 42.3 dBm (≈ 17W).

Fig. 4.17 shows the measured drain efficiency and gain of the CCL-lin DPA as a function of output power at different operating frequencies. These results agree well with simulation (Fig. 4.13) in terms of efficiency peaks, saturation output power, gain levels and gain compression values. Since the auxiliary device is forced to turn on before the main device reaches maximum efficiency, the observed first efficiency peak appears to decrease slightly in compared with the CCL-eff DPA. Nevertheless, the gain compression was found to be lowered to 1.5 dB, which implies linearity improvement.

4.3.2 Two-tone Signal Measurement

The third-order inter-modulation (IMD3) performance of the proposed and conventional designs was also characterized. By applying a two-tone signal with a center frequency of 2GHz and tone spacing of 5 MHz, both amplifiers (CCL-eff and RCL-eff) were found to exhibit a relative IMD level (below carrier power) of around

-25 dBc over the Doherty region (Fig. 4.18). The poor linearity is due to the application of harmonic voltage shaping technique in raising the output power of the Main device (PUF ~ 1). For the CCL-lin DPA, owing to the improved gain compression and the introduced IM3 cancellation, a reduction of IMD3 level of 5-10dB can be observed over the entire operating range.

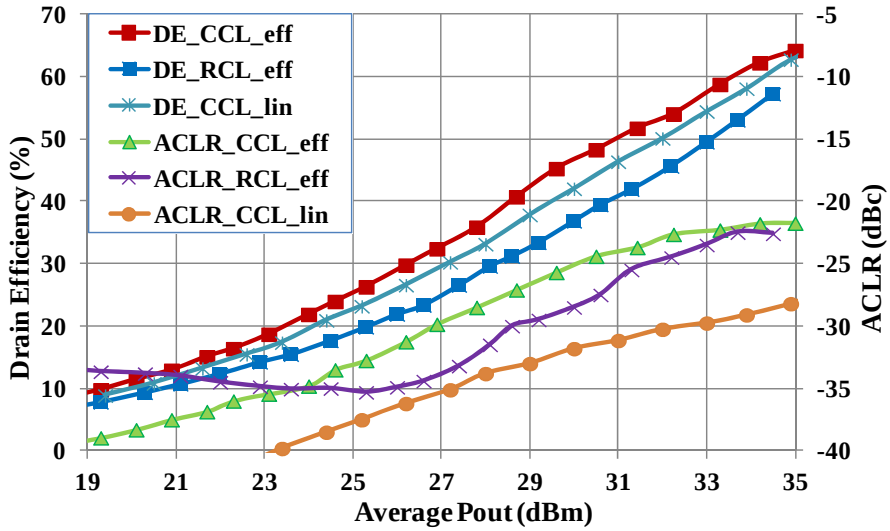


Fig. 4.19 Measured average drain efficiency and ACPR of all designs (9.6 dB PAPR WCDMA)

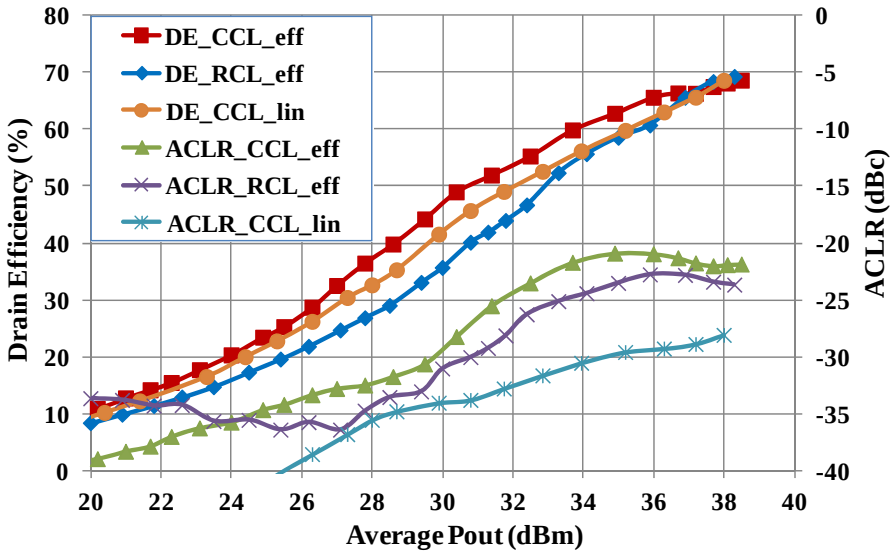


Fig. 4.20 Measured average drain efficiency and ACPR of all designs (6.6 dB PAPR WCDMA signal)

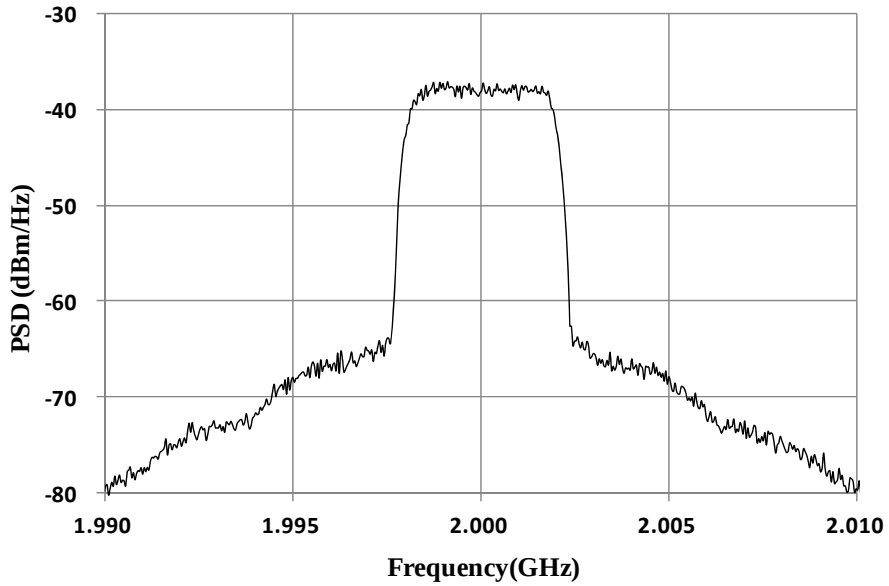


Fig. 4.21 Measured spectrum of WCDMA signal (9.6 dB PAPR) of the CCL-lin design at an average output power of 33.2 dBm.

4.3.3 Modulated Signal Measurement

To access the efficiency and linearity performance of DPA under modulated signal stimulation, measurements based upon single-carrier WCDMA signal with PAPR of 6.6 dB and 9.6 dB at 0.01% probability of complementary cumulative distribution function (CCDF) were employed. Average drain efficiency and ACLR (with 5 MHz offset) of all designs (CCL and RCL) were measured and depicted in Fig. 4.19 and 4.20. With PAPR = 9.6 dB (Fig. 4.19), both CCL designs (CCL-eff and CCL-lin) show distinct improvement in average power-efficiency (from 49% to 57/54%) at an output power of 33.2 dBm. In Fig. 4.21, the measured output spectrum (WCDMA with 9.6 dB PAPR) of the CCL-lin DPA indicates an ACLR level of approximately -30 dBc (at an average output power of 33.2 dBm). In summary, with high-PAPR signal excitation, the proposed method can offer an enhancement in average

Table 4.4
Comparison of some recent DPA designs with similar OBO range

Ref.	Freq. (GHz)	Topology	P_{avg} (dBm)	OBO (dB)	Signal	PAPR (dB)	Eff. (%)	ACLR
[8]	2.14	Multi-stage	38.5	11.5	WCDMA	11.5	53	-30
[9]	2.655	Multi-stage	42.5	8	WIMAX	7.8	55	-20
[19]	3.45	Modified LMN	40.5	9	LTE	8.5	44	-31
[14]	2.14	Asymmetrical	37.3	9	WCDMA	**NA**	48	-35
[4]	2.655	Asymmetrical	41.5	8	WIMAX	7.8	48	-23
This Work (CCL-eff)	2.0	Complex Combining Load	33.2	9.1	WCDMA	9.6	57.4	-23
This Work (CCL-lin)	2.0	Complex Combining Load	33	8.8	WCDMA	9.6	54.4	-30

power-efficiency over a wide range of output power (due to the extended OBO) with slight degradation (a few dB) in ACLR performance. Moreover, good linearity performance can be obtained with some tradeoff in efficiency.

Table 4.4 shows the measurement results of this work and some recent reports on DPA designs with similar OBO range and device technology. By comparison, the proposed design can offer the best efficiency with equal-cell architecture and high level of PUF (close to unity).

4.4 Conclusion

A new design approach, based upon complex combining load, to extend the high efficiency region of DPA has been presented. The relationship between the dynamic load span, current ratio and load reactance has been investigated. The evaluation of the major operation parameters and drain efficiency of the proposed method has also been addressed. Prototypes of DPA, with and without complex combining load, has been designed, built and characterized with different test signal formats. These

results validate the enhanced capability of the proposed method in relating to OBO and average-efficiency performance. Two-tone and ACLR measurements of various DPA designs have been conducted. The proposed technique allows the expansion of OBO without the need of multi-stage or asymmetric-cell implementation.

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Chapter 5

Broadband, Wide Efficiency Range, Doherty Amplifier Design Using Frequency-Varying Complex Combining Load

In the previous chapter, the DPA design based upon Complex Combining Load (CCL) has been demonstrated to extend the OBO range to beyond 9 dB, with the major drawback of small operating bandwidth (around 5%). In this chapter, the design of DPA with frequency-varying complex combining load is presented. Broadband operation and wide OBO range is attained by the proper selection of complex load space and optimal control of branch currents. For verification, the measured performance of a high efficiency DPA with 20% bandwidth and OBO of 9 dB is shown.

5.1 Proposed Methodology

Fig. 5.1 shows the simplified circuit diagram of DPA and impedance transformation of the output matching networks (OMN_M and OMN_A). For the CCL case, a non-zero x_n is used. The operation principle of CCL DPA has been detailed discussed in Chapter 4. Here, the analysis will be focused on the performance

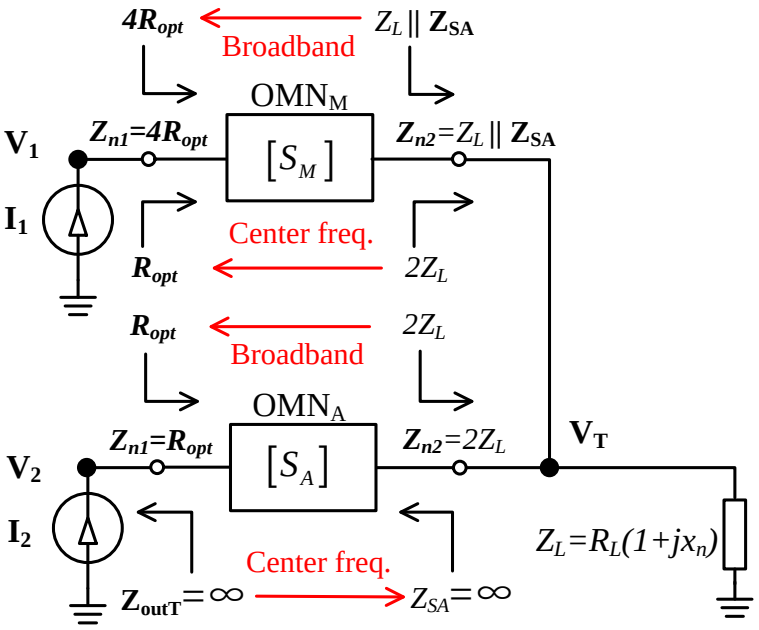


Fig. 5.1 Simplified circuit diagram of DPA and impedance transformation relationships of the output matching networks.

evaluation of DPA with a frequency-varying load, symmetrical topology (identical main and auxiliary devices), and a targeted OBO of 9 dB. Consequently, both devices will encounter the same optimum drain load at saturation (R_{opt}). At 9 dB back-off level, the effective load seen by the main device is simply equal to $4R_{opt}$. Without loss of generality, the saturated output power, the combining resistance (R_L), drain bias (V_{dd}), saturation drain current and center frequency (f_0) are all normalized to unity.

5.1.1 S-Parameter Formulation of Matching Networks

Referring to Fig. 5.1, in a narrow band design, OMN_M should transform the complex combining loads to the corresponding optimum impedance values (at the first and second efficiency peaks). However, such requirements of impedance

transformation could not be fulfilled simultaneously in broadband design. Since the first efficiency peak is more crucial to the average efficiency performance of DPA, the design priority of OMN_M is therefore given to the broadband generation of the first efficiency peak (9 dB back-off level). The efficiency performance at saturation can be optimized by the control of branch currents (to be explained later).

For the OMN_A design, broadband matching between the optimum drain load (R_{opt}) and the complex combining load ($2Z_L$) is assumed (saturation level). Furthermore, when auxiliary device is OFF, open circuit condition ($\mathbf{Z_{SA}} = \infty$) will be presented to the combining node at center frequency. With the reference impedance introduced in Fig. 5.1, the S-Parameters of OMNA and OMNM can be simplified as [1]:

$$S_{A(M)} = \begin{bmatrix} 0 & e^{-j\theta_{A(M)}} \\ e^{-j\theta_{A(M)}} & 0 \end{bmatrix} . \tag{5.1}$$

To a first approximation, θ_M and θ_A are both assumed to be linear function of frequency with non-zero group delay:

$$\theta_A = (f_n - f_0)\tau_A \tag{5.2}$$

$$\theta_M = f_n \tau_M \quad . \tag{5.3}$$

Note that τ_M can be calculated from (4.13) and (4.15). On the other hand, τ_A should be small enough to maintain a quasi-open $\mathbf{Z_{SA}}$ [2]-[4]. For illustration, a typical value of τ_A ($=\tau_M/3$) is adopted in the following analysis. Therefore, for a given x_n, S_A can be directly constructed from (5.1) and (5.2), and S_M can be deduced using (5.1) and (5.3).

5.1.2 Optimum broadband performance extraction

For the given x_n, the matching networks can be constructed for perfect back-off efficiency. Meanwhile, to ensure broadband Doherty operation at saturation level, the proper control of injection currents ($\mathbf{I_1}$, $\mathbf{I_2}$) are necessary. In the determination of the optimal relationship between I_1 and I_2 (both magnitude and phase difference), the following criteria are imposed:

(1) Output power of DPA at saturation is maintained at a constant level over the frequency band of interest (i.e. $P_{out} = |V_{Tsat}|^2 * real(1/Z_L)/2 = V_{dd}I_{MAX}/2$);

(2) To avoid degradation in load modulation span and linearity performance, the drain voltage swing (V_1 and V_2) has to be kept out of the knee region and the maximum allowance of drain voltage (of the active devices);

(3) Both main and auxiliary transistors are operating at the highest possible value of PUF (~ 100%) for cost effectiveness (i.e. I_{1sat}, I_{2sat}=I_{MAX}/2);

By circuit simulation, the optimal values of I_1 and I_2 (Fig. 5.2) were extracted as a function of frequency for x_n/x_{n0} = 0.8, 1 and 1.2 in which x_{n0} is the value of x_n under a fixed CCL given by (4.16) and (4.17). Fig. 5.3 and 5.4 show the corresponding behaviors of saturation drain voltage, saturation output power and PUF ($= 0.5I_{MAX}/max\ (I_{1sat}, I_{2sat})$). If class F operation is assumed ($V_{1(2)sat} \leq 1.15V_{dd}$), an estimated bandwidth of about 25% can easily be realized by the proper selection of x_n (frequency dependent). Under these circumstances, the variation of saturation output power was found to be less than 0.2 dB, with PUF > 85%, over the frequency range from $0.9f_0$ to $1.15f_0$.

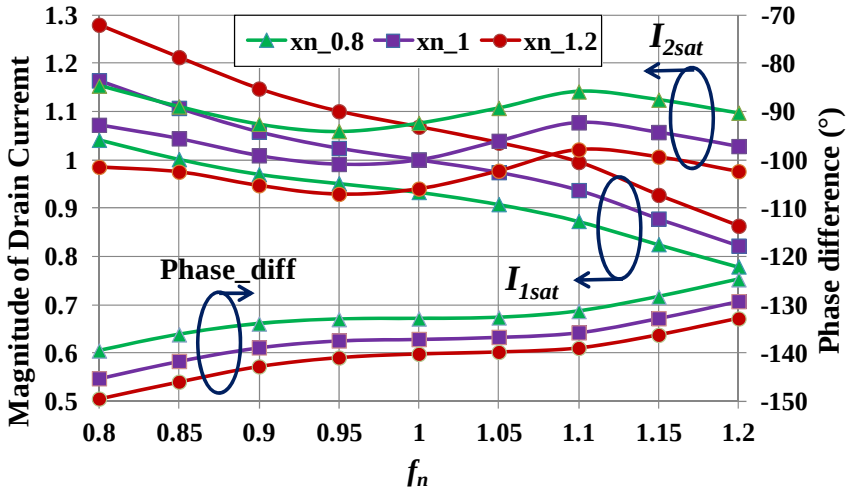


Fig. 5.2 Drain current control (magnitude and phase difference).

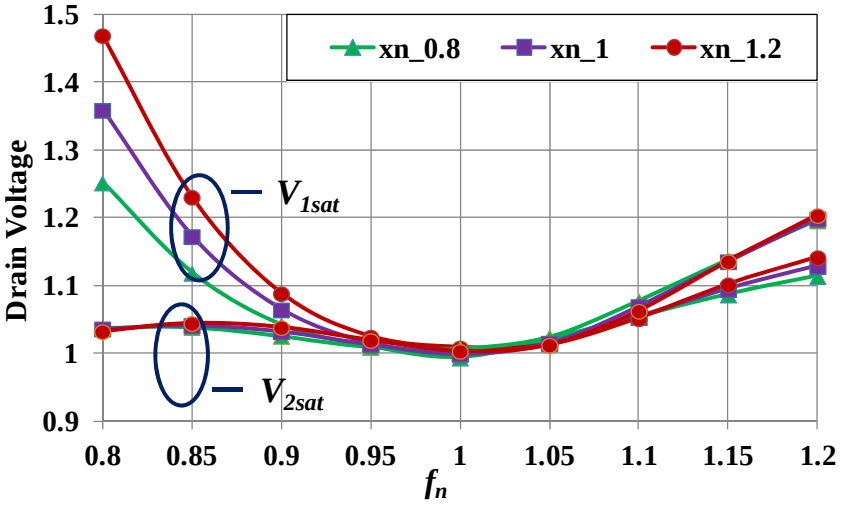


Fig. 5.3 Optimum saturation drain voltages.

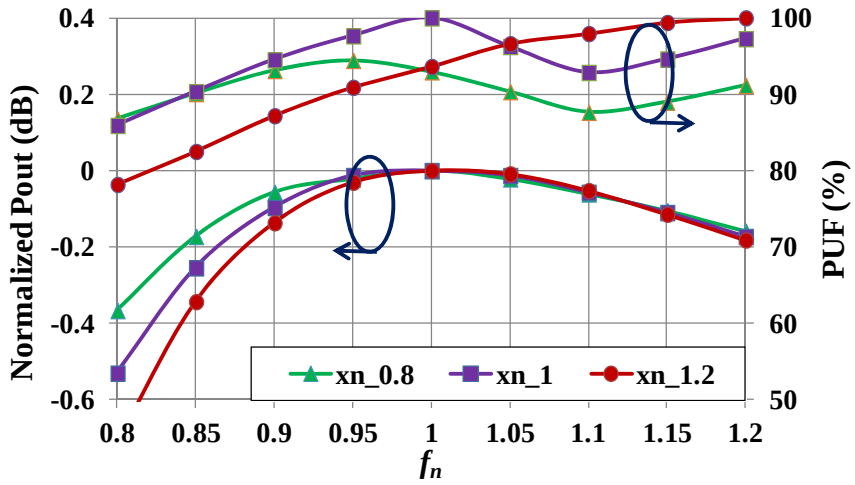


Fig. 5.4 Optimum saturation output power and PUF.

5.2 Design and Simulation

The previous section reveals that, with proper control of drain current, a frequency-varying CCL design can provide OBO extension in substantial bandwidth. For validation, a 1.8-2.2 GHz broadband DPA with targeted output power of 42 dBm and OBO of 8.5 dB is designed based on the proposed theory. All simulations are conducted using ADS in conjunction with the large signal model of Cree's GaN transistor CGH40006S.

5.2.1 Drain Bias Selection and Optimum Load Extraction

According to [5], the nominal output power of CGH40006S is 8 W (39 dBm) with a drain bias of 28V and quiescent current of 100 mA (Class AB operation). Due to the reduced output power in class C operation, the bias of the auxiliary device is slightly increased to 32V. As a result, the auxiliary device and the main device (drain bias=28V) will exhibit the same level of output power (39 dBm).

With the selected conditions, load-pull simulations are performed to extract the value of optimum drain load. The optimum loads of main device ($\mathbf{Z_{optcri}}$ and $\mathbf{Z_{optsat}}$) are evaluated at a back-off level of 8.5 dB (34 dBm) and saturation (39.5 dBm), respectively. For the auxiliary device, the saturation optimum load ($\mathbf{Z_{optaux}}$) is obtained at output power level of 39.5 dBm. The results of load-pull simulation are listed in Table 5.1.

TABLE 5.1
Optimum Drain Loads of Main and Auxiliary Devices

Freq. (GHz)	Z_{optcri}	Z_{optsat}	Z_{optaux}
1.8	23.3+63.2j	24.1+37.8j	27.1+27.4j
1.9	22.1+61.4j	24.3+34.6j	25.9+27.1j
2.0	20.8+59.1j	25.6+31.1j	25.2+26.5j
2.1	19.7+57.3j	24.7+29.71j	24.3+25.9j
2.2	18.8+55.5j	24.2+28.9j	22.8+25.4j

5.2.2 Frequency-varying CCL and Output Matching Network Design

With reference to Fig. 5.1, for broadband and high efficiency, OMN_M and OMN_A with complex combining load has to be adopted, and the frequency varying CCL is realized by OMN_C. Initially, a fixed combining load (x_{n0}=1.45) is selected for Z_L, and the output matching networks are synthesized by using SRFT. Then, to maximize the operation bandwidth, optimization of circuit parameters (line impedance and length) is applied with $0.8<x_n/x_{n0}<1.2$. The finalized output matching networks are shown in Fig. 5.5.

The Return Loss and phase responses of OMN_M and OMN_A are shown in Fig. 5.6, good matching performance can be obtained with small phase variation, which is essential for broadband DPA design [6]-[7].

As mentioned in Section 5.1, for wideband operation, the application of harmonic tuning (waveform shaping) of drain voltage (Class F and Class J) is necessary. In practice, the low-pass topology is adopted for OMN_C design to realize the required drain impedance. Table 5.2 listed the selected value of frequency varying CCL [8].

TABLE 5.2
Frequency Varying Complex Combining Load

Freq. (GHz)	x_n/x_{n0}	Z_L
1.8	1.09	12.5+19.7j
1.9	0.84	13.8+16.6j
2	0.86	11.9+14.6j
2.1	1.01	10.3+15.0j
2.2	0.81	10.8+12.7j

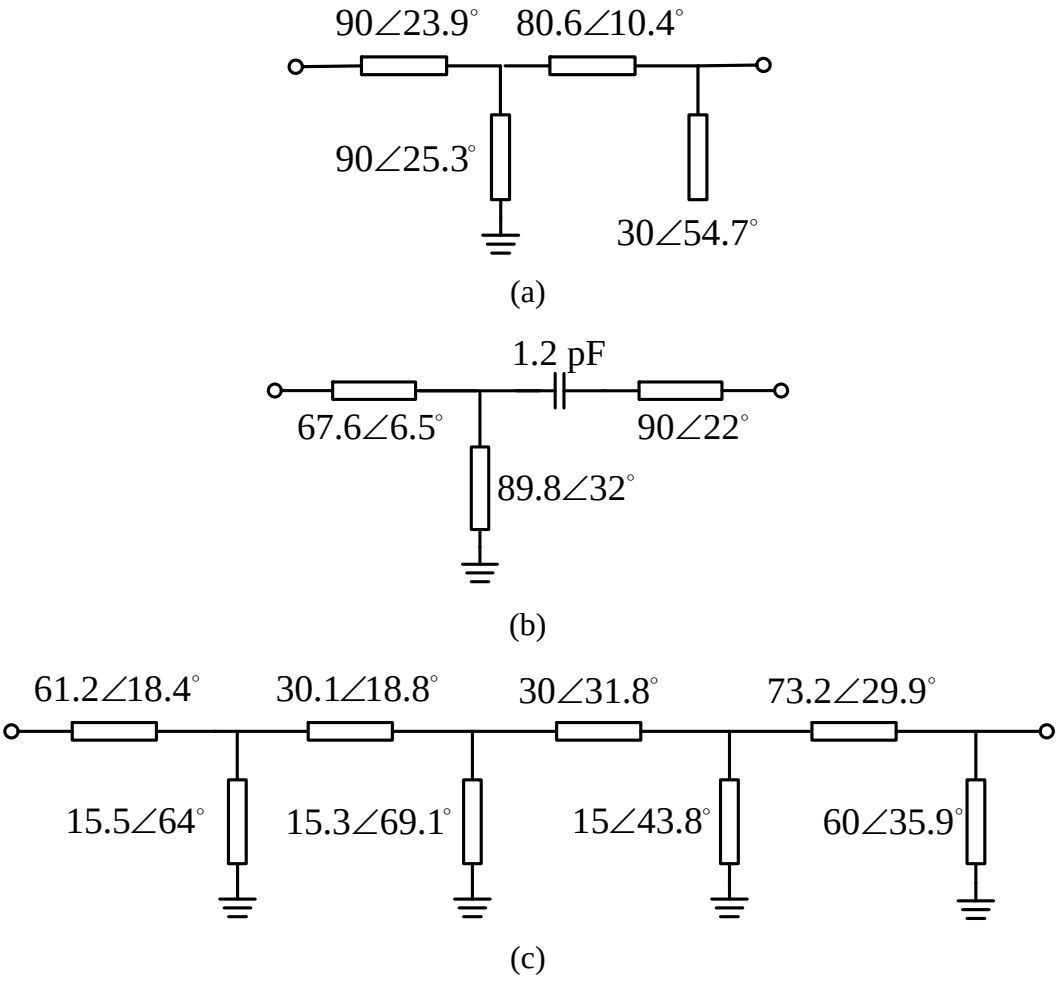
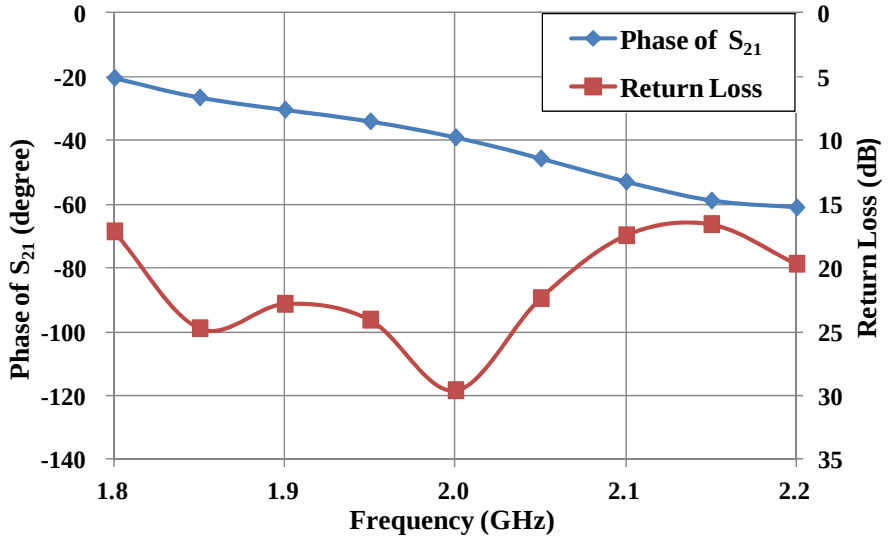
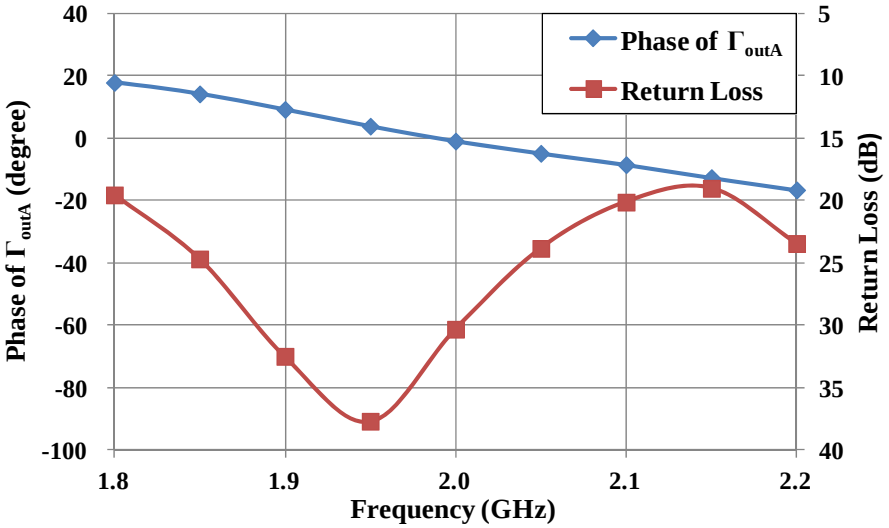


Fig. 5.5 Designed output matching networks: (a) OMN_M; (b) OMN_A; (c) OMN_C



(a)



(b)

Fig. 5.6 Simulated matching performance and phase response: (a) OMN_M; (b) OMN_A

5.2.3 Extraction of Current Relationship and Input Matching Network Design

In Section 5.3, the optimum drain currents (both magnitude and phase difference) for enhanced high efficiency range and bandwidth have been identified under different x_n value. However, in real devices, due to the presence of parasitic

capacitance (drain-source), the drain current sources (intrinsic model) are hard to access. Therefore, the gate voltage ratio (=$\mathbf{V_{gA}/V_{gM}}$) is being monitored instead. With reference to Fig. 5.7, two voltage sources (main and auxiliary inputs), having controllable magnitude and phase, were employed in the extraction process. The source impedances ($\mathbf{Z_{MS}}$ and $\mathbf{Z_{AS}}$) of the main and auxiliary devices were obtained through source-pull simulation (with optimized gain performance). The gate bias of the main device is set equal to –3 V which corresponds to a quiescent current of 35 mA (deep class AB), while the gate bias of the auxiliary device is a free parameter to be determined. Based upon Harmonic Balance simulation, at each frequency point, the drain efficiency was computed as a function of output power. Then, the gate bias, the source impedances and the input signals (both magnitude and phase) were finely tuned with an aim to optimize the output power, OBO and efficiency performance. A gate bias (auxiliary) of -6.6V and input signals of equal magnitude were subsequently obtained. Finally, based on the extracted source impedances and gate voltage ratio, the input matching networks were synthesized by using SRFT. Both extracted and realized results of gate voltage ratio are summarized in Table 5.3, which were found to be approximately 1.7 (magnitude of voltage ratio) and -130^{o} (phase of voltage ratio), over the frequency range from 1.8 to 2.2 GHz.

5.2.4 Simulation Result of Frequency-varying CCL DPA

Fig. 5.8 shows the TL circuit diagram of the whole DPA. After transform the TL circuit to layout version, the co-simulation can be conducted under the selected bias

TABLE 5.3
Summary of The Extracted and Realized Gate Voltage Ratio

Freq. (GHz)	Extracted voltage ratio	Realized voltage ratio
1.8	1.57/-129°	1.47/-122°
1.9	1.54/-30°	1.53/-128°
2	1.7/-134°	1.68/-134°
2.1	1.75/-128°	1.77/-139°
2.2	1.73/-129°	1.79/-134°

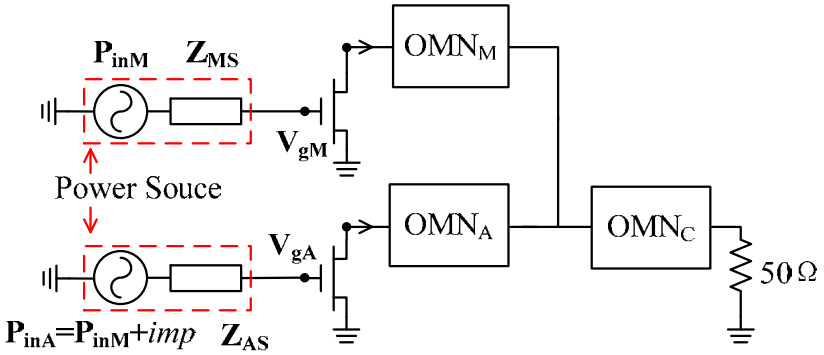


Fig. 5.7 Circuit configuration for optimal phase extraction

condition (V_{gm}=-3V and V_{ga}=-6.6V). Fig. 5.9 shows the simulated drain efficiency and gain performance as a function of output power. For all frequency points, the saturation output power is among 41.7 dBm to 42.3 dBm with the saturation gain level around 10 dB. Typical Doherty efficiency behavior can be observed with the 8.5 dB back-off efficiency of 56.8-58.4% and saturation level efficiency of 66-71%.

5.3 Experiments and Results

For experimental validation, the proposed frequency-varying CCL DPA with extended OBO and bandwidth has been fabricated on the Rogers substrate RO4003C ($\varepsilon_r = 3.55$, substrate thickness = 0.813 mm). The top-view of the prototype is shown

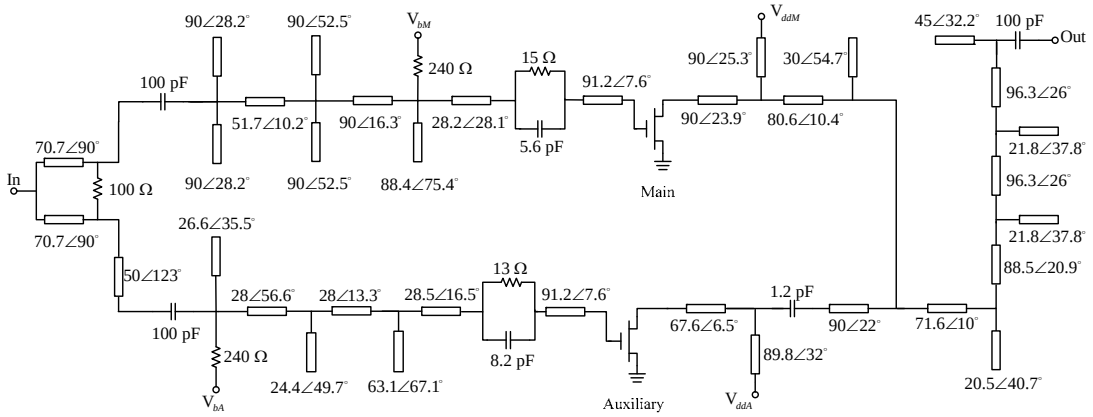


Fig. 5.8 Schematic diagram of the proposed frequency-varying CCL DPA

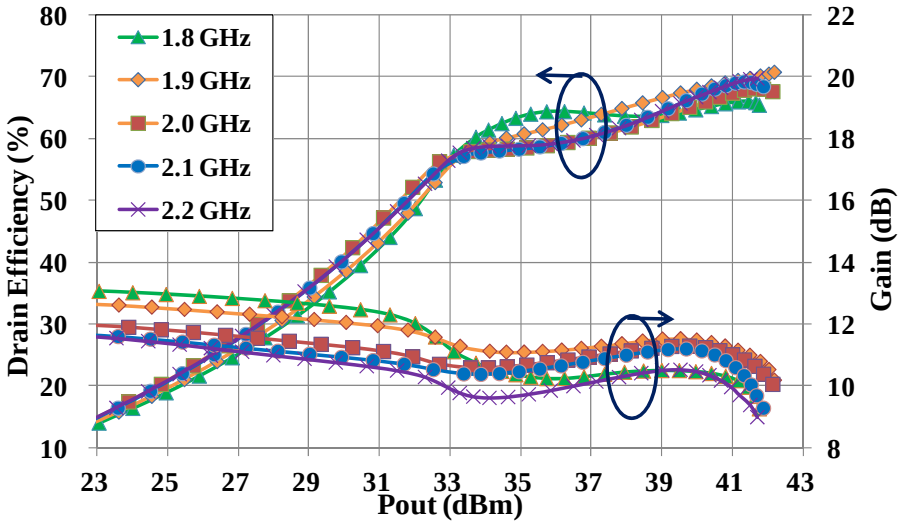


Fig. 5.9 Simulated drain efficiency and gain performance of the proposed design

in Fig. 5.10. For optimized gain flatness, the auxiliary gate bias has been adjusted to -6.2V. Fig. 5.11 shows the measured drain efficiency and gain performance of the prototype as a function of output power under CW stimulation. Good Doherty efficiency behavior can be observed with a gain compression of less than 2 dB. Over the entire frequency band (Fig. 5.12), the measured drain efficiencies were found to be over 69% (at saturation) and 55% (OBO = 8.5 dB), which corresponds well with

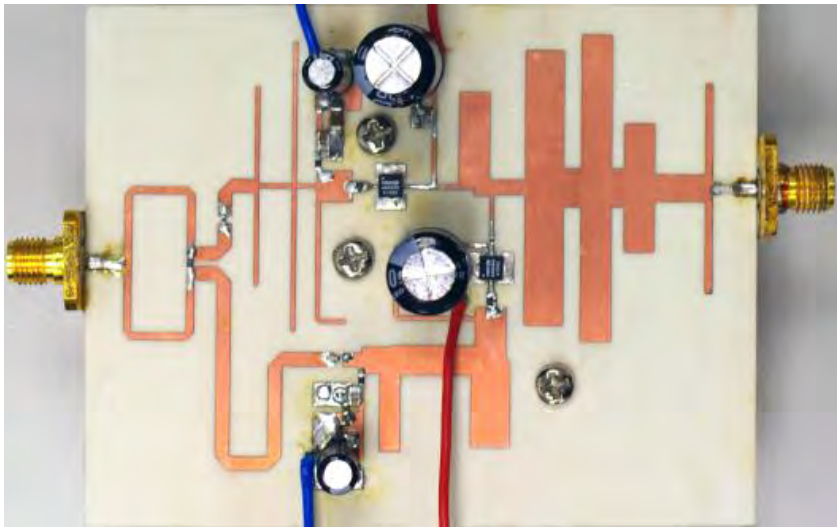


Fig. 5.10 Top-view of the fabricated DPA.

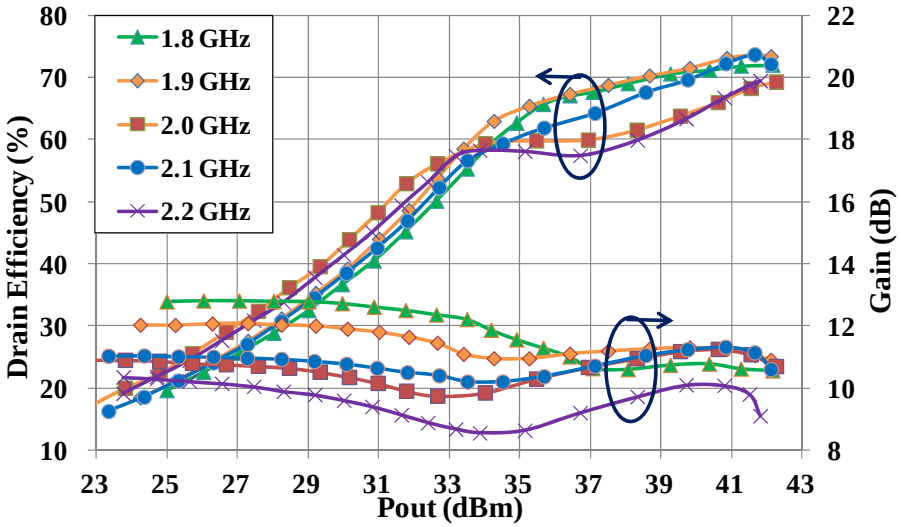


Fig. 5.11 Measured drain efficiency and gain performance of the proposed design.

the simulation result. Fig. 5.13 shows the measured drain efficiency and ACLR (5MHz offset) at an average output power of 33.5dBm with single carrier WCDMA signal excitation (9.6 PAPR). Excellent average drain efficiency (~ 56%) can be observed with ACLR of around -30 dBc. Table 5.4 compares the performance of broadband DPAs with resistive and complex (frequency-varying) combining loads. The proposed design offers the best performance in terms of saturation/back-off

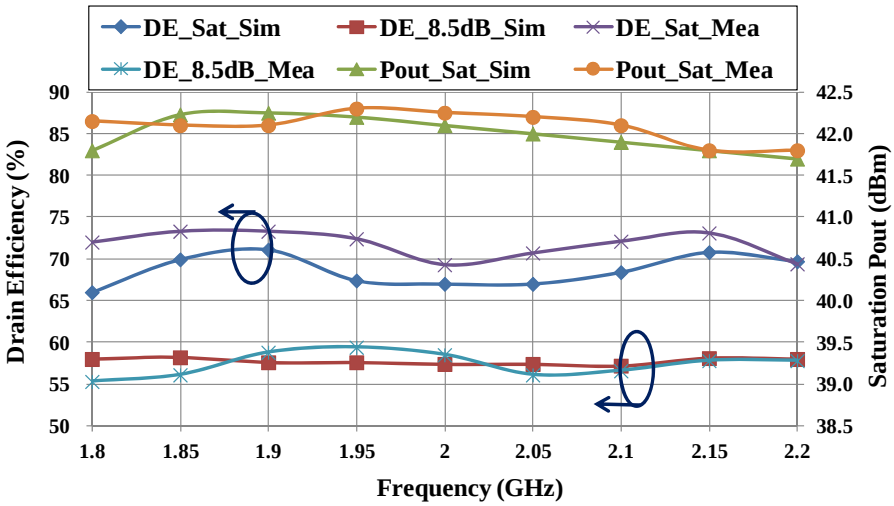


Fig. 5.12 Measured and simulated drain efficiency and saturated output power.

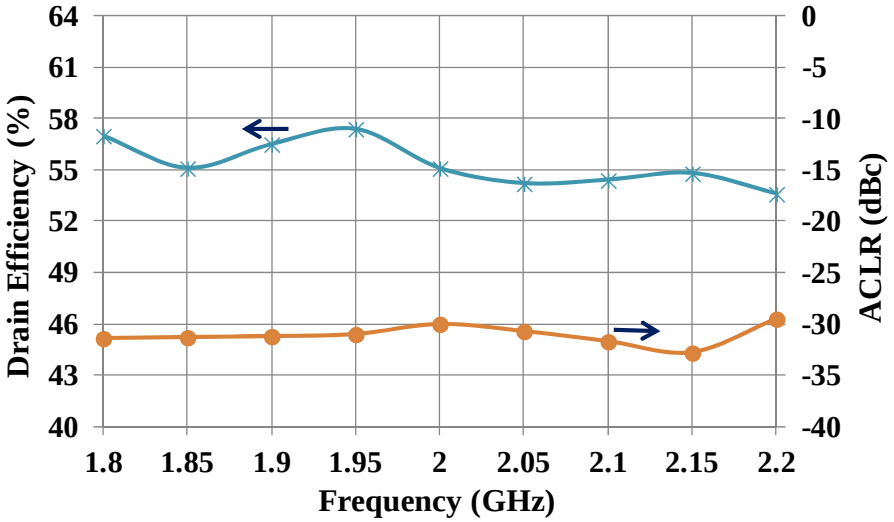


Fig. 5.13 Measured average drain efficiency and ACLR (WCDMA test signal at an average output power of 33.5 dBm).

efficiency, OBO range and PUF value.

5.4 Conclusion

A new DPA design using frequency-varying complex combining load and optimal input current control to achieve broadband operation and wide OBO range has been

Table 5.4
Comparison of Some Recent Broadband DPA Designs

Ref.	Freq. (GHz)	FBW	DPA Configuration	Technology	PUF	OBO (dB)	Sat. Pout (dBm)	DE at Sat. (%)	DE at back-off (%)
[2]	1.7-2.6	42%	Resistive Combining Load	GaN	1	5-6	42.1-45.3	50-55	41-55
[3]	0.7-1.0	35%	Resistive Combining Load	GaN	0.51	6	49-50.8	61-75	52-64
[4]	0.79-0.96	20%	Resistive Combining Load	Mixed GaN and LDMOS	0.5	9	~ 51	50-61	51-61
This Work	1.8-2.2	20%	Complex Combining Load	GaN	0.94	8.5-9	41.8-42.3	69-73	55-59

described. Prototypes of the proposed DPA has been designed, fabricated and characterized. Measured results indicate that the proposed method is capable of offering bandwidth of over 20%, OBO of 9 dB, PUF of 0.94, and enhanced efficiency performance.

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Chapter 6

Improving Power Utilization Factor of Broadband Doherty Amplifier by using Band-pass Auxiliary Transformer

Previous studies reveal that broadband Doherty behavior can be obtained at the expense of PUF (= 0.5). In this chapter, a novel DPA design based on auxiliary transformer is introduced. By inserting a transformer into the output matching network of the auxiliary amplifier, ideal PUF condition and broadband Doherty behavior can be achieved simultaneously. Moreover, the optimum design of the auxiliary matching network based upon band-pass topology is also addressed to minimize the impact of frequency dispersion. For validation, both the simulated and measured results of a 1.6-2.4 GHz, 20 W DPA with 6 dB back-off efficiency of over 55% and saturation efficiency of around 72% are demonstrated.

6.1 Theory

For sake of analyses, the following assumptions are adopted:

5) Ideal device model with zero knee voltage and parasitic. In other words, the optimum drain load for maximum output power is purely resistive;
6) Symmetrical DPA (identical main and auxiliary devices) is employed with the

same upper limits on breakdown voltage and current rating (V_{MAX} and I_{MAX}). Both devices are operating in Class B mode;

7) All higher voltage harmonics are short circuited and only the fundamental component is retained;

8) All matching networks are lossless and reciprocal.

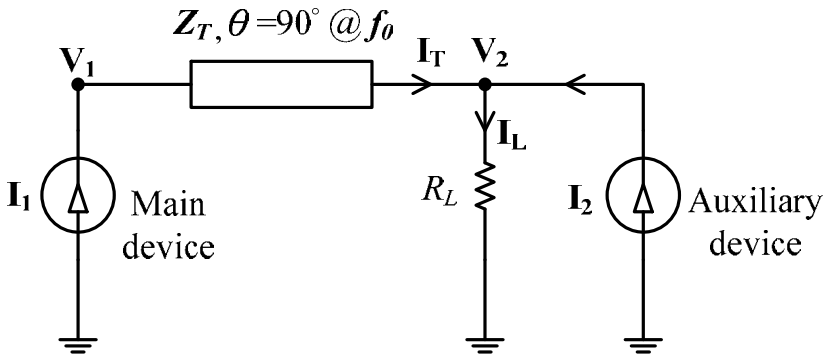


Fig. 6.1 Simplified schematic of Doherty power amplifier

6.1.1 PUF of Conventional DPA configurations

Referring to Fig. 6.1, by using ABCD-parameter representation, the relation between the drain voltages and currents of the main and auxiliary devices can be formulated as:

$$\begin{bmatrix} \mathbf{V_1} \\ \mathbf{I_1} \end{bmatrix} = \begin{bmatrix} jZ_T / R_L & jZ_T \\ j / Z_T & 0 \end{bmatrix} \begin{bmatrix} \mathbf{V_2} \\ -\mathbf{I_2} \end{bmatrix} \tag{6.1}$$

With OBO range of 6 dB, the load impedance of the main device under low power operation (i.e. I_2 = 0) is given by (6.2), where R_{opt} denotes the optimum load impedance of the Main device for a given dc bias voltage and saturation current

level.

$$\frac{Z_T^{\ 2}}{R_L} = 2R_{opt} \tag{6.2}$$

Furthermore, by combining equation (6.1) and (6.2), with the assumption that $\mathbf{I}_2$ lags $\mathbf{I}_1$ by 90º, the magnitudes of the saturation voltages and currents can simply be related as:

$$V_{2sat} = \frac{2R_L}{Z_T} V_{1sat} \tag{6.3}$$

$$I_{2sat} = \frac{Z_T}{2R_L} I_{1sat} \tag{6.4}$$

According to [1], PUF is defined by the ratio between the maximum output power of DPA and the two active devices (Class B operation is assumed):

$$PUF = \frac{P_{\max,DPA}}{P_{\max,M} + P_{\max,A}} = \frac{4V_{2sat} I_{2sat}}{V_{MAX} I_{MAX}} \tag{6.5}$$

Subsequently, with $Z_T = 2R_L$ (classical DPA design [2]-[3]), the main and auxiliary devices are expected to have the same saturation voltage ($V_{1\text{sat}} = V_{2\text{sat}}$) and current ($I_{1\text{sat}} = I_{2\text{sat}}$) levels. Therefore, with appropriate selection of drain bias (= $0.5V_{\text{MAX}}$), the power capacity of both devices can be fully deployed (PUF = 1). However, as suggested in [4] and [5], this configuration is not suitable for broadband operation, since the adopted quarter-wavelength transformer is band limited and severe

degradation in efficiency and output power can be observed. To maintain high performance over wide bandwidth, a different choice of characteristic impedance (Z_T=R_L) was suggested. Under low power operation (below the first efficiency peak), the load impedance seen by the main device is inherently independent of frequency (= $2R_{opt}$). Unfortunately, according to (6.3) and (6.4), the saturation voltages and currents of the main and auxiliary devices will become unequal (i.e. V_{2sat} = $2V_{1sat}$; and I_{2sat} = $0.5I_{1sat}$). In other words, the bias voltage of the main device has to be substantially reduced (V_{1sat} = $0.25V_{MAX}$), while only half of the current capacity of the auxiliary device (I_{2sat} = $0.25I_{MAX}$) is exploited. In consequence [1], this broadband topology performs sub-optimally with reduced PUF (= 0.5).

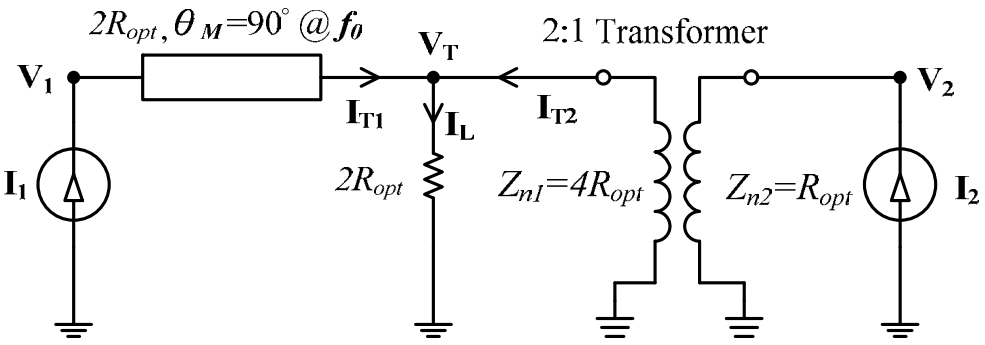


Fig. 6.2 Proposed DPA configuration with auxiliary transformer

6.1.2 Enhanced PUF by using Auxiliary Transformer

To improve PUF, a transformer is introduced into the auxiliary branch as depicted in Fig. 6.2. With the specific voltage ratio (2:1) of the transformer, the saturation voltages and currents of both devices are maximized (i.e. V_{1sat} = V_{2sat} = 0.5 $V_{MAX;}$ and I_{1sat} = I_{2sat} = 0.5 I_{MAX}). Therefore, the main and auxiliary devices can operate at full

capacity (PUF = 1) while ideal Doherty behavior is maintained over an extended bandwidth.

In practice, ideal transformer (broadband and low loss) is not available at microwave frequencies. Therefore, an impedance transformer with pre-selected port impedances ($Z_{n1}=4R_{opt}$, $Z_{n2}=R_{opt}$) is chosen to perform the required voltage scaling function. If the transmission phase response of the auxiliary transformer is denoted as θ_A ($\theta_A = 0$ only at f_0), its scattering-parameters can thus be expressed as follows [6]:

$$S_A = \begin{bmatrix} 0 & e^{-j\theta_A} \\ e^{-j\theta_A} & 0 \end{bmatrix} \tag{6.6}$$

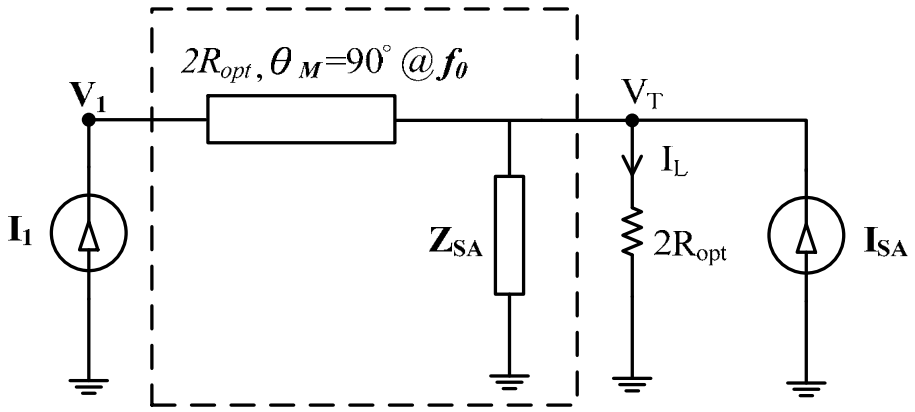
Accordingly, by using ABCD parameters, the dependency between the terminal voltages and branch currents of the auxiliary transformer can simply be written as:

$$\begin{bmatrix} \mathbf{V_T} \\ -\mathbf{I_{T2}} \end{bmatrix} = \begin{bmatrix} 2\cos\theta_A & j2R_{opt}\sin\theta_A \\ j\sin\theta_A / 2R_{opt} & \cos\theta_A / 2 \end{bmatrix} \begin{bmatrix} \mathbf{V_2} \\ -\mathbf{I_2} \end{bmatrix} \tag{6.7}$$

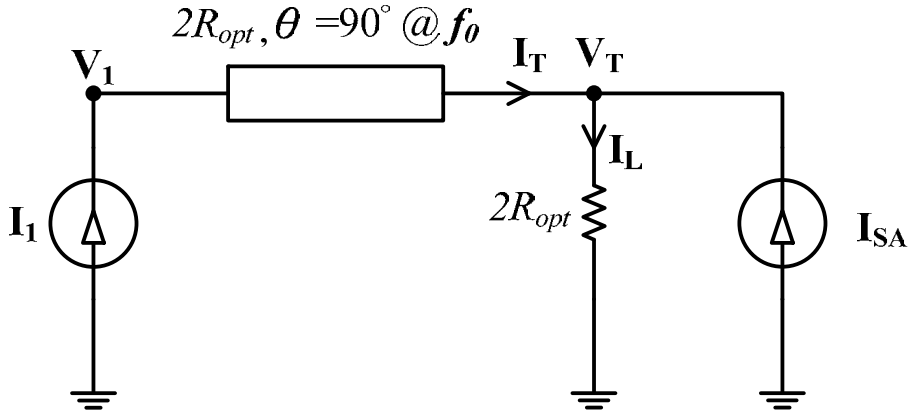
For further analysis, the transformer and the auxiliary current are replaced by its equivalent circuit as depicted in Fig. 6.3(a). The mathematical expressions of the shunt reactance ($\mathbf{Z}_{SA}$) and the modified current source ($\mathbf{I}_{SA}$) are given by (6.8) and (6.9). Note that the frequency response of the shunt reactance is similar to that of a parallel-tuned circuit ($\mathbf{Z}_{SA} = \infty$ at f_0).

$$\mathbf{I_{SA}} = \frac{\mathbf{I_2}}{2\cos\theta_A} \tag{6.8}$$

$$\mathbf{Z_{SA}} = \frac{4R_{opt}}{j\tan\theta_A} \tag{6.9}$$



(a)



(b)

Fig. 6.3 Proposed DPA with non-ideal transformer: (a) Simplified version; (b) Equivalent circuit.

To maintain broadband Doherty operation (first efficiency peak), the combined effect of TL_M (quarter-wavelength transmission line) and $\mathbf{Z_{SA}}$ is made equivalent to an ideal transmission line with characteristic impedance of $2R_{opt}$ and electrical length of 90º (at f_0 only), as depicted in Fig. 6.3(b). Note that, when the auxiliary device is off (I_2 = 0), the circuits in Fig. 6.1 and Fig. 6.3(b) are basically identical. To a first approximation, the electrical length (θ) of the equivalent line can be evaluated by (6.10), where θ_M corresponds to the phase response of TL_M; while the second term represents the transmission phase introduced by the shunt reactance (auxiliary

transformer).

$$\theta = \theta_M + \theta_A / 2 \tag{6.10}$$

6.1.3 Optimal Phase Control for Broadband Operation

With reference to Fig. 6.3(b), by the multiplication of ABCD matrices, the relation between the terminal voltages and branch currents can be obtained as:

$$\begin{bmatrix} \mathbf{V_1} \\ \mathbf{I_1} \end{bmatrix} = \begin{bmatrix} e^{j\theta} & j2R_{opt}\sin\theta \\ e^{j\theta}/2R_{opt} & \cos\theta \end{bmatrix} \begin{bmatrix} \mathbf{V_T} \\ -\mathbf{I_{SA}} \end{bmatrix} \tag{6.11}$$

Combining (6.8) and the second row of (6.11), we have:

$$\mathbf{V_T} = R_{opt}(2\mathbf{I_1} + \frac{\mathbf{I_2}}{\cos\theta_A}\cos\theta)e^{-j\theta} \tag{6.12}$$

For broadband Doherty operation (second efficiency peak), the saturation value of $\mathbf{V_T}$ has to be maximized over the frequency band of interest. Equation (6.11) and (6.12) implies that both the magnitude and phase control of $\mathbf{I_1}$ and $\mathbf{I_2}$ are required. Here, for the ease of DPA implementation, only the optimal control of phase is exploited based on the synthesis of matching networks with specific dispersion characteristics. If the phase difference between $\mathbf{I_1}$ and $\mathbf{I_2}$ is denoted as θ_Δ, the output current of the auxiliary device can thus be mathematically expressed as:

$$\mathbf{I_2} = \begin{cases} 0 & I_1 < 0.5I_{1sat} \\ (2I_1 - I_{1sat})e^{j\theta_\Delta} & I_1 \geq 0.5I_{1sat} \end{cases} \tag{6.13}$$

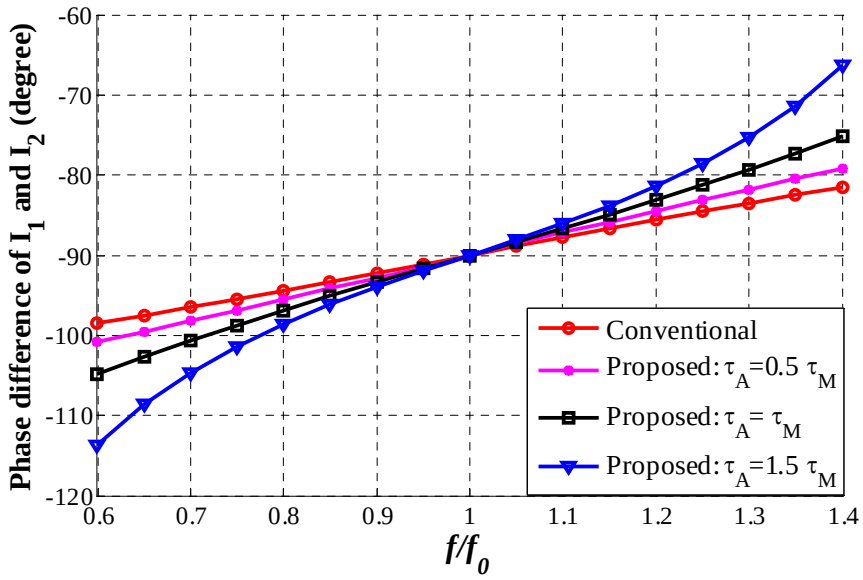


Fig. 6.4 Calculated phase difference as a function of frequency

By inserting (6.13) into (6.12), the value of $\mathbf{V_T}$ at saturation is simply given by:

$$\mathbf{V}_{\mathbf{Tsat}} = I_{1sat} R_{opt} (2 + \frac{\cos\theta}{\cos\theta_A} e^{j\theta_\Delta}) e^{-j\theta} \tag{6.14}$$

Based on the criteria of maximum output power (i.e. $|\mathbf{V}_{\mathrm{Tsat}}| = V_{\mathrm{MAX}} = 2I_{1\mathrm{sat}} R_{\mathrm{opt}}$), the optimal phase difference can be deduced from (6.14) and written as:

$$\cos(\theta_\Delta) = -\frac{\cos(\theta)}{4\cos(\theta_A)} \tag{6.15}$$

For illustration, Fig. 6.4 shows the calculated phase difference as a function of normalized frequency. It is further assumed that θ_{M} (= 90º at f_0) and θ_{A} (= 0º at f_0) are both linear function of frequency with non-zero group delays (τ_{M} and τ_{A}). It can be observed that the frequency response of the optimum phase difference strongly depends on the group delay of the auxiliary transformer. For closer examination, Fig. 6.5 and Fig. 6.6 show the corresponding saturation voltages ($V_{1\mathrm{sat}}$ and $V_{2\mathrm{sat}}$) of the

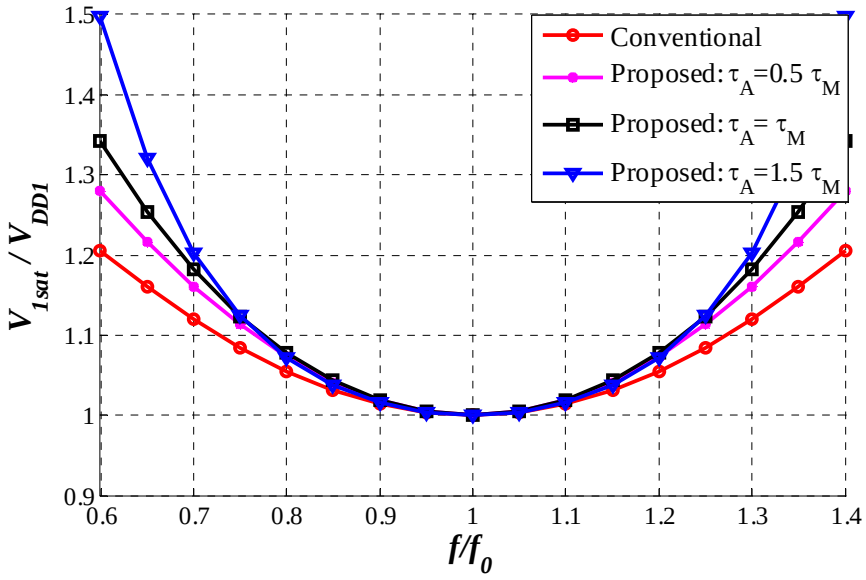


Fig. 6.5 Saturation drain voltage of main device versus frequency

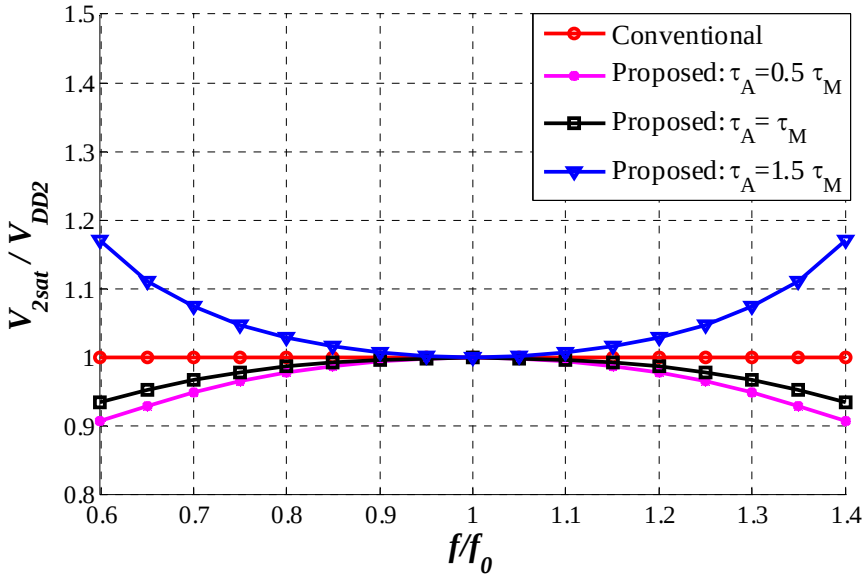


Fig. 6.6 Saturation drain voltage of auxiliary device versus frequency

proposed (with auxiliary transformer) and conventional (without auxiliary transformer) designs. In these plots, optimum phase control of $\mathbf{I_1}$ and $\mathbf{I_2}$ (θ_Δ) is enforced to compensate for the frequency dispersion of θ_M and θ_A. It can be seen that both voltage ratios are normalized to 1 at the center frequency. However, they deviate gradually from unity with increasing offset in frequency. It is because only

phase compensation is deliberately applied but not magnitude control (main and auxiliary currents). Nevertheless, the operating bandwidth is primarily determined by the overdrive of the main device (voltage ratio > 1). For instance, with a maximum voltage ratio of 1.1, a Fractional Bandwidth (FBW) of about 50% can be achieved. Meanwhile, the available bandwidth diminishes with increasing value of τ_A.

6.1.4 Drain Voltage Profiles and Efficiency Performance

Figs. 6.7-6.8 show the calculated drain voltage profiles as a function of Main current with equal group delay assumption ($\tau_M = \tau_A$). Both the proposed (with transformer) and conventional (without transformer) DPA configurations were examined at the center frequency and band edges ($0.75f_0$, f_0 and $1.25f_0$). It is also assumed that each device is operating at its highest possible rating (saturation voltage and current). In compared to the conventional circuit, the saturation voltage of the

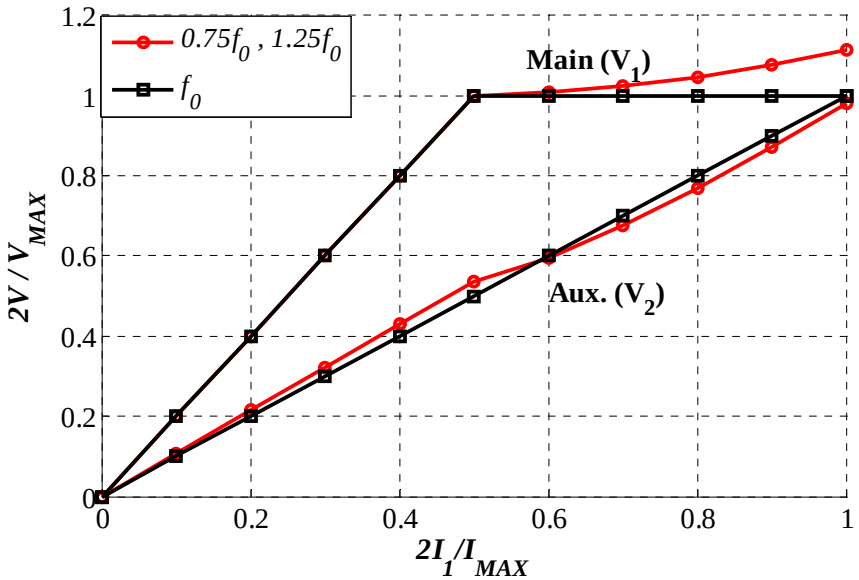


Fig. 6.7 Calculated drain voltage of proposed topology

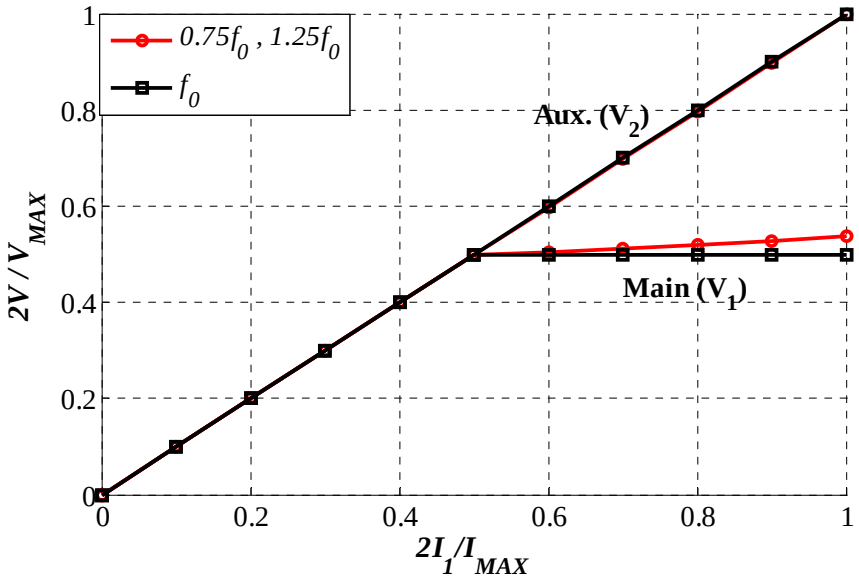


Fig. 6.8 Calculated drain voltage of conventional topology

main device in the proposed topology is double over the entire Doherty region, due to adoption of a higher drain bias. Meanwhile, the drain voltage profiles of the two auxiliary devices are very similar. At the band edges, the saturation voltage ratio of the main device (proposed) has increased slightly to 1.1, as expected. For further investigation, Fig. 6.9 illustrates the calculated Drain Efficiency (DE) of the two DPA configurations. Both designs offer excellent Doherty behavior (OBO range of 6 dB), but the proposed topology can deliver 3 dB more output power than the conventional structure due to the enhancement of PUF.

6.2 Circuit Design and Simulation

A broadband DPA (1.6-2.4 GHz), with targeted output power of 43 dBm and PUF=1, was designed based on the adoption of auxiliary transformer and optimum

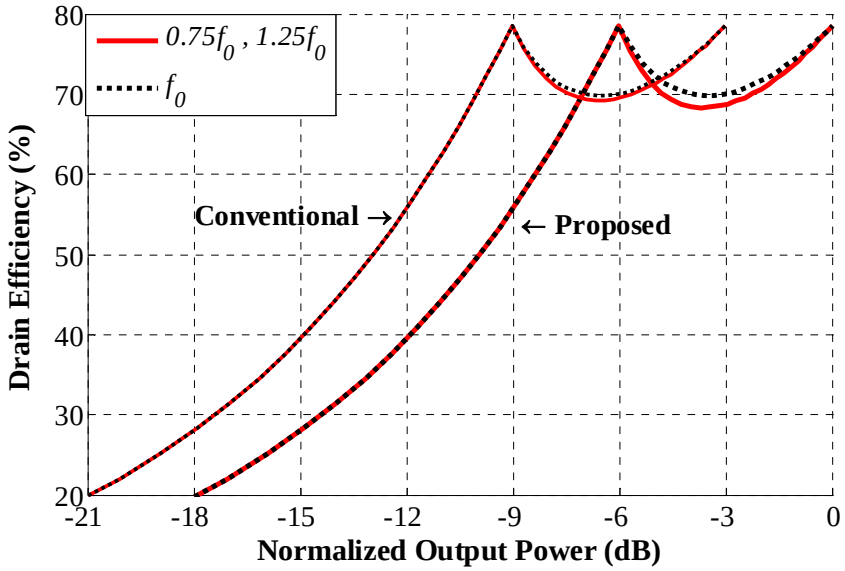


Fig. 6.9 Drain efficiency of the proposed and conventional designs

phase compensation. All simulations were performed using ADS with large signal model of Cree's GaN transistor CGH40006S.

6.2.1 Bias Selection and Optimum Drain Load Extraction

According to specifications [7], the breakdown voltage (drain-source) of CGH40006S is 120 V. Meanwhile, the drain voltage (peak value) of high efficiency amplifiers (e.g. Class C, J and F) is much larger than the dc bias voltage (2-3 times) [8]-[9]. For reliability consideration, the auxiliary drain bias is therefore selected to be 40 V. Furthermore, the adoption of AB-C Doherty configuration will lead to a slight reduction of PUF (by a few percent). It is also well known that, to attain ideal Doherty behavior with OBO of 6 dB, it is essential to have similar level of output power delivered from both the main and auxiliary devices. However, the lower output power capacity of the auxiliary device (class C) [10] causes insufficient load

modulation and results in degradation in efficiency and power performance [11]. This issue is prominent in broadband DPA design as the harmonic tuning of PA is usually more difficult to achieve over wide bandwidth. Subsequently, the drain bias of the main device is deliberately reduced to 35 V for having comparable output power (hence, the theoretical PUF is lowered by 6%).

The optimum drain load impedances (table 6.1) of the real devices (under the above bias condition) were extracted by using load-pull simulations. The optimum load impedances ($\mathbf{Z_{optcri}}$ and $\mathbf{Z_{optsat}}$) of the main device were determined at an output power level of 37.5 dBm (6 dB back-off) and 40.5 dBm (saturation). Meanwhile, the optimum load impedance ($\mathbf{Z_{optaux}}$) of the auxiliary device was obtained at output power of 40.5 dBm (saturation).

6.2.2 Design of Output Matching Network of Auxiliary Device

It is well known that the inclusion of the combining load network can offer additional design freedom to the implementation of OMN_M and OMN_A. Fig. 6.10(a) summarizes the design targets of OMN_A which include broadband impedance transformation from the combining load ($2R_L$) to the optimum drain load ($\mathbf{Z_{optaux}}$) as well as the provision of sufficiently high output impedance ($\mathbf{Z_{outA}}$) when the auxiliary device is off. Note that the 2:1 transformer (Fig. 6.2) is realized by the combined effect of OMN_A and device parasitic.

TABLE 6.1
Optimum Drain Loads of Main and Auxiliary Devices

Freq. (GHz)	Z_{optcri}	Z_{optsat}	Z_{optaux}
1.6	26.26+52.5j	24.88+37.64j	27.7+39.4j
1.8	24.1+50.4j	24.37+35.67j	25.6+36.6j
2	24.6+48.1j	25.56+31.81j	24.9+32.5j
2.1	24.7+47.3j	24.38+30.71j	24.4+31.3j
2.4	23.8+43.5j	24.38+27.94j	22.8+28.8j

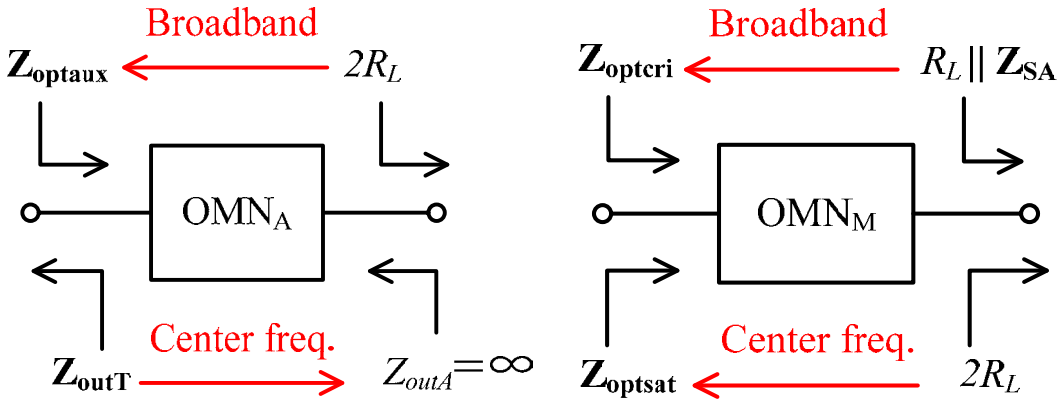


Fig. 6.10 Design Targets of output matching networks: (a) Auxiliary device ; (b) Main device

It is well understood that the output impedance of the auxiliary matching network in off-state is crucial in realizing broadband Doherty behavior. In theory, the output impedance of the matching network should approach infinity (open-circuit) when the auxiliary device is off, but in practice, the quasi-open-circuit requirement ($|\mathbf{\Gamma}_{\mathrm{outA}}| \approx 1, -45^\circ < \angle\mathbf{\Gamma}_{\mathrm{outA}} < -45^\circ$) is usually imposed [3]. Hence, apart from fulfilling the purpose of impedance matching, the auxiliary circuit should also exhibit minimal phase variation in output reflection coefficient [3]. Fig. 6.11 shows the prototypes under investigation which include one band-pass and two low-pass topologies. In meeting the design targets, they can be synthesized by the Simplified Real Frequency

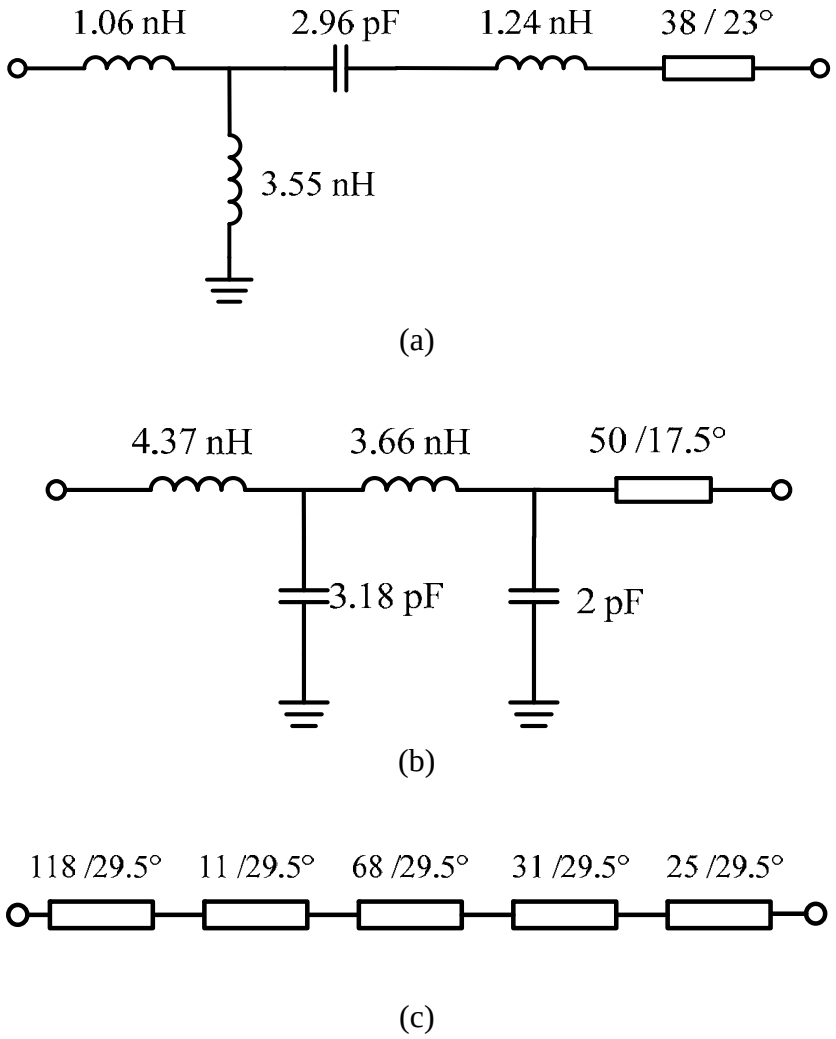
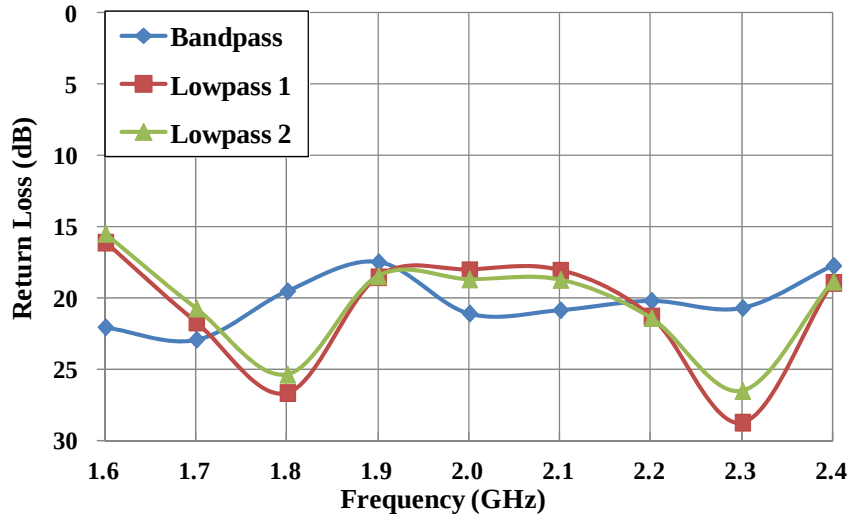
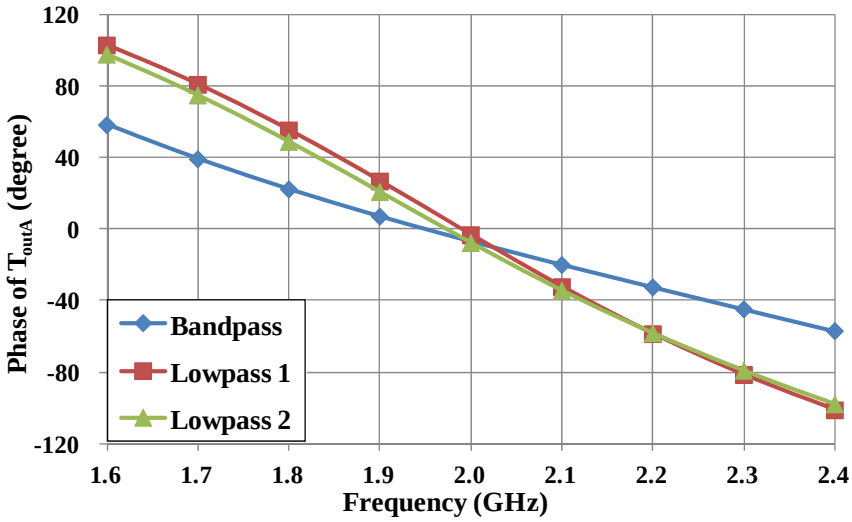


Fig. 6.11 Circuit topologies for auxiliary matching network: (a) Band-pass ; (b) Low-pass 1; (c) Low-pass 2 (line impedance in ohm)

Technique (SRFT) [12]-[13]. For comparison purposes, the frequency response of return loss and phase of $\mathbf{\Gamma_{outA}}$ (all prototypes) were simulated and depicted in Fig. 6.12. Among the three cases, only the band-pass design can offer good matching performance and small phase change. These results indicate that the phase variation of the band-pass design is almost halved with respect to the low-pass counterparts.



(a)



(b)

Fig. 6.12 Simulation results of different circuit topologies: (a) Return Loss; (b) Phase response

6.2.3 Output Matching of Main Device and Combining Network

Referring to Fig. 6.10(b), the major design target of OMN_M is to transform the load impedance from R_L//$\mathbf{Z_{SA}}$ to $\mathbf{Z_{optcri}}$ (auxiliary device is off), and from R_L to $\mathbf{Z_{optsat}}$ (auxiliary device is on). The combined effect of OMN_M and device parasitic should represent an impedance inverter (Fig. 6.3 (b)) with characteristic impedance of $2R_{opt}$ and phase shift of 90º (center frequency). Fig. 6.13 shows the simulation results of

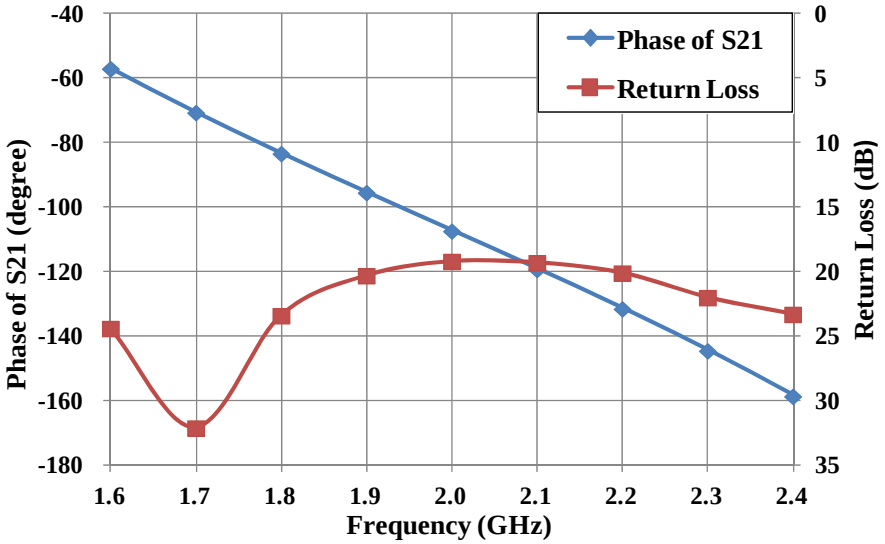


Fig. 6.13 Simulated Return Loss and phase response of OMN_M

return loss and the transmission phase of the synthesized matching network. Its group delay is much larger (× 3) than that of an ideal quarter-wavelength transmission line, which is considered to be the major cause of bandwidth reduction [5].

The Combining Output Matching Network (OMN_C) is employed to transform the external load (50 ohm) to the required combining load (19 ohm). As mentioned in section II, the drain voltage of the main device could exceed the safety level at large offset frequency from center, and waveform shaping [8]-[9] is often introduced to enhance efficiency and output power. A combining network based on low-pass topology can be designed to provide proper reactive loading (harmonic) as well as impedance matching (fundamental) [14].

6.2.4 Proposed DPA: Simulation Results

The optimum condition (phase difference of drain current sources) for enhanced output power and bandwidth has been analytically identified. However, the actual

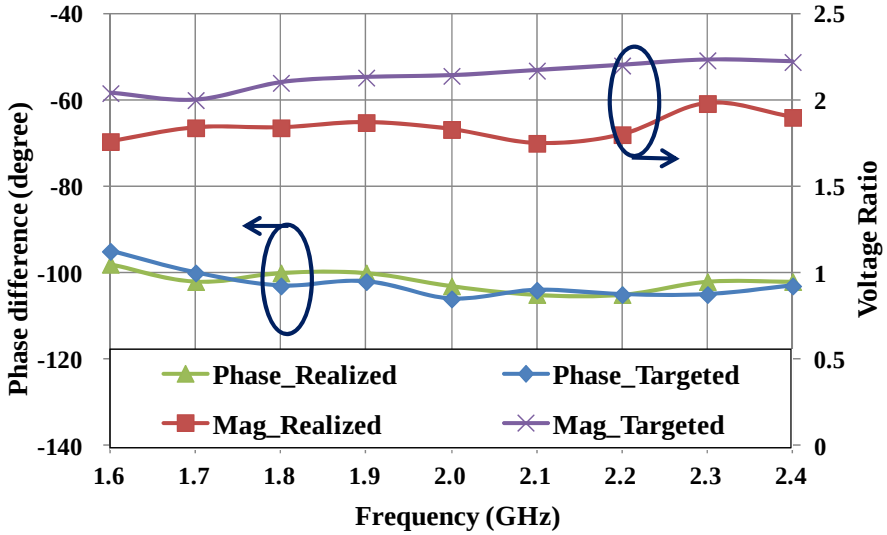


Fig. 6.14 Extracted and realized voltage ratio and phase difference by simulation

phase difference need to be re-extracted via nonlinear Harmonic Balance simulation since a real transistor behaves very differently from an ideal current source. As explained in Section 5.2.3, the gate voltage ratio (=$\mathbf{V_{gA}/V_{gM}}$) can be used to evaluate the ratio (magnitude and phase difference) between the main and auxiliary branch currents. Fig. 6.14 shows the extracted and realized results of gate voltage ratio, which were both found to be approximately 2 (magnitude of voltage ratio) and -105º (phase difference), over the frequency range from 1.6 to 2.4 GHz. Finally, based on the extracted source impedances and gate voltage ratio, the input matching networks were synthesized by using SRFT.

Fig. 6.15 shows the schematic diagram of the final design. A Wilkinson power divider was employed to split the input signal into two equal parts. Both low-pass (input matching, output matching of main device, combining network) and band-pass (output matching of auxiliary device) networks were involved with line impedance ranging from 24 – 96 ohm. For stability control, RC circuits were inserted in series

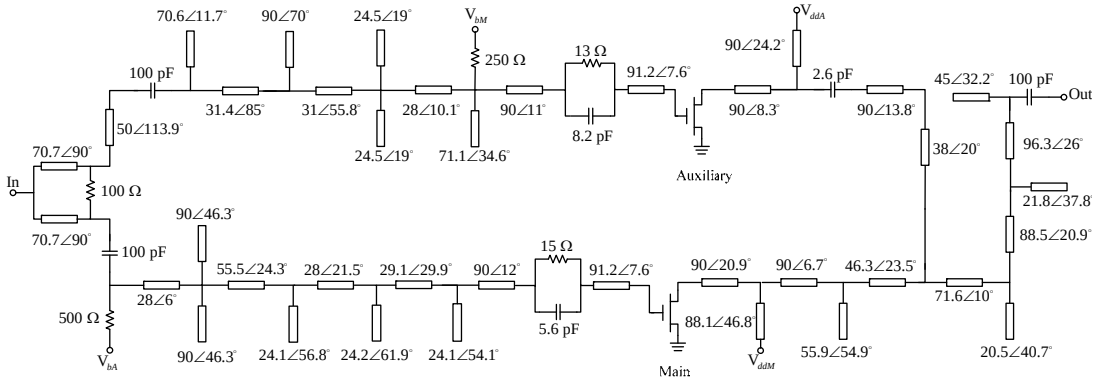
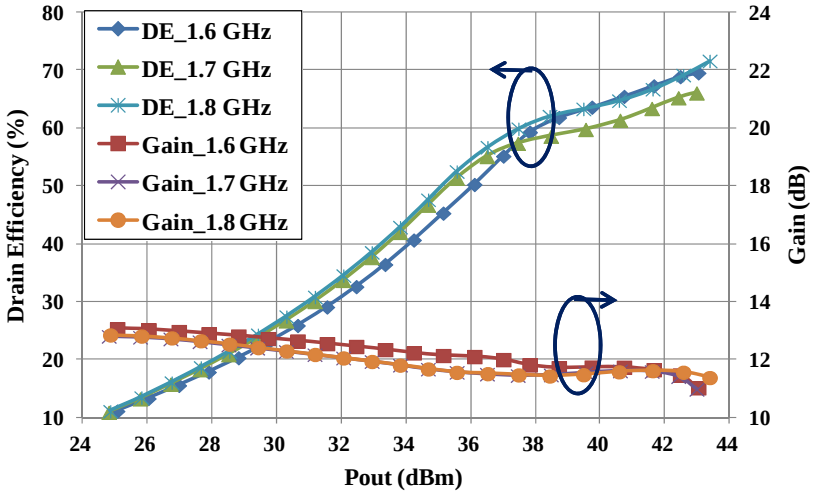


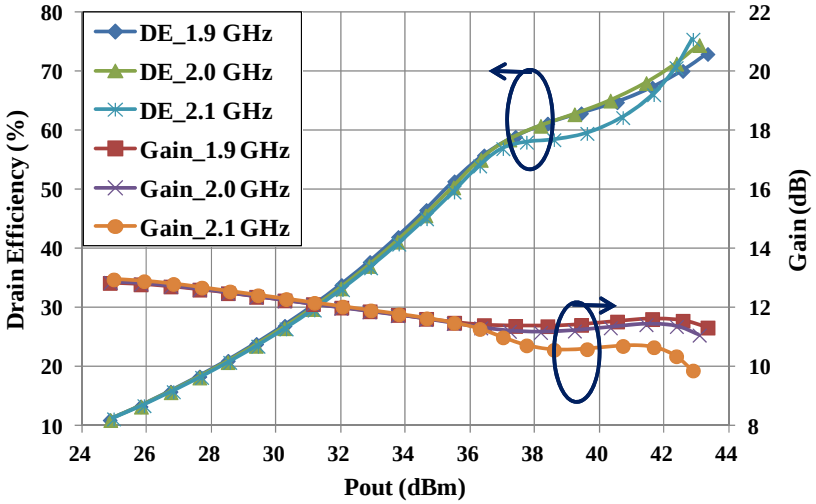
Fig. 6.15 Schematic diagram of the proposed DPA (line impedance in ohm)

connection with the gate inputs of the active devices. To take into account the effect of junction discontinuities and device nonlinearity, co-simulation based upon large signal model was conducted. Some fine-tuning of the layout was made to further optimize the efficiency and power performance. To minimize the gain variation in (low power and Doherty regions), the gate bias of the main device (deep Class AB) was slightly modified to give a quiescent drain current of 35 mA while the gate bias of the auxiliary devices (Class C) was adjusted to –6.7 V.

Fig. 6.16 shows the simulated drain efficiency and gain performance as a function of output power. Over the frequency range from 1.6 to 2.3 GHz, the saturation output power was found to be close to 43 dBm with the power gain of about 12 dB. Typical Doherty behavior can be observed with a 6 dB back-off efficiency of 55-64% and saturation efficiency of 68-76%.



(a)



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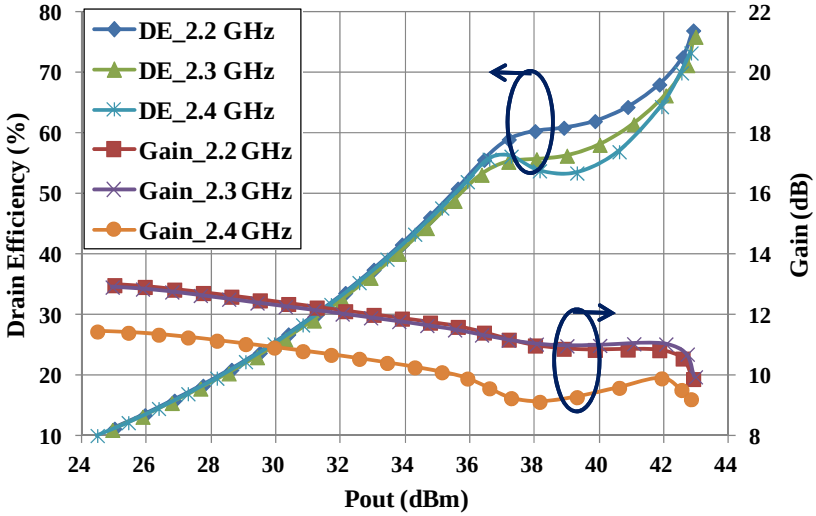


(c)

Fig. 6.16 Simulated drain efficiency and gain performance of the proposed DPA: (a) 1.6-1.8 GHz; (b) 1.9-2.1 GHz; (c) 2.2-2.4 GHz

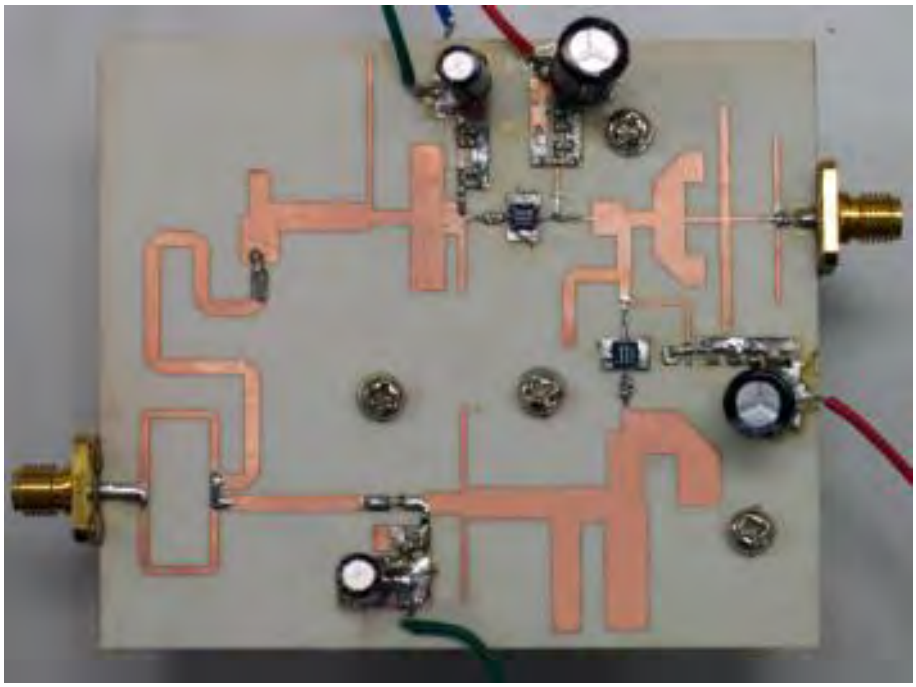


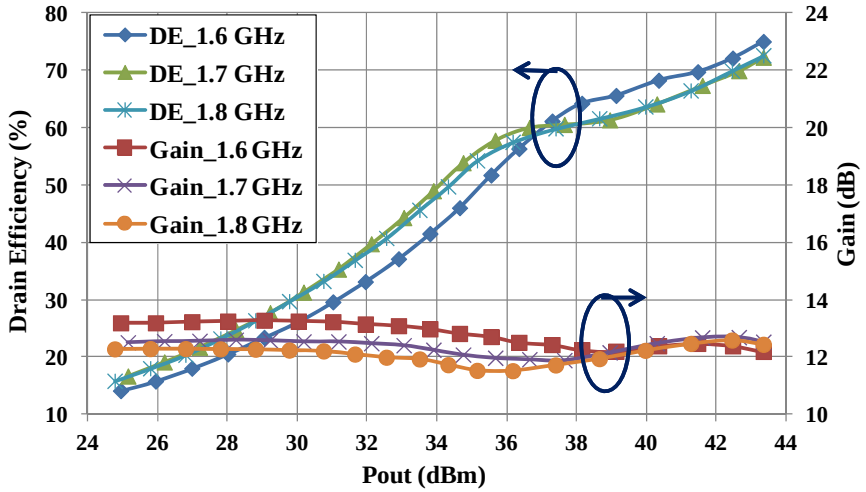
Fig. 6.17 Photograph of the fabricated DPA

6.3 Experimental Verification

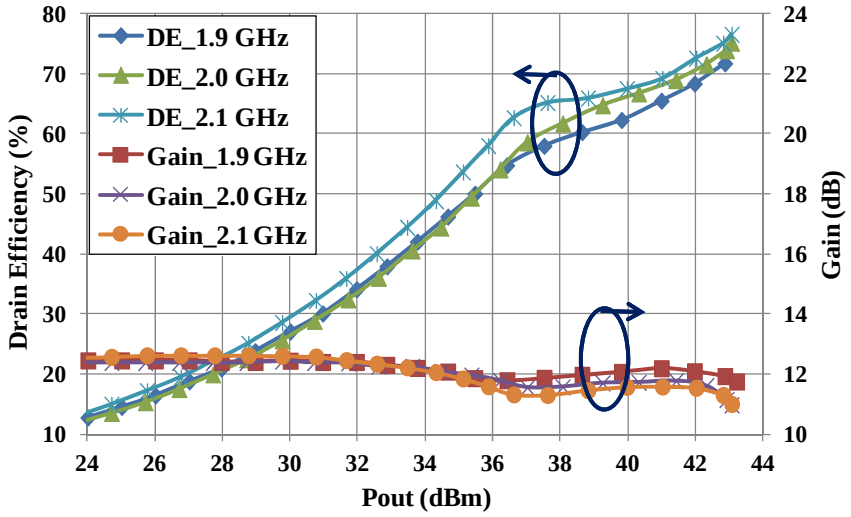
For experimental validation, the proposed DPA was fabricated on microwave substrate (RO4003C) with thickness of 0.813mm and dielectric constant of 3.55. The top view of the prototype is shown in Fig. 6.17.

6.3.1 CW Signal Measurement

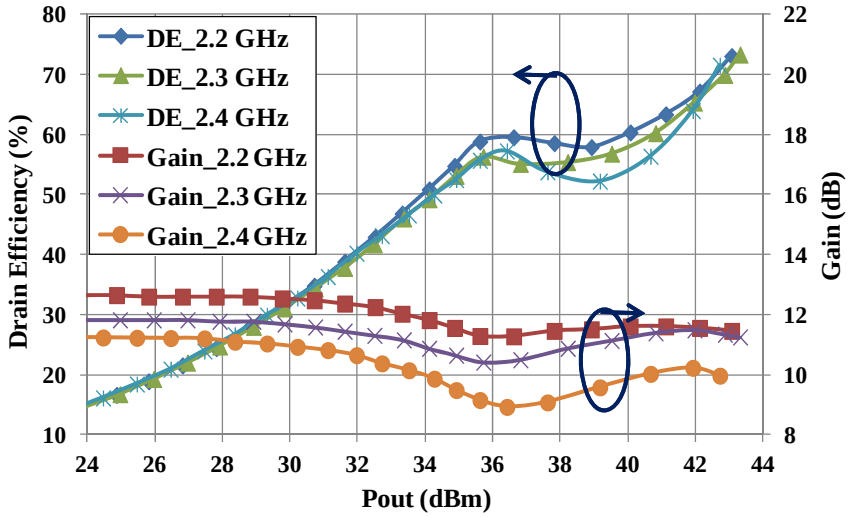
Fig. 6.18 gives the measured gain performance and drain efficiency of the proposed DPA as a function of output power under CW signal stimulation (with frequency ranged from 1.6 to 2.4 GHz in step of 0.1 GHz). Inside the low power region, excellent gain flatness (11.5 – 13 dB) can be observed. Meanwhile, good Doherty efficiency behavior was found from 1.6 to 2.3 GHz with a gain compression of less than 1.5 dB. With reference to Fig. 6.19, the measured drain efficiencies at



(a)



(b)



(c)

Fig. 6.18 Measured drain efficiency and gain performance of the proposed DPA: (a) 1.6-1.8 GHz; (b) 1.9-2.1 GHz; (c) 2.2-2.4 GHz

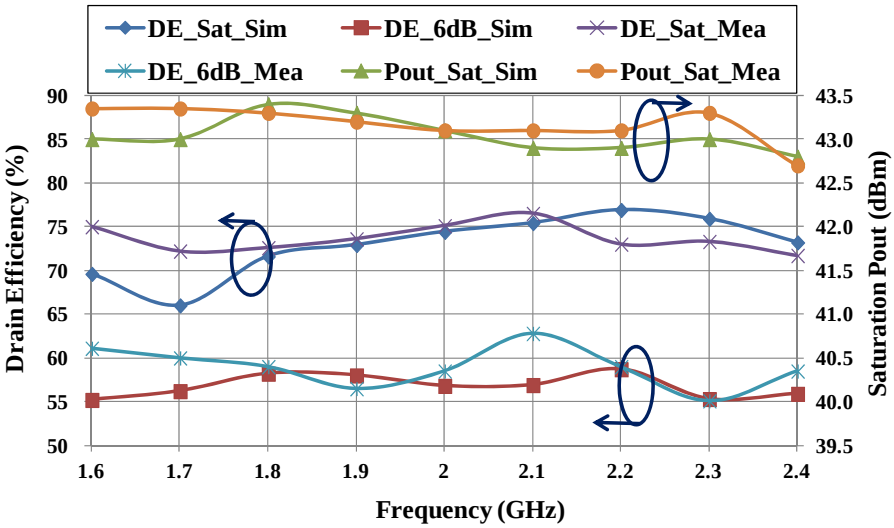


Fig. 6.19 Measured and Simulated drain efficiency (at saturation level and 6 dB back-off) and saturation output power

saturation (around 43 dBm) and 6 dB power back-off (around 37 dBm) were over 71% and 55%, respectively, for the entire frequency band. Small variation in saturation output power and drain efficiency with frequency was clearly observed.

6.3.2 Modulated Signal Measurement

To access the efficiency and linearity performance of the proposed DPA under modulated signal stimulation, measurements based upon single-carrier WCDMA signal with PAPR of 6.6 dB at 0.1% probability of complementary cumulative distribution function (CCDF) were employed. Fig. 6.20 shows the measured drain efficiency and ACLR (with 5 MHz offset) at an average output power of 37 dBm. The ACLR performance was better than –32 dBc from 1.6 to 2.2 GHz. Nevertheless, excellent average drain efficiency (53-58%) can be obtained over the entire band. Fig. 6.21 shows the output spectrum of the proposed DPA with WCDMA stimulation centered at 2 GHz, which indicates an ACLR level of -37 dBc.

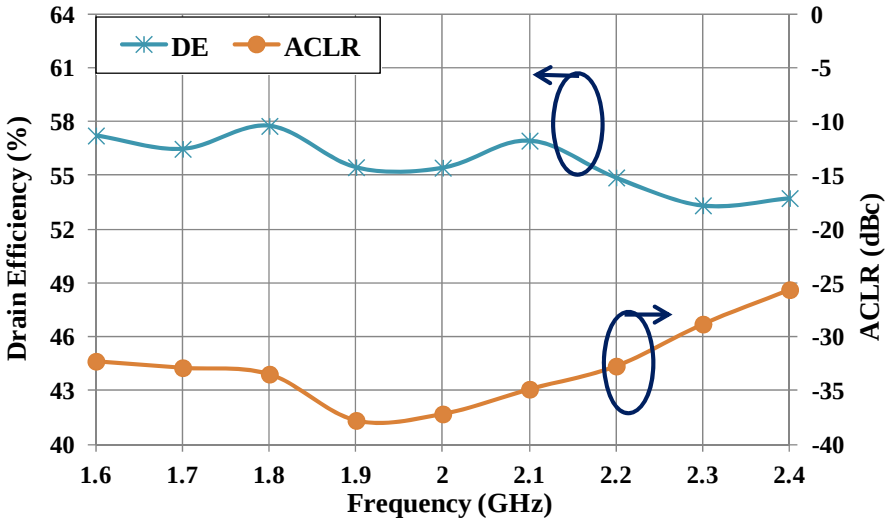


Fig. 6.20 Measured average drain efficiency and ACLR (WCDMA test signal at an average output power of 37 dBm)

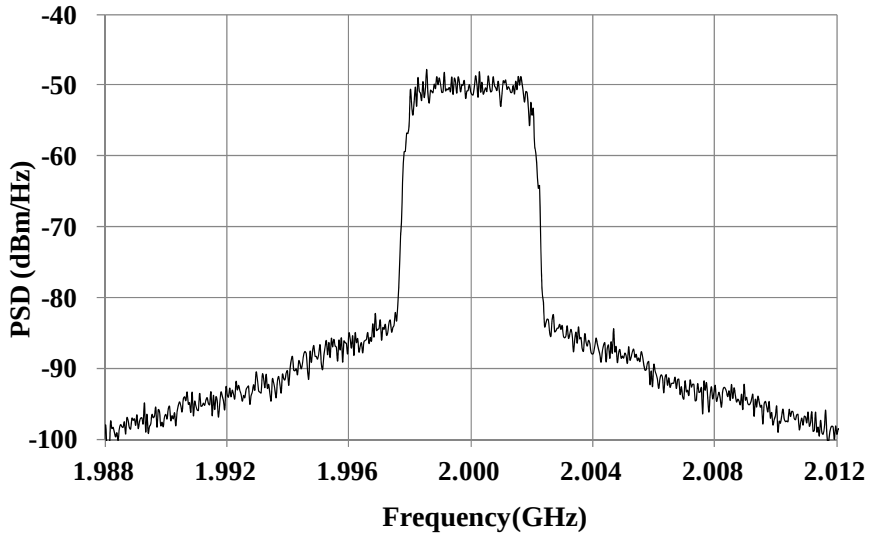


Fig. 6.21 Measured output spectrum of proposed design (WCDMA test signal at 2 GHz with an average output power of 37 dBm)

Table 6.2 shows the summary of this work and some recent reports on broadband DPA designs with the same device technology. As some of the auxiliary transistors involved were operating under high efficiency classes (e.g. J and F) with uncertain peak voltage levels, and therefore, in the calculation of PUF, the drain bias of the device has been adopted as the maximum voltage rating (rather than one-half of the break-down voltage).

Table 6.2
Comparison of Some Recent Broadband DPA Designs Based on GaN Technology

Ref.	Freq. (GHz)	FBW	DPA Configuration	PUF	OBO (dB)	Sat. Pout (dBm)	DE at Sat. (%)	DE at 6 dB OBO (%)
[4]	1.7-2.6	42%	Classical with Low-pass OMN_A	1	5-6	42.1-45.3	50-55	41-55
[5]	2.2-3.0	31%	Classical with Low-pass OMN_A	1	5-6	39.4-41.8	55-69	29-53
[6]	1.05-2.55	83%	Modified with Low-pass OMN_A	1	5-6	40-42	45-83	35-58
[7]	0.7-1.0	35%	Modified w/o OMN_A	0.51	6	49-50.8	61-75	52-64
[8]	1.5-2.4	46%	Modified w/o OMN_A	0.54	6	~ 42	52-68	50-62
This Work	1.6-2.4	40%	Modified with Band-pass Auxiliary Transformer	0.94	6-7	42.7-43.3	72-77	55-63

In compared to conventional approaches [4]-[5], it is clear that PUF can be greatly enhanced (from 0.5 to 0.94) with the introduction of auxiliary transformer. Besides, the best 6 dB back-off and saturation efficiencies (around 59% and 75%, respectively) have been achieved, which reveals that the proposed method can offer excellent efficiency-bandwidth performance. Especially when compared to [5], the proposed design is solely based on analog circuitry and no sophisticated digital control is involved. It is also worth mentioning that this work deliberately selects unequal drain bias for the main and auxiliary amplifiers to improve OBO (6-7 dB) and output power variation with frequency (43±0.3 dBm) at the expense of PUF (= 0.94).

6.4 Conclusion

A new broadband DPA configuration using band-pass auxiliary transformer to improve PUF has been presented. The broadband performance of the proposed and conventional topologies has been analytically investigated and compared. Issues relating to the design of auxiliary transformer and optimum control of phase difference have also been addressed. Prototype of the proposed DPA has been designed, built and characterized with CW and WCDMA signal formats. These results indicate that the proposed design is capable of providing high PUF and state-of-the-art efficiency-bandwidth performance.

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Chapter 7
Conclusions and Future Works

7.1 Conclusions

The growing demand for high data-rate transmission with mobile devices leads to the deployment of spectrum-efficient modulation techniques and multi-carrier access technology, which generate signals with ever-increasing value of PAPR and operating bandwidth.

The proper handling of these signals calls for advanced design of RF power amplifiers. In this thesis, three new design approaches of DPA have been presented. Prototypes based on the GaN technology has been designed, fabricated and characterized with different test signal formats for validation purposes. The major contributions of this work include:

1. By the introduction of complex combining load, high efficiency region of DPA can be largely extended without the need of multi-cell or asymmetrical implementation. In other words, the complex combining load is adopted as a new degree of freedom to enhance the span of the dynamic load modulation, and thus, the range of OBO;

2. The major drawback of the fixed complex combining load method is the narrow available bandwidth. To achieve extended OBO range and extended bandwidth, a new DPA design based upon frequency-varying complex combining load and

optimal input current control has been proposed. Fractional bandwidth of over 20% has been demonstrated by the proper selection of frequency-varying complex load space, with OBO of 8.5 dB and excellent output power performance.

3. To achieve optimal PUF and broadband operation, a new DPA configuration based upon band-pass auxiliary transformer has been presented. The broadband performance of the proposed and conventional topologies has been analytically investigated and compared. Issues relating to the design of auxiliary transformer and optimum control of phase difference have also been addressed.

7.2 Recommendation for Future Research

Inspired by this work, some future research topics related to DPA design are summarized below:

1. In Chapter 5, it has been demonstrated, for a given set of combining loads, both OBO extension and broadband performance can be achieved with the help of optimal input current control. However, the different choice of frequency-varying CCL may lead to further enhancement of DPA performance. Therefore, future investigation can be carried out to identify the optimal choice of frequency-varying CCL for best efficiency-bandwidth-PUF performance.

2. It is well known that, suitable harmonic tuning is necessary for wideband and high efficiency operation. However, at saturation, the harmonic load impedances (main device) are heavily affected by the harmonic current of the auxiliary device.

Therefore, the conventional harmonic tuning method (originally developed for PA design with fixed load) is no longer applicable to DPA design. Hence, new implementation concept of wave-shaping involving dynamic load modulation over broadband operation is required to be developed in future for optimized efficiency and power performance of DPA.

List of Publications

[1] X. Fang, K. M. Cheng, "Extension of high-efficiency range of Doherty amplifier by using complex combining load," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 9, pp. 2038–2047, Sep. 2014.

[2] X. Fang, K. M. Cheng, "Broadband, wide efficiency range, Doherty amplifier design using frequency-varying complex combining load" to be presented *in IEEE MTT-S 2015 Int. Microw. Symp. Dig*., USA, May, 2015.

[3] X. Fang, K. M. Cheng, "Improving power utilization factor of broadband Doherty amplifier by using band-pass auxiliary transformer," submitted to *IEEE Trans. Microw. Theory Techn.*, 2015.