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Transistor Ring Oscillators and Material Assessment

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John F. Wager

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) constitute the central theme of this thesis. Within this theme, three primary areas of focus are pursued.

The first focus is the realization of a transparent three-stage ring oscillator with buffered output and an output frequency in the megahertz range. This leads to the possibility of transparent radio frequency applications, such as transparent RFID tags. At the time of its fabrication, this ring oscillator was the fastest oxide electronics ring oscillator reported, with an output frequency of 2.16 MHz, and a time delay per stage of 77 ns.

The second focus is to ascertain whether a three-terminal device (i.e., a TFT) is an appropriate structure for conducting space-charge-limited-current (SCLC) measurements. It is found that it is not appropriate to use a diode-tied or gate-biased TFT configuration for conducting a SCLC assessment since square-law theory shows that transistor action alone gives rise to $I \propto V^2$ characteristics, which can easily be mistakenly attributed to a SCLC mechanism. Instead, a floating gate TFT configuration is recommended for accomplishing SCLC assessment of AOS channel layers.

The final focus of this work is to describe an assessment procedure appropriate for determining if a dielectric is suitable for use as a TFT gate insulator. This is accomplished by examining the shape of a MIM capacitor's $log(J)$-ξ curve, where J is the measured current density and ξ is the applied electric field. An appropriate dielectric for use as a TFT gate insulator will have a $log(J)$-ξ curve that expresses a clear breakover knee, indicating a high-field conduction mechanism dominated by Fowler-Nordheim tunneling. Such a dielectric produces a TFT with a minimal gate leakage which does not track with the drain current in a $log(I_D)$-V_{GS} transfer curve. An inappropriate dielectric for use as a TFT gate insulator will have a $log(J)$-ξ curve that does not express a clear breakover knee, indicating that the dominate conduction mechanism is defect driven (i.e., pin-hole like shunt paths) and, therefore, the dielectric is leaky. It is shown that experimental $log(J)$-ξ leakage curves can be accurately simulated using Ohmic, space-charge-limited current (SCLC), and Fowler-Nordheim tunneling conduction mechanisms.

Amorphous Oxide Semiconductor Thin-Film Transistor Ring Oscillators and Material Assessment

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I understand that my thesis will become part of the permanent collection of Oregon State University libraries. My signature below authorizes release of my thesis to any reader upon request.

Eric Steven Sundholm, Author

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"When the dust settles... and a miracle occurs."

John F. Wager

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1. INTRODUCTION

Next generation integrated circuits are likely to employ bold new approaches, as required to achieve their electrical requirements. One aspect of such new technology could tie directly into substrate choice. Imagine, for example, what could be accomplished if the usual expensive, rigid, brittle, flat, and opaque substrate were replaced by a curved, durable, flexible, and transparent substrate.

Manufacturing such circuits would likely involve the use of thin-film transistors (TFTs). TFTs are often characterized according to the active channel layer utilized. Possibilities include amorphous silicon (a-Si), poly-crystalline silicon (poly-Si), silicon-on-insulator (SOI), organic, poly-crystalline oxide, and amorphous oxide semiconductor (AOS) TFTs.

The use of AOS TFT technology for the realization of transparent circuits is the main focus of this thesis. This realization of transparent electronics is promised on the use of transparent thin-film transistors (TTFTs). In addition to TTFTs, other AOS devices such as capacitors and resistors can be produced which are also transparent. Partially transparent or non-transparent AOS devices are equally well suited to a broader category of oxide electronic application due to inherent materials, devices, circuits, and manufacturing applications of this technology.

The commercial promise of transparent AOS devices is compelling. Creative applications such as windows that serve as televisions, bathroom mirrors with interactive makeup and hair preparation assistance utilities, and automatically dimming windows are feasible possibilities. In addition to such futuristic applications, transparent circuits exist today. Approximately thirty percent of the power in a standard

TFT liquid crystal display is dissipated by the backlight [1]. Of the generated light that reaches the opaque pixel driver circuitry, only fifty percent is transmitted [2]. If these circuits were transparent, the display would consume less power by lowering the backlight intensity while maintaining performance. Lower display power consumption would enhance portability and battery requirements.

This thesis is organized as follows. Chapter 2 provides background information including an overview of TFT operation and of previous work related to transparent circuits and discrete devices for comparison to the work presented in this thesis. Chapter 3 consists of a discussion of thin-film processing methods used for the fabrication of transparent circuits, device characterization methods, and design and simulation considerations. Chapter 4 describes AOS circuit realization and design. Chapter 5 is a discussion of space-charge-limited-current measurements of thin-film transistors. Chapter 6 is a discussion of dielectric assessment in terms of leakage characteristics. Chapter 7 consists of a summary of the conclusions drawn from the experiments performed for this thesis and recommendations for future work.

2. LITERATURE REVIEW AND TECHNICAL BACKGROUND

This chapter explores previous reported work as it relates to transparent circuits and provides information on fundamental concepts regarding TFTs, TTFTs, and circuits used within this work.

2.1 Thin-Film Transistors

TFTs constitute a class of field-effect transistors in which the active channel layer, gate insulator, and metal contacts (gate, source, and drain) are deposited as thin-film layers. TFTs have been in development since their invention in 1930 [3, 4, 5, 6], while the the use transparent conducting oxide (TCO) like materials for a channel has been used since 1964 [7]. Transparent transistor versions, TTFTs, have been in development since 1996, initially in the context of a ferroelectric transistor [8]. This ferroelectric device differs greatly from the devices discussed herein in that ferroelectric transistor channel layers are purposely doped to high to very high electron concentrations ($> 10^{18}$ cm^{-3}), whereas the channel layers of TFTs and TTFTs in this work are engineered to have a low carrier concentration ($\sim 10^{16}$ cm^{-3}) [9]. Inorganic amorphous oxide semiconductor (AOS) channel materials are often used in these TFTs with low channel layer carrier concentrations. AOSs were originally proposed for TCO applications. The first TTFTs were fabricated using zinc oxide, which is a polycrystalline material. These ZnO TTFTs were created almost simultaneously (i.e., within a few months of each other) by three different research groups in 2003 - Oregon State University [10], Minolta Co. [11], and DuPont Research and Development [12]. The following subsections are focused on TFT structure, operation, and metrics.

2.1.1 TFT Device Structures

There are four basic types of TFT structures, as shown in Fig. 2.1; staggered top-gate, co-planar top-gate, staggered bottom-gate, and co-planar bottom-

gate. Staggered structures are so named because the source/drain contacts are placed on the opposite side of the channel-insulator interface than the gate contact. Coplanar structures are so named because the source/drain and gate contacts are placed on the same side of the channel-insulator interface. Each of these four structures has specific advantages and disadvantages [13]. The staggered bottom-gate structure is exclusively employed in this work.

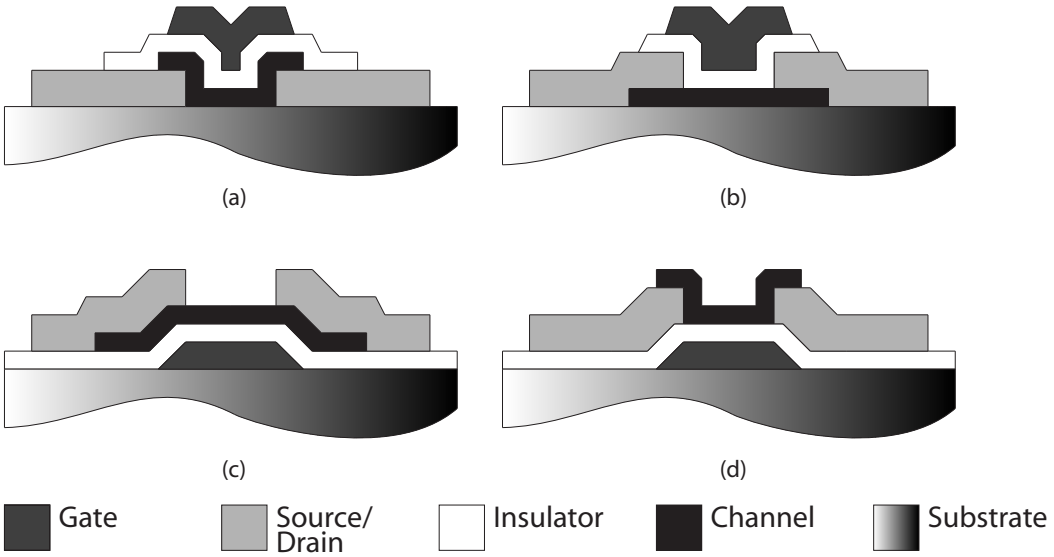

Figure 2.1: Four basic TFT structures: (a) staggered top-gate, (b) co-planar top-gate, (c) staggered bottom-gate, and (d) co-planar bottom-gate.

2.1.2 TFT Device Operation

Figure 2.2 illustrates energy band diagrams for an n-type accumulation-mode TFT under various gate bias conditions. Under ideal conditions, when no gate bias is applied, the bands are assumed to be at flat-band, as shown in Fig. 2.2(a). When a negative gate bias is applied, delocalized electrons in the channel are repelled from the channel-insulator interface. This creates a region of positive charge referred to as

a depletion region (i.e., depleted of carriers, or electrons since this material is n-type). Positive charge creates a positive (upward) bending of the conduction and valance bands, as shown in Fig. 2.2(b). When a positive gate bias is applied, delocalized electrons in the channel are attracted to the channel-insulator interface. This creates a region of negative charge referred to as a accumulation region (i.e., accumulation of carriers, or electrons since this material is n-type). The region of negative charge creates a negative (downward) bending of the conduction and valance bands, as shown in Fig. 2.2(c).

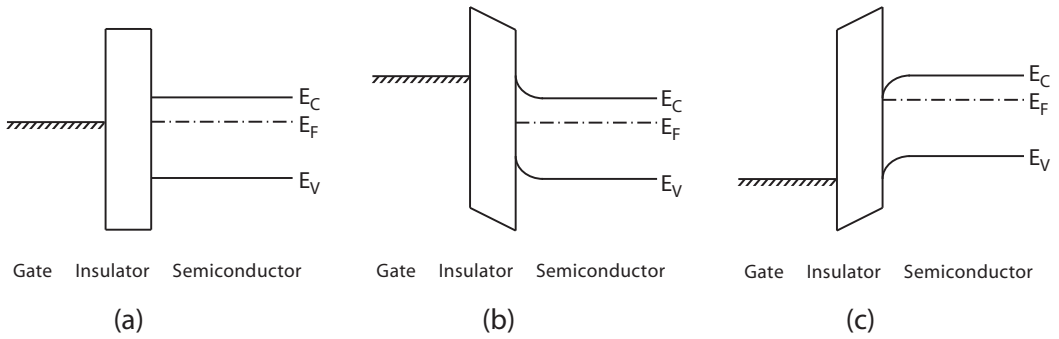

Figure 2.2: Energy band diagrams of a n-type accumulation-mode TFT. (a) Under ideal conditions and no applied gate bias a condition of flat-band occurs at $V_G = 0$ V. (b) Depletion of carriers resulting in upward band bending with negative gate bias, $V_G < 0$ V. (c) Accumulation of carriers resulting in downward band bending with positive gate bias, $V_G > 0$ V.

TFTs may be classified as enhancement-mode, requiring a positive gate-to-source (V_{GS}) bias to accumulate a channel and turn the device on, or depletion-mode, requiring a negative V_{GS} bias to deplete the channel and turn the device off. The required V_{GS} to turn the device on/off is known as the turn-on voltage, V_{ON}, and is controlled by the balance between free carriers and traps (i.e., electric defects which can hold or release carriers), and can be expressed by the discrete donor trap model

[9],

$$V_{ON} = \frac{-q}{C_{INS}}(n_{co} - p_{to}), \tag{2.1}$$

where n_{co} is the equilibrium carrier concentration, p_{to} is the equilibrium empty trap concentration, q is the electronic charge, and C_{INS} is the gate capacitance density. Carrier generation in AOS is believed to be the result of oxygen vacancies within the amorphous network [14]. Trap generation in AOS can be attributed to defects in the channel material, and can be either bulk or surface/interface defects.

In addition, TFTs can operate in three regions: cut-off with no drain current (I_D) flow, pre-saturation in which I_D monotonically increases with increasing drain-to-source voltage (V_{DS}), and saturation where I_D is ideally independent of V_{DS}.

A more detailed description of TFT operation in terms of enhancement- depletion-mode, turn-on voltage, threshold voltage, and regions of operation (including appropriate current modeling equations) can be found in Section 5.3.

2.2 Transparent Conducting Oxides

TCO's are a class of materials which exhibit both high electrical conductivity and optical transparency. Due to the band gap required for optical transparency, it is usually considered that electrical conductivity and transparency are two properties which are mutually exclusive [15]. To achieve this combination, the material must have a band gap $>\sim$3.1 eV, a carrier concentration of $>\sim 10^{19}$ cm^{-3}, and a mobility $>\sim$1 cm^{2}V^{-1}s^{-1} [9].

Table 2.1 is a summary of basic electrical properties of the three classic TCOs, indium oxide, zinc oxide, and tin oxide [9]. Arguably the best TCO listed in Table 2.1 is indium oxide with the largest band gap, highest conductivity, and greatest mobility. However, indium is quite rare and extremely expensive. Today, some countries have started recycling programs to reclaim precious indium from discarded consumer products [16]. The most common TCO used today is indium tin oxide (ITO). ITO is

Table 2.1: Electrical properties of common transparent conducting oxides (TCOs). Conductivites reported are for best-case polycrystalline films.

Material	**Bandgap** (eV)	**Conductivity** (S cm^{-1})	**Electron concentration** (cm^{-3})	**Mobility** (cm^2V^{-1})
In_2O_3	3.75	10,000	$> 10^{21}$	35
ZnO	3.35	8,000	$> 10^{21}$	20
SnO_2	3.6	5,000	$> 10^{20}$	15

primarily indium oxide mixed with a small amount of tin oxide (i.e., 10:1 In_2O_3:SnO ratio). While considered a conductor, the resistivity of ITO is rather high, having a resistance of $R_S = 70 - 100\ \Omega$ for the ∼15-30 nm thick films used for circuit fabrication in this work [17]. This correlates to approximately an order of magnitude lower conductivity than common metals used in circuit fabrication like tungsten, aluminum, and copper [9].

TCOs can be credited as contributing to two important aspects of a TTFT. First, as previously mentioned, the AOS materials family was originally proposed for TCO applications. Second, TCOs are used in TTFTs for source, drain, and gate contacts, as well as for interconnects. Due to the wide band gaps of suitable TTFT gate insulators, this leaves only the substrate to consider in terms of transparency.

2.3 Transparent Amorphous Oxide Semiconductors

This section provides a brief overview of AOS and highlights the most important information as it is related to this work [9].

Seven years before the first report of a TTFT, Hosono et al. pointed out the advantages of using AOS for TCOs [18, 19]. The amorphous nature of AOS makes them attractive for manufacturing because of their low temperature processability, surface smoothness, and lack of grain boundaries. This makes AOS an appropriate choice for large-area, low-cost, transparent, and possibly flexible electronics applications. As Fig. 2.3 illustrates, AOS conduction band minima are derived from large

overlapping s-orbitals. The amount of atomic orbital overlap is directly related to

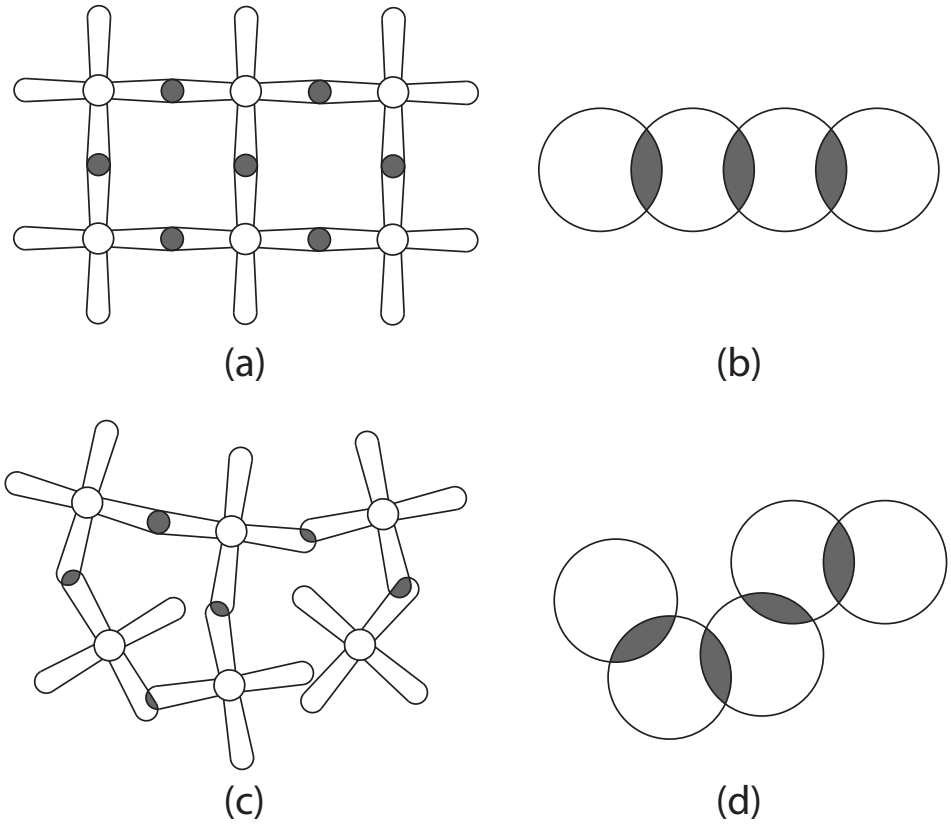

Figure 2.3: Atomic orbital overlap (shaded) for (a) crystalline covalent semiconductors, (b) crystalline oxide semiconductors with large, spherically-symmetrical orbital radii, (c) amorphous covalent semiconductors, and (d) amorphous oxide semiconductors.

the carrier mobility within the material. The large s-orbitals, being spherical and not requiring orientation to overlap, allow their amorphous structures to have carrier mobilities of similar magnitudes as their polycrystalline counterparts. This is in contrast to classic semiconductors (e.g., crystalline silicon) with covalent bonding and sp-hybrid orbitals with precise orientation between bonds, as occurs with a crystalline or poly-crystalline microstructure. This precise bond orientation is required in order

to obtain a sufficient degree of orbital overlap, leading to a high mobility. Also, note that while the overlap between the crystalline and amorphous oxide semiconductors in Fig. 2.3(b) and Fig. 2.3(d), respectively, is nearly identical, the "path" which a carrier might take is less direct in the amorphous semiconductor. This increase in path length gives rise to the slight decrease in mobility which can be observed between crystalline, polycrystalline, and amorphous oxide semiconductors.

The use of metal oxides (as opposed to sulfides, nitrides, etc...) offers a naturally thermodynamically stable material. Since oxygen reacts readily with a metal, and nitrogen does not, AOS are capable of being processed (e.g., annealed, stored, or tested) in air [9].

Focusing on these constraints, i.e., metal *oxides* with large s-orbitals in an amorphous structure, narrows the choice of possible constituent cations to a small section of the periodic chart, as shown in Fig. 2.4[19]. Further reduction of these choices can be made when cost, toxicity, and abundance is considered.

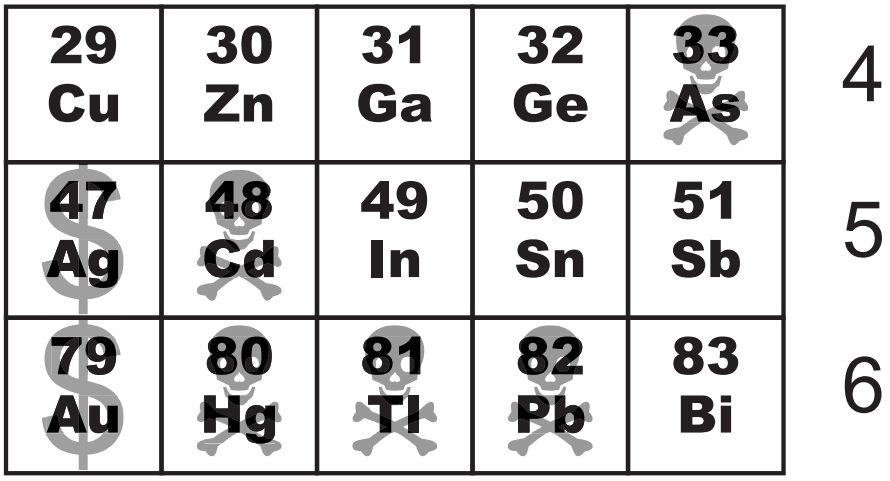

Figure 2.4: Section of the periodic table appropriate for selecting AOS materials showing those excluded for cost (ghosted dollar sign) and those excluded for toxicity (ghosted skull/crossed bones). Additionally, indium and gallium are costly.

An AOS is obtained by selecting multi-component combinations of oxides from the portion of the periodic table shown in Fib. 2.4. The use of multi-component oxides allows an amorphous microstructure to be realized as a consequence of crystal frustration.

After the year 2003, when transparent electronics made its entrance [10, 11, 12], AOS research divided into two main camps; those using indium and gallium for performance reasons, and those avoiding indium and gallium due to cost. While indium and gallium are both expensive, these elements offer electrical performance advantages. It is believed that indium provides higher electron mobility, while gallium tends to suppress electron carrier concentration allowing TFTs to have gate-bias controlled channel modulation. Indium gallium zinc oxide, IGZO, and indium gallium oxide, IGO, are the two most commonly used AOSs [14, 20].

The use of multiple metals in an AOS offers a unique methodology for controlling the properties of the AOS. Contrary to conventional manufacturing wisdom in which compositional simplicity is always preferred, AOS engineering via the use of multi-component ternary, quaternary, or more complicated alloys offers electrical performance advantages which may outweigh disadvantages inherent in the use of more compositionally complex materials.

Three main AOS semiconductors are used in this work, i.e., 1:1 indium gallium oxide (IGO; 1:1 In_2O_3 to Ga_2O_3), 2:1 zinc tin oxide (ZTO; 2:1 ZnO to SnO_2), and 2:1 zinc indium oxide (ZIO; 2:1 ZnO to In_2O_3).

2.4 n-Type Only Transistor Circuits

Presently, AOS circuits are limited to the use of n-type only TFTs. The lack of p-type TFTs forces the circuit designer to use NMOS-like designs rather than CMOS-like architectures, in which both n- and p-type transistors are available. CMOS designs are preferable and offer many advantages, such as lower power consumption,

"rail to rail" operation, and smaller circuit area. However, complicated and sophisticated NMOS circuits can be realized.

In 1978, Tsividis published a paper on design considerations in single-channel MOS analog integrated circuits [21]. The paper steps through calculations and procedures for designing critical analog circuits such as biasing circuits (e.g., voltage dividers and current sources), split-load inverters, cascode stages, source followers, differential pairs, differential to single-ended converters, and output stages. This circuit list, plus small-signal calculations included, makes this paper an extremely valuable guide for any complex analog n-type only circuit.

In 1979 Young published a high-performance all-enhancement NMOS operational amplifier (op-amp) design [22]. Op-amps are needed for the realization of more complex and functional systems such as A-D and D-A converters, CODEC's (compression and decompression), and switched-capacitor filters. All of these systems are as important today as in 1979, and therefore older publications focusing on n-type only circuits are quite useful in aiding in the design of AOS-based circuits.

A major improvement to any single-channel (i.e., n-type only) circuit is the use of a depletion-mode transistor for the load [23]. Unfortunately this adds processing complexity as two different channel behaviors must be produced (i.e., enhancement- and depletion-mode). The advantage of this design is, unlike enhancement-mode transistor loads, depletion-mode loads allow the output of the circuit to climb all the way to the high supply rail (i.e., an inverter output can reach V_{DD}, the high supply rail) and have exceptionally large DC gain [23]. Depletion-mode load transistor circuit design is used within this work for digital inverters, NAND gates, NOR gates, and latches.

2.4.1 Enhancement-Mode Load Inverter

Figure 2.5 is an example of enhancement-mode load architecture, showing an inverter utilizing an enhancement-mode load transistor and an enhancement-mode

driver transistor. This architecture is the simplest, because it requires only one type of TFT (i.e., enhancement-mode, n-type). With the gate terminal of the enhancement-

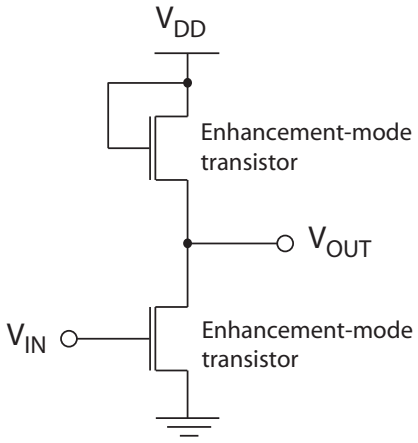

Figure 2.5: Schematic of an n-type only inverter utilizing an enhancement-mode load transistor and an enhancement-mode driver transistor. Note that the gate and drain terminals of the load transistor are tied together (i.e., $V_{GS} = V_{DS}$).

mode load transistor tied to its drain terminal (i.e., $V_{GS} = V_{DS}$), the transistor acts as a current source.

Figure 2.6(a) shows that as the output of the inverter increases (or the input decreases), V_{DS} of the load transistor decreases, and the load transistor's supplied current decreases. This allows the current supplied by the load transistor to gradually decrease until an abrupt turning off of the load transistor when the V_{GS} of the load transistor drops below its threshold voltage. Therefore the output can only rise up to within the load transistors threshold voltage of the high supply rail, i.e., $V_{OUT-Max} = V_{DD} - V_{TH-Load}$ [23].

Three distinct regions in the inverter transfer curve are indicated in Fig. 2.6(b). In region I, where the driver transistor is in cutoff, the load transistor is in saturation,

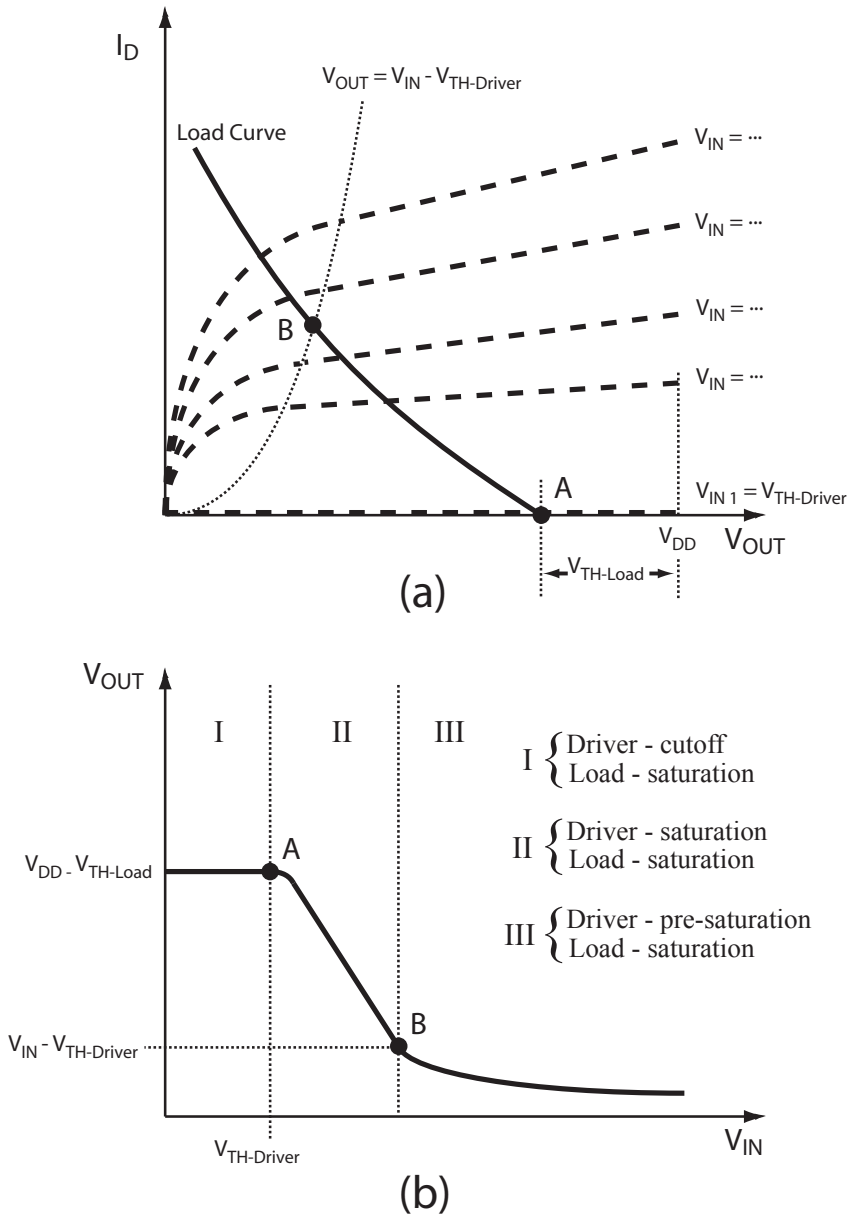

Figure 2.6: Operation of an n-type only inverter utilizing an enhancement-mode load transistor and an enhancement-mode driver transistor is shown by (a) I_D-V_{OUT} output curves for the driver (dashed) and load (solid) transistor, and (b) the transfer characteristic of the inverter. Key transitions for transistors are marked by (A) the driver transistor changing from cutoff to saturation, and (B) the driver transistor changing from saturation to pre-saturation. Note the output is only allowed to reach the high supply rail less the threshold voltage of the load transistor (i.e., $V_{OUT-Max} = V_{DD} - V_{TH-Load}$).

and the output is high. In region II, where the driver transistor is in saturation, the load transistor is in saturation, and the output is falling with maximum gain. In region III, where the driver transistor is in pre-saturation, the load transistor is in saturation, and the output is low. These regions are defined by key transition points. The first transition (A) is where the driver transistor changes from cutoff to saturation, and is defined by [23]

$$V_{GS-Driver} = V_{TH-Driver}. \tag{2.2}$$

The transistor is in saturation because the $V_{DS-Driver}$ (defined as V_{OUT}) is at $V_{DD} - V_{TH-Load}$. Since $V_{GS-Driver} = V_{IN}$ the equation can be rewritten as,

$$V_{IN} = V_{TH-Driver}. \tag{2.3}$$

The second transition (B) is where the driver transistor changes from saturation to pre-saturation, and is defined by

$$V_{DS-Driver} = V_{GS-Driver} - V_{TH-Driver}. \tag{2.4}$$

Since $V_{DS-Driver} = V_{OUT}$, and $V_{GS-Driver} = V_{IN}$ the equation can be rewritten as,

$$V_{OUT} = V_{IN} - V_{TH-Driver}. \tag{2.5}$$

Enhancement-mode load inverters suffer from limited output swing (i.e., $V_{OUT-Max} = V_{DD} - V_{TH-Load}$), and low gain. To achieve better performance, the load characteristics must be improved upon. Several other n-type inverter load options exist that do not require p-type (i.e., CMOS) channel materials. These load options include bootstrapping, as discussed in Section 2.4.2, and using a depletion-mode gate-source tied transistor, as discussed in Chapter 7.

2.4.2 Bootstrapped Inverter

Another advanced option for n-type only circuitry is the so-called "bootstrapped" design [24]. This design has the advantage of using only one type of channel (i.e., all n-type enhancement-mode devices). Figure 2.7 shows how the classic diode-tied enhancement-mode transistor load is augmented by the addition of a capacitor and third transistor. The capacitor acts as a voltage source, forcing the output and load transistor gate terminal to shift together. This acts as dynamic loading, decreasing or increasing the output resistance, as needed, to promote the inverter output transition from high to low or low to high. The third transistor is a merely a current source to charge the capacitor [24, 25]. The bootstrapped design is used within this work to

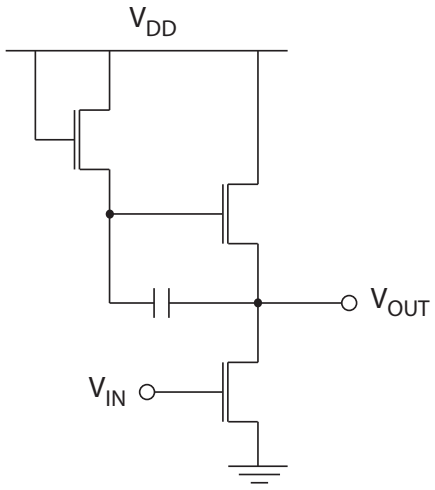

Figure 2.7: Schematic of an n-type only inverter utilizing the bootstrapped design. Note that the gate and output terminals of the load transistor are capacitively coupled, creating a dynamic load.

create ring-oscillators, and a modified version is used in a low power latch design for an RFID tag.

2.4.3 Ring Oscillator

Ring oscillators are fabricated by stringing odd numbers (greater than one) of inverters together in a circular (ring) formation to create alternating input/output voltages, as shown in Fig. 2.8. By using an odd number of inverters in a circular

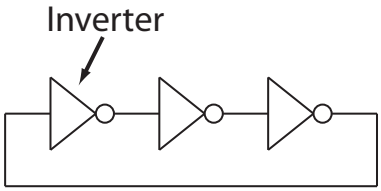

Figure 2.8: Schematic of a three-stage ring oscillator. Note that with any odd number of inverter stages (greater than one), no stable inverter input/output state of high/low exists. Any node between inverter stages can be considered an output.

formation, no stable inverter input/output state of high/low exists. The lack of a stable state forces the circuit to oscillate at a specific frequency based upon the relationship,

$$f = \frac{1}{2 \cdot n \cdot t_d}, \tag{2.6}$$

where n is the number of inverter stages, t_d is the delay per inverter stage, and f is the output frequency of the ring oscillator. Therefore, ring oscillators with fewer stages oscillate faster. However, in order to sustain oscillation, the required level of DC gain in each inverter stage is inversely proportional to the number of stages. This gain per stage requirement is explained using the Barkhausen Criterion for an oscillating system. This states that the magnitude of the loop gain ($|A(s)|$) must be greater than or equal to one, and the phase of the loop gain ($\angle A(s)$) must be 180°.

The loop gain of a ring oscillator is defined as,

$$A(s) = \left[\frac{-A_o}{1+\frac{s}{\omega_p}}\right]^n, \tag{2.7}$$

where A_o is the DC gain of a single inverter stage, ω_p is the pole frequency of a single inverter stage, and n is the number of inverter stages. Equation 2.7 assumes that all inverter stages are equal. Note that $s = j\omega_{osc}$ where ω_{osc} is the frequency of oscillation. Applying the Barkhausen Criterion to Eq. 2.7 and solving for when $|A(s)| = 1$ (to find the *minimum* gain per stage required) leads to,

$$\left|\frac{-A_o}{1+\frac{s}{\omega_p}}\right|^n = 1. \tag{2.8}$$

Next, substituting $j\omega_{osc}$ for s and solving for the magnitude in Eq. 2.8 leads to,

$$\frac{-A_o^n}{\left(1+\frac{\omega_{osc}}{\omega_p}\right)^n} = 1. \tag{2.9}$$

Then, substituting $j\omega_{osc}$ for s and applying the Barkhausen Criterion to Eq. 2.7 and solving for when $\angle A(s) = 180°$ leads to,

$$\frac{\omega_{osc}}{\omega_p} = \tan\left(\frac{-180°}{n}\right). \tag{2.10}$$

Finally, simplifying Eq. 2.9 using Eq. 2.10, results in,

$$A_o = \sqrt{1+\left(\tan\left(\frac{-180°}{n}\right)\right)^2}. \tag{2.11}$$

Equation 2.11 defines the relationship between the required DC gain per inverter stage and the number of inverter stages [26]. When Eq. 2.11 is plotted, as in Fig. 2.9, it becomes apparent that ring oscillators with five or less stages require significantly

more DC gain per inverter stage. Consequently, most reported ring oscillators have many (i.e., ≥ 7) stages in order to meet the DC gain per stage requirements with enhancement-mode load inverters which exhibit rather poor DC gain. In addition, more inverter stages are sometimes used to demonstrate integrated circuit complexity [27].

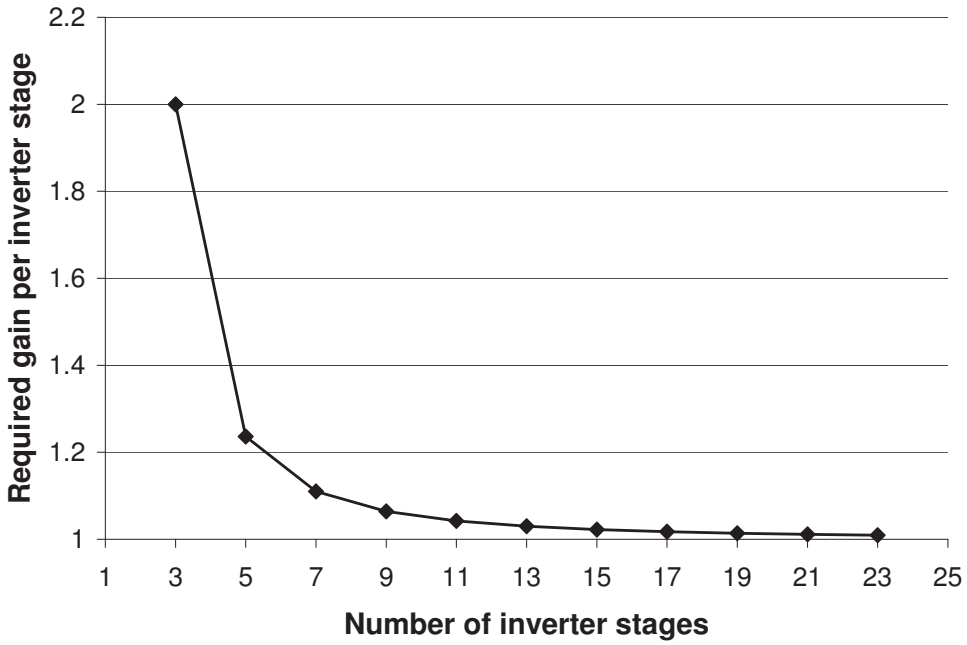

Figure 2.9: Plot of the required DC gain per inverter stage versus the number of inverter stages of a ring oscillator.

Ring oscillator outputs are normally buffered by placing another inverter between the test probe and the ring oscillator, as shown in Fig. 2.10. The buffer prevents additional loading by the test probe which may slow the output frequency of the ring oscillator.

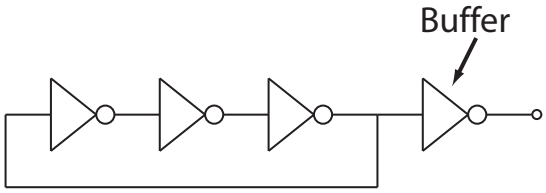

Figure 2.10: Schematic of a buffered three-stage ring oscillator.

2.5 Transparent Circuits

Transparent circuits are a relatively new reality. It was not until 2006 that the first fully transparent circuit was created [28]. Despite this technology's infant status, several possible applications have already been identified. For example, display technologies which utilize both passive and active transparent electronics [29]. Another example is interactive mirrors and windows. Transparent electronics within these common glass surfaces could cancel either light, noise, or both. The window could darken on a bright day, or use piezo-like technology to cancel outside/background noise [9]. Another interesting idea is, AOS can be used to create "functional windows". These windows, while still transmitting visible light, will absorb ultra-violet (UV) light and generate electric power. This would constitute a transparent solar cell.

The first transparent circuit was created by Presley et al. at Oregon State University in 2006. The circuit was a 5-stage ring oscillator, operating at a maximum frequency of ∼2.2 kHz with a 30 V supply, and ∼9.5 kHz with a ∼80 V supply. This circuit was never fully optimized for performance and suffered from extreme capacitive parasitics due to source/drain contacts to gate contact overlap (i.e., $GSD_{OVERLAP}$ =200 μm). This greatly degraded the output frequency of the oscillator. However, due to the rather large size of the TFTs used, the current driving

capabilities were reasonable, providing a buffered output swing of 8 V using the 30 V supply [28].

2.5.1 Previous Work With *Partially*-Transparent AOS Circuits

To the author's knowledge, Presley et al.'s first example of a transparent circuit, still remains as the only true *fully* transparent circuit. Therefore, discussions of transparent circuits must be broadened. This section includes a short list of circuit work, which could have very well been transparent (e.g., containing AOS, or similarly transparent channel material), yet was fabricated with opaque metal layers, and/or opaque substrates. These circuits are referred to as partially-transparent circuits.

Ring oscillators account for the majority of AOS circuits. Published in April 2007 is a paper by Ofuji et al. [30] where a 5-stage ring oscillator is fabricated with IGZO TFTs. At the time of publication, this was the fastest ring oscillator known. The 5-stage oscillator had an output frequency of 410 kHz with an 18 V power supply. This corresponds to a delay per stage of 240 ns.

The TFTs fabricated were bottom-gate structure, using electron-beam deposited 50 nm thick Ti (5 nm)/Au (40 nm)/Ti (5 nm) pattered via lift-off for gate contacts, RF magnetron sputtered 100 nm thick SiO_2 patterned via buffered HF (wet etch) as the gate insulator, and electron-beam deposited Ti (5 nm)/Au (150 nm) source/drain contacts patterned via lift-off. The substrate was glass. The channel material was a RF magnetron sputtered deposited (of unknown thickness) layer of IGZO (unspecified patterning technique). The channel material was never intentionally annealed, which combined with the low temperature processing techniques used, makes this circuit compatible with plastic (and therefore flexible) substrates.

TFT performance was moderate with a saturation mobility of 18.2 cm^2/Vs, turn-on voltage of $\sim$-2.5 V, and threshold voltage of $\sim$3.7 V. Parasitic overlap was greatly reduced to $GSD_{OVERLAP} = 5\mu$m. This, plus the lowered resistance of the

metal layers (i.e., RC time constants!), and increased TFT performance can account for the faster oscillation and shorter delay per stage when compared to Presley et al.

In December 2007, Sun et al. [27] published a paper where they used ZnO TFTs to produce 5-, 7-, and 15-stage ring oscillators. Their published 7-stage oscillator had an output frequency of 1.04 MHz with a 32 V power supply. This corresponds to a delay per stage of 75 ns and was the fastest known at the time of publication (based on delay per stage, not the output frequency).

The TFTs fabricated were bottom-gate structure, using ion-beam sputtered 100 nm thick chromium pattered via wet etch for gate contacts, atmospheric pressure chemical vapor deposition (APCVD) 100 nm thick Al_2O_3 patterned via dilute HF (wet etch) as the gate insulator, and thermally evaporated aluminum source/drain contacts (of unknown thickness) patterned via lift-off. The substrate was glass. The channel material was a APCVD deposited 20 nm thick layer of undoped ZnO and patterned in dilute HCL. The channel material was annealed in situ during deposition at 200 °C.

TFT performance was moderate with a field-effect mobility of > 15 cm^2/Vs, turn-on voltage of $\sim$0 V, threshold voltage of 14 V, subthreshold swing of < 0.5 V/decade, and a drain current on-to-off ratio of $> 10^8$. The parasitic overlap was minimal at $GSD_{OVERLAP} = 2\mu$m, and can account for most of the performance improvement (i.e., delay per stage and output frequency) compared to Ofuji et al.

Another example of emerging partially-transparent AOS circuits is that of an active-matrix back plane for displays. In 2008, Jeong et al. [29] used a-IGZO TFTs to drive a 12.1-inch WXGA active-matrix organic light emitting diode (AMOLED) display. This paper highlights advantages of AOS compared to poly- and a-Si:H for use as display drivers. Quoting Jeong et al., "It was found that the fabricated AMOLED display did not suffer from the wellknown pixel non-uniformity of luminance, even though the simple structure consisting of 2 transistors and 1 capacitor was adopted as a unit pixel circuit, which was attributed to the amorphous nature of IGZO semi-

conductor." This statement eloquently shows how the amorphous nature of AOSs gives the technology a distinct advantage over poly-silicon technology. In addition it is stated that, "The AMOLED display with a-IGZO TFT array would be promising for large size applications such as note PC and HDTV because a-IGZO semiconductor can be deposited on large glass substrate[s] (> Gen. 7) using conventional sputtering systems[s]." Conventional sputtering offers numerous advantages including room-temperature depositions, precise stoichiometric control, and ease of large substrate.

All TFTs reported in Jeong's paper are of staggered bottom-gate structure, using molybdenum gate contacts, PECVD deposited SiO_x or SiO_x/SiN_x bilayer as the gate insulator. Also, an etch stop layer (ESL) was used to protect the channel layer during the molybdenum or Ti/Al/Ti source/drain contacts dry etch patterning. The composition of the ESL was not reported. No thin film thicknesses were reported. The substrate was SiO_x coated glass. The ESL may also act as a passivation layer. The paper does include performance and stability measurements for the IGZO TFTs, including a study on the effects of different ESL materials. The channel material was a APCVD deposited 20 nm thick layer of undoped ZnO and patterned in dilute HCL. There is no discussion of the channel layer annealing, and so it is assumed that no intentional heating took place.

TFT performance was moderate with a field-effect mobility of 8.2 cm^2/Vs, turn-on voltage of ∼-2 V, threshold voltage of 1.1 V, subthreshold swing of 0.58 V/decade, and a drain current on-to-off ratio of $> 10^8$. Despite the moderate TFT performance, the AMOLED display performs very well. The 12.1-inch display has 123 ppi resolution with 1280 x RGB x 768 pixels and a panel size of 283 x 181 mm^2.

In September 2008, McFarlane at Oregon State University fabricated AC to DC rectifying circuits [31]. McFarlane used two difference architectures, one being a full bridge rectifying using diode-tied transistors instead of diodes, and the second being a "cross-tied" design using two diode tied transistors and two transistors acting as

switches [32]. The TFTs fabricated were bottom-gate structure, using RF sputtered ∼150 nm thick ITO pattered via photolithography and wet etch for gate contacts, plasma enhanced chemical vapor deposition (PECVD) 100 nm thick SiO_2 patterned via photolithography and dilute HF (wet etch) as the gate insulator, and thermally evaporated ∼500 nm thick aluminum source/drain contacts patterned via lift-off. The substrate was glass. The channel material was an RF sputter deposited ∼50 nm thick layer of IGO and patterned in dilute HCL. The channel material was post deposition annealed in air at 400 °C.

TFT performance was moderate with a incremental mobility of 14 cm^2/Vs, average mobility of 10 cm^2/Vs, turn-on voltage of ∼1 V, threshold voltage of ∼5.7 V, and a drain current on-to-off ratio of $\sim 10^7$. The parasitic overlap was moderately low at $GSD_{OVERLAP} = 10\mu$m.

McFarlane's AC to DC rectifiers (i.e., full bridge and cross-tied architectures) performed well. The cross-tied performed better at high input frequencies, maintaining rectification to the testing setup limit of 20 MHz with little output voltage swing decay. As expected, output swing proved to be very dependent on the output loading and peaked at ∼45% of the input swing with a load of 2 MΩ. The cross-tied architecture proved to be superior except for the asymmetrical nature of the output. The lower, or negative output, (DC signal) showed nearly 5 V of of peak to peak ripple which was not smoothed by the circuit. This could have been overcome with the addition of filtering components.

In December 2008, Heineck at Oregon State University was successful in fabricating depletion-mode load inverters [33]. The depletion-mode channel material was realized as a two part deposition process. The first part was identical to the enhancement-mode channel, sharing the same deposition and patterning processes. The second deposition was done over the first deposition (selectively to the depletion-mode transistors only via lift-off patterning) and differed by changing the RF sputtering parameters from that of the first channel deposition. Changes included lowering

the oxygen partial pressure to zero and increasing the RF power. This "stacking" method also provided a thicker overall channel which is known to decrease the turn-on voltage slightly.

The TFTs fabricated were bottom-gate structure, using RF sputtered ∼150 nm thick ITO pattered via photolithography and wet etch for gate contacts, plasma enhanced chemical vapor deposition (PECVD) 100 nm thick SiO_2 patterned via photolithography and dilute HF (wet etch) as the gate insulator, and thermally evaporated ∼500 nm thick aluminum source/drain contacts patterned via lift-off. The substrate was glass. The channel materials, both enhancement- and depletion-mode channels, were RF sputter deposited layers of ZTO and patterned via dry etch and lift-off patterning respectively. The channel material was post deposition annealed in air at 400 °C.

TFT performance was moderate with a incremental mobility of ∼14 cm^2/Vs, average mobility of ∼7 cm^2/Vs, enhancement-mode turn-on voltage of -2.5 V, depletion-mode turn-on voltage of -8 V, enhancement-mode threshold voltage of ∼4.5 V, and depletion-mode threshold voltage of ∼-4 V. Heineck's inverter performance was impressive, with a peak gain of 10.6 V/V. The inverter voltage transfer characteristic (VTC) (see Section 3.7.5 for a detailed discussion on VTC) was not centered between ground and V_{DD}. This issue is easily solved by changing the threshold voltages of the load and driver transistors.

In later examination of Heineck's process, it was found that the two stacked channel layers contained unavoidable contamination from the pre-second-channel-deposition lift-off photolithography processing. This contamination gave rise to a "kink" in the $log(I_D)$-V_{GS} transfer curves, which is thought to be caused by acceptor like traps at the channel-insulator interface [9]. This kink usually occurs in the subthreshold region of the transistor transfer curve, and results in a decreased turn-on voltage and slightly decreased threshold-voltage.

In October 2009, Lee et al. published their results of a depletion-mode load inverter using IGZO as the channel material [34]. The control of V_{ON} and V_{TH} for enhancement versus depletion mode operation was achieved by varying the channel thickness. This publication did not include statements of TFT performance, but did provide a few figures depicting TFT transfer (I_D - V_{GS}) and output (I_D - V_{DS}) curves. By examining the output of the inverter and understanding the inverter VTC, it can be seen that the inverter VTC can not be reproduced using the provided TFT tranfer and output curve data. Careful examination also shows that the sizing (W/L) of the circuit versus discrete devices shown also differs. Therefore, different TFTs must be used for the inverter circuit than the transfer and output curves. Despite this confusion, the inverter is reported to have excellent performance using a voltage supply of $V_{DD} = 20$ V. Peak DC gain was 37.4 V/V, and the VTC was very centered and balanced with the peak DC gain and shift from low to high occurring at midrail, $\sim V_{DD}/2 = 10$ V. Noise margins were also large and balanced at $NM_H = 8.2$ V and $NM_L = 8.4$ V. Using varying channel thicknesses to control V_{ON} has been explored (by the author of this thesis and others [35]) where similar a trend, but to a much lesser extent, has been observed. It is unlikely that such a drastic trend as seen in Lee et al. is entirely channel thickness dependent. Similarl to that of Heineck's results, an interfacial contamination layer may have a profound, yet unreported (or unknown to the authors), effect on V_{ON}. However, it is not reported which IGZO channel layer (enhancement or depletion) was deposited first, nor how the IGZO channel layers were pattered (i.e., wet or dry etching and photolithography may shift V_{ON} and contribute to contamination), it is impossible to conclude what or if any interfacial layer is to blame.

2.5.2 Previous Work With Competing Technology

Not all partially-transparent circuits were created using AOS channel layers. Several competing technologies deserve mention. Organic semiconductors have be-

come increasingly popular over the past few years [36]. Organic light-emitting diodes (OLEDs) and similar optical devices are often used in displays and provide good transparency [37]. Organic semiconductors can be deposited at low temperatures, and unlike AOS, are not post-deposition annealed. This lack of annealing is not only required for organic semiconductors due to their weaker atomic bond strengths, but does make them attractive for use with transparent and flexible (i.e., plastic) substrates. However, the use of organic semiconductors as channel materials in TFTs is more limited. Organic semiconductors suffer from low mobility (often $\ll 1$ cm^2/Vs) [36], which coupled with the restriction to use only lower electronic fields (high electric fields break the weaker organic atomic bonds which causes irreversible damage and transistor instability [38]), produces poor TFT output currents. To increase the current output, very large (W/L) transistors could be implemented. However, large transistors require greater areas over which both semiconductors and insulators must be defect free for reliable operation. Despite these performance limitations, organic semiconductors are being extensively explored internationally.

As briefly mentioned above, motivation for McFarlane's AC to DC rectifier circuits and circuit design originated from a publication by Rotzoll et al. in March 2006 [32]. Organic semiconductors were used to create AC to DC rectifier circuits operating with 13.56 MHz (RF) input frequencies. Organic semiconductor TFTs are though to have a unity-gain bandwidth of 1 MHz, making RF operation seemingly impossible. However, Rotzoll's TFTs operated in the nonquasistatic (NQS) regime of operation, successfully opening the possibilities for organic semiconductors to include high frequency circuits.

The number of high frequency, specifically RF, applications have increased at a dramatic rate. RFID tags (i.e., RF transponders for multi-bit identification messages) have seen widespread use in everything from anti-theft devices to door lock key cards. Thus, as the volume of these often disposable devices increases, a cheaper technology

is desired. Again, TFT technologies, including a-Si, AOS, and organic semiconductors are found to be attractive solutions for RFID applications.

In January 2007, Cantatore et al. published a 13.56 MHz (i.e., the industry standard RF frequency) RFID system based on organic transponders [39]. These transponders were capable of generating complex 64-bit identification codes at 13.56 MHz. The bit rate was 150 b/s with an internal clock frequency of 150 Hz using a -30 V supply. This trumped the previous organic code generators which were capable of producing 15-bit code at the same 13.56 MHz frequency [40]. The TFTs were fabricated using a co-planar bottom-gate structure. The TFTs fabricated were co-planar bottom-gate structure, 50 nm thick gold layer pattered via photolithography and wet etch for gate contacts, spin-deposited poly-4-vinylphenol (PVP) patterned photochemically as the gate insulator, and gold source/drain contacts. The substrate was a 25 μm thick polyimide foil laminated on a rigid support to facilitate handling. The channel material was a spin-deposited organic semiconductor pentacene precursor, and converted to pentacene by the retro Diels-Alder reaction [41]. The transponder circuits used a classic design in which the 13.56 MHz reader output is capacitively coupled to the RFID tag. The RFID tag rectifies the 13.56 MHz for DC power. Code is generated via row and column shift registers and a 64-bit ROM. The code is then synchronized and fed back into the reader, carried on the same 13.56 MHz signal. This publication is significant since it demonstrates that complex and potentially profitable electronics applications are possible even with a carrier mobility of $\ll 1$ cm^2/Vs.

An interesting solution to the problem of being limited by a n-type only circuit architecture, is to use AOS for n-type and organic semiconductors for p-type TFTs, thereby creating a complementary circuit architecture. An example of using two different channel materials for complementary design is a publication by Oh et al. in which ZnO and pentacene are used for n-type and p-type TFTs, respectively, to build an inverter on a polyethersulfone (PES) substrate [42]. These inorganic-organic

hybrids offer substantial electronic performance gains (i.e., the ∼100 DC gain of the inverter reported by Oh et al.) but at a price of significant process integration complexity and technology incompatibilities (e.g., low thermal budget of the organic channel and substrate materials and mobility mismatch between the inorganic and organic TFTs). The ZnO channel material was RF sputtered first, followed by thermal evaporating the pentacene. The PES substrate was purposely heated to 100° C during the ZnO deposition. To ease process integration, shadow masks were used for all patterning, including the gate contacts, both channel materials, and source/drain contacts. Via fabrication to the gate contacts was not reported. In this particular example, the n-type and p-type TFT showed similar mobility (0.9 cm^2/Vs and 0.4 cm^2/Vs saturation field effect mobility respectively). The unusually low mobility of the ZnO devices can be partially attributed to the un-annealed (as deposited) state of the devices. A highlight of the publication is that the substrate (PES) is quite flexible. Flexed and un-flexed measurements of the inverter show a similar output with minimal degradation. In addition, long-term stability testing of the inverter also showed minimal degradation. Such inorganic-organic hybrid devices show promise for low voltage (to avoid irreversible damage to the organic channel material [38]), and therefore low current (due to the rather poor mobility) applications. Such applications include switching networks and digital logic.

3. EXPERIMENTAL TECHNIQUE

This chapter reviews different methods of thin-film processing used in this work, including thin-film deposition and patterning [43]. Additionally, device and circuit characterization and design considerations are discussed.

3.1 Physical Vapor Deposition

Physical vapor deposition (PVD) refers to a wide variety of thin-film deposition techniques which physically convert a solid or liquid source into its vapor phase. The vapor is then transported across a region of reduced pressure, often created in a vacuum chamber, from the source to the substrate. The vapor then condenses onto the surface of the substrate (and the surrounding vacuum chamber) [43]. Two common PVD methods used in this work are radio frequency (RF) magnetron sputtering and thermal evaporation.

3.1.1 Radio-Frequency Sputtering

Sputter deposition is a common method for thin film deposition and is often preferred over other PVD techniques (e.g., thermal evaporation, Section 3.1.2). Several reasons exist for this preference for sputtering including good uniformity over large area, precise film thickness control, both room temperature and heated deposition capability, and ease of multicomponent thin film deposition due to excellent control of film stoichiometry [43].

Several types of sputtering exist, including RF magnetron sputtering, which is used in this work exclusively. RF sputtering is used because of difficulties inherent in DC sputtering using an insulating target. While DC *reactive* sputtering with a metal target was also explored, ultimately RF sputtering proved to be superior for this work.

Figure 3.1 depicts RF sputter deposition and shows how sputtering is the ejection of atoms or molecules from a target surface when it is struck by accelerated positive ions. The ejected particles create a plume of material which deposits onto the substrate. Ions (both positive and negative) are created via a RF generated plasma (glow discharge) and are accelerated due to a DC bias which is created by a phenomenon known as "self-bias", in which lighter electrons are more rapidly accelerated to the electrode (target) surface during the positive portion of the RF AC input voltage than are heavier ions during the negative portion of the RF AC input voltage. After several RF AC cycles, a negative potential builds up at the target. This creates a strong attraction for positive ions, resulting in their acceleration towards the target [33], [43]. In this work, both argon and oxygen are used as sputter gases. Argon

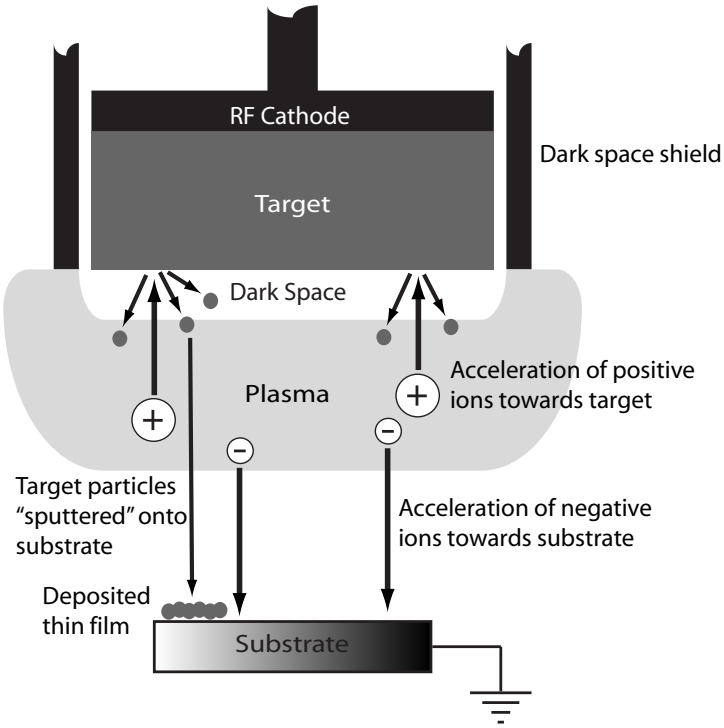

Figure 3.1: A schematic illustrating basic aspects of RF sputtering.

serves as the heavy, nonreactive positive ion for sputtering. Oxygen is introduced to more precisely control the film stoichiometry. The presence of oxygen can result in "negative ion resputtering", in which the negative ions (e.g., oxygen or fluorine) are accelerated towards the substrate instead of the target. This reactive oxygen bombardment of the target can lead to nonuniformity and substrate sputtering problems [33].

Magnetron sources increase the percentage of electrons that cause ionizing collisions, thereby sustaining the glow discharge, by utilizing a magnetic field to confine electrons near to the target surface. In addition, the magnetic field can also be customized to promote more uniform utilization of the target and, therefore, larger targets. Also, a magnetic field helps to sustain a glow discharge at a lower pressure [43].

In this work all AOS channel layers and ITO top contacts (source, drain, traces, etc.) are deposited by RF magnetron sputtering using the *TANG* (Tasker-Chiang) custom-built sputtering system [13]. This system features a 600 W RF power supply, 1.5 kW DC power supply, three 2-inch sputter guns, two 3-inch sputter guns, a load-locked chamber, z-axis in situ translation, turbomolecular high vacuum pumping, and a custom computer-controlled user interface.

3.1.2 Thermal Evaporation

Thermal evaporation is a PVD method by which thermal energy is used to create the physical vapor of the source material. Figure 3.2 illustrates a typical thermal evaporation tool layout. The source material is placed within a boat or filament which is resistively heated by current flow through it. The source material either melts and subsequently evaporates, or sublimates (i.e., goes directly from the solid phase to the gas phase). The vapor then condenses onto the substrate, which is usually placed directly above the source. For this work thermal evaporation is

used for depositing aluminum source/drain electrodes and interconnects. Thermal evaporation is performed using a Polaron Thermal Evaporation tool.

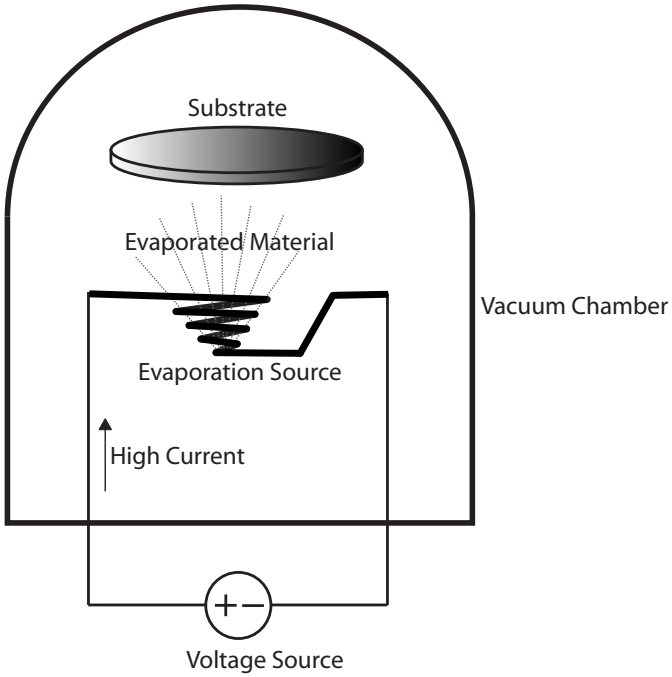

Figure 3.2: Schematic of a thermal evaporator showing the evaporation source and substrate placement.

3.2 Chemical Vapor Deposition

Chemical vapor deposition (CVD) involves a wide variety of thin-film deposition techniques in which a gas or liquid source is used to grow a thin film. Two methods used in this work are plasma-enhanced chemical vapor deposition (PECVD) and atomic layer deposition (ALD).

3.2.1 Plasma-Enhanced Chemical Vapor Deposition

Plasma-enhanced chemical vapor deposition (PECVD) uses a radio-frequency induced plasma to increase the reactivity of the fluid sources commonly used in CVD. Classically, a high temperature (>400 °C) is used to drive a chemical reaction. PECVD is attractive in that the substrate temperature can be reduced ($250-400$ °C) while maintaining a moderate deposition rate. In this work, PECVD of the SiO_2 gate insulator layer is accomplished within a Semi-Group cold-wall, parallel-plate reactor, in which only the lower platen (grounded) is heated and the gas sources are emitted from a shower-head RF cathode, as shown in Fig. 3.3. This local heating helps to

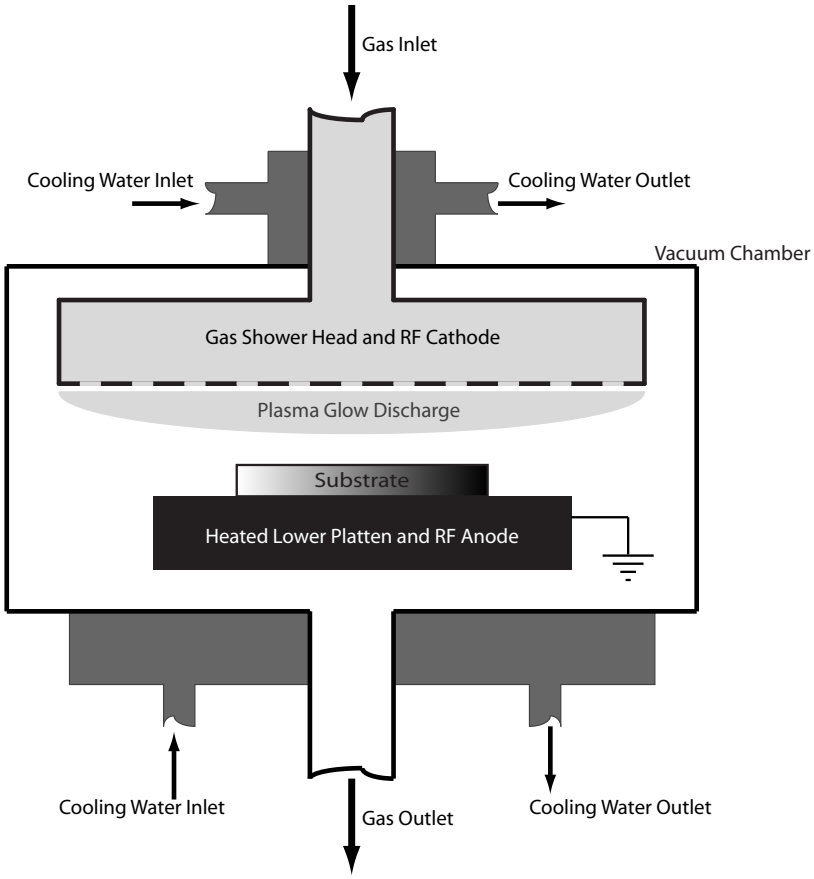

Figure 3.3: Schematic of a PECVD reactor showing the heated lower platen, cold-wall chamber (water cooled), and gas showerhead RF cathode.

reduce unwanted deposition within the chamber and, in turn, reduces the required frequency for cleaning and maintenance. While only the lower platen on which the substrate lays is heated, the chamber walls may still be inadvertently warmed, resulting in some deposition occurring away from the lower platen. However, due to the lower temperature of the chamber walls, this deposition is more porous and less adhesive. Therefore, it contributes to particle contamination within the deposited thin film [43].

3.3 Photolithography

Photolithography is a process whereby a specific pattern is transferred into a thin-film layer of a photosensitive polymer (photoresist) by the use of high intensity short-wavelength light (exposure) and selective wet etching (development). The resist then serves as a mask, either protecting underlying layers from etching, or as the release layer in a technique known as lift-off (described in Section 3.5).

The specific process, shown in Fig. 3.4, is to first spin coat the substrate with the photoresist, followed by an initial bake. Second, the resist is preferentially exposed to UV light through a photomask. Third, the photoresist is preferentially removed with Micro Posit 351 developer (i.e., positive resist exposed to light is removed). The substrate is then again baked. Finally, the underlying material is etched (wet or dry, as described in Section 3.4) and the photoresist is removed altogether. The photoresist bake times are of variable duration depending on the environmental temperature and humidity. A hotplate temperature of 85 °C is used to avoid excessive dehydration, shrinking, and cracking of the resist. In addition, the use of hexamethyldislazane (HMDS) as a primer to promote photoresist adhesion greatly reduces mask undercutting during the etch step. HMDS also aids in a lift-off process, providing stability through better adhesion for long, narrow photoresist lines (e.g., TFT length definition in the source/drain layer). The specific HMDS product used is MCC Primer 80/20 (20% HMDS and 80% PM Acetate) and is purchased from MicroChem [44].

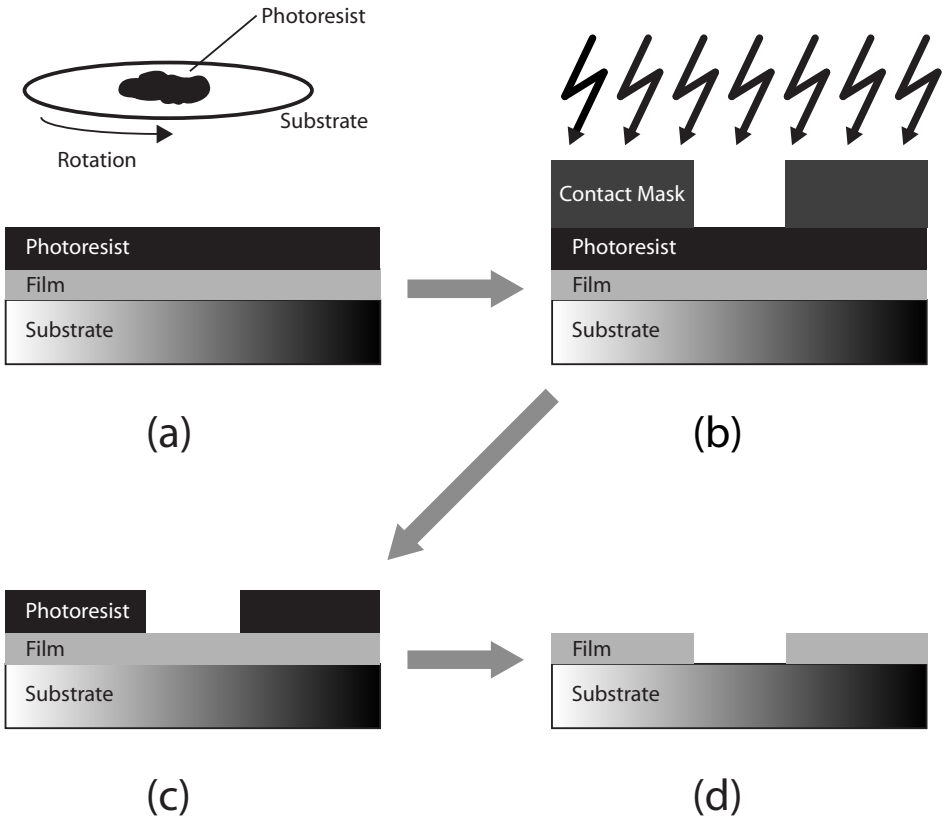

Figure 3.4: Flowchart depicting the photolithography process used in this work utilizing Microposit S1818 positive photoresist and a Suss MJB3 aligner. (a) Spin coat photoresist and bake. (b) UV exposure. (c) Development and bake. (d) Material etch and photoresist removal.

The exact photolithography process including all process specifications can be found in *Appendix A: Process Flow*.

3.4 Etching

Etching is a subtractive process in which the substrate is completely covered by a thin-film layer which later is selectively removed [45]. Photolithography is usually used to create a mask which protects regions of the underlying layer from being etched. The two main methods of etching are wet etching (i.e., an aqueous acid/base mixture)

and dry etching (i.e., reactive ion etching). Two of the most important aspects of the etching process are selectivity and isotropy. These factors typically determine which method is used for a given process step. In this work, wet etching is used for defining the ITO bottom gate layer, gate insulator layer, and AOS channel layer. Top metal layers (i.e., source/drain of either aluminum or ITO) layers are patterned via lift-off patterning, as described in Section 3.5.

3.4.1 Selectivity

Different materials etch at different rates, depending on the etching method used. Selectivity refers to the relative etching rate of the targeted material layer, the mask above, and the material layer below [43]. Figure 3.5(a) is an example of good selectivity where only the targeted material is etched. Figure 3.5(b) is an example of poor selectivity, when the etch is uncontrollable due to mask etching. Such a result is also possible when there is poor adhesion between the photoresist mask and the targeted etch layer (see Section 3.3 and the use of HMDS). Figure 3.5(c) is an example of poor selectivity, when the etch is not controlled due to the underlying layers being partially or fully etched. This is extremely undesirable because the underlying layers cannot be repaired or replaced. In this case, pealing or flaking of the above layers is likely to occur.

3.4.2 Isotropy

During an etch, the targeted material may etch both vertically, as desired, and horizontally, under the mask. Figure 3.6 illustrates the two extremes, being (a) equal vertical and horizontal etching (i.e., completely isotropic), and (b) zero horizontal etching (i.e., completely anisotropic). Isotropy is a measure of how vertical the etch process is and is mathematically defined by,

$$A = 1 - L_R, \tag{3.1}$$

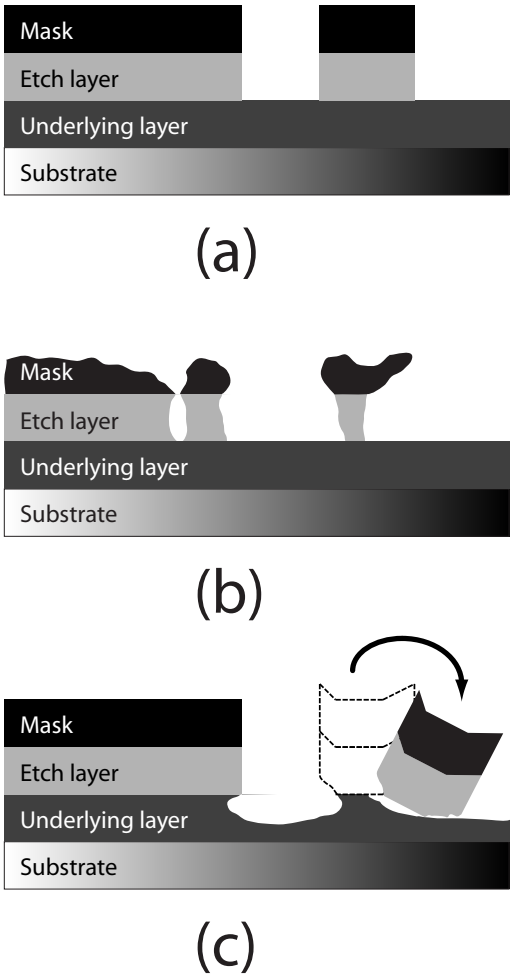

Figure 3.5: Examples of the limiting cases of etch selectivity showing (a) good selectivity, where only the targeted material is etched, (b) poor selectivity, due to mask etching and degradation, and (c) poor selectivity, due to the underlying layers being partially or fully etched.

where A is the degree of anisotropy, and L_R is the lateral etch ratio defined by,

$$L_R = \frac{\text{Horizontal Etch Rate of Material}}{\text{Vertical Etch Rate of Material}}. \tag{3.2}$$

Therefore, the degree of anisotropy, A, can vary between zero and one. If $A = 0$, then the etch is completely isotropic such that the horizontal and vertical etch rates

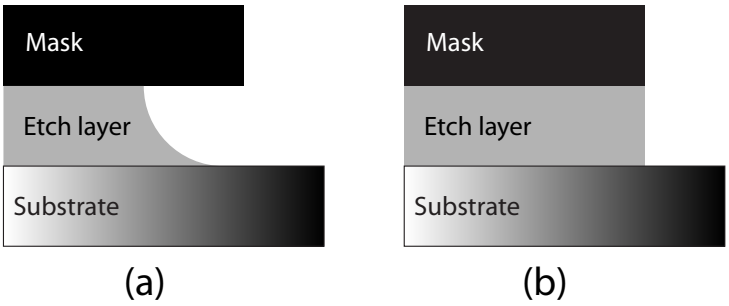

Figure 3.6: Examples of the two extremes of etching isotropy. (a) Completely isotropic, in which the horizontal and vertical etch rates are equal. (b) Completely anisotropic, in which the horizontal etch rate is zero.

are equal, as shown in Fig. 3.6(a). If $A = 1$, then the etch is completely anisotropic such that the horizontal etch rate is zero, as shown in Fig. 3.6(b) [43].

Figure 3.7 illustrates how extended isotropic overetching also results in vertical sidewalls. However, overetching is not desired as the amount of mask undercutting results in smaller feature sizes than desired. In general, it has been found that step

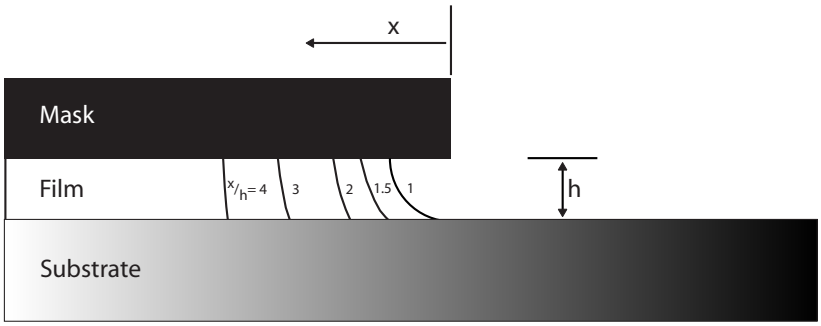

Figure 3.7: Isotropic overetching versus time. h is the film thickness and x is the horizontal overetch distance. Note that overetching results in a more vertical sidewall profile, but at a cost of mask undercutting. Therefore, overetching unintentionally leads to smaller features.

coverage can be an issue with thin-film deposition (i.e., RF sputtering) [43]. Therefore, subsequent layers over a step created from etching may benefit from isotropic etching with non-vertical sidewalls. For example, the ∼45° sidewalls created during a wet etch of an ITO bottom-gate structure allows for better sidewall coverage of the subsequently deposited gate insulator compared to the vertical sidewalls associated with a dry etch of the ITO.

3.4.3 Wet Etching

Wet etching is a isotropic etch method which utilizes an aqueous etch solution. In this work, strong acidic solutions of hydrochloric (HCl) and hydrofluoric (HF) acids are used. HCl is used for etching AOS layers utilizing a 2:1 H_2O:HCl solution for etching 2:1 ZTO, a 5:1 H_2O:HCl solution for etching 1:1 IGO, and a 200:1 H_2O:HCl solution for etching 2:1 ZIO. For experimentation with depletion-mode load circuits, where both ZIO (depletion-mode) and ZTO (enhancement-mode) AOS are used, the ZIO etches extremely quickly compared to ZTO in the same etch solution. Therefore, for good selectivity the ZTO layer is deposited and etched before the ZIO layer. This ensures that the ZTO layer remains during the ZIO etch. Also, it has been observed that annealed AOS layers etch more slowly than un-annealed layers (approximately four to five times slower for 2:1 ZTO). Thus, a two-channel circuit structure utilizing ZTO for both AOS channel layers is still possible. This can be accomplished by annealing the first AOS channel layer to increase its etch resistance and etching the unannealed second AOS channel layer.

A buffered HF solution is used for etching the SiO_2 gate insulator layer. Special care should be taken whenever HF is used. HF readily penetrates the skin and is attracted to calcium within the human body (i.e., bones and nervous system!). HF exposure can produce deep and severe burns that are often not detected until the damage has been done [45]. Often the pain of the burn is not sensed on the skin, but only with the deep internal burns. Severe exposure to HF (i.e., 50% or stronger

solution hydrofluoric acid to 1% or more body surface area) can cause systemic fluoride ion poisoning which may lead to hypocalcemia (i.e., decreased calcium levels which may cause a break down in normal cell function, neural transmission, membrane stability, bone structure, blood coagulation, and intracellular signaling) [46], hyperkalemia (i.e., increased potassium levels which may cause cardiac arrhythmias) [47], hypomagnesemia (i.e., decreased magnesium levels which may cause neuromuscular irritability, CNS hyperexcitability, and cardiac arrhythmias) [48], and sudden death [49].

3.4.4 Reactive Ion Etching

Reactive ion etching (RIE), a type of dry etching, is a anisotropic etch method which simultaneously utilizes chemical and physical effects to accomplish anisotropic etching. Gas mixtures are carefully chosen to be specific to the target layer and therefore often provide excellent selectivity. As shown in Fig. 3.8, physical etching (i.e., sputtering as discussed in Section 3.1.1) is performed with a non-reactive heavy ion (usually argon) while the chemical etch is specific to the film being etched. Note that the chamber layout is similar to that of a PECVD reactor but that the RF cathode and anode have been switched.

The two etch mechanisms (physical and chemical) must be carefully balanced and performed together. A consequence of this synergy is that during chemical etching new surface compounds are created (e.g., polymer or diamond like carbon buildup with the use of methane). Then, the newly formed layers are removed via physical etching (i.e, argon ion milling) so that the chemical etching can continue. The etch rate must be carefully maintained through balancing of the gas mixture. For example, when etching ZTO, if the mixture is too methane rich, then the polymer buildup dominates and etching ceases. In contrast, if too little methane is used, then the etch relies only on the physical etching of the argon which has poor selectivity, resulting in a degraded photoresist mask. An optimal mixture has just enough argon to remove

the polymer buildup created by the methane, allowing the chemical etch to continue [33]. This process for etching ZTO ultimately proved to be to unpredictable in the PlasmaTherm System VII available. Therefore, for this work when etching ZTO, RIE was abandoned and wet etching became the standard. In a private conversation with Tim Emery of HP, it was discussed that such RIE etching of ZTO with methane is readily possible in such systems where remote high density plasma sources are used to control the buildup of polymer or diamond-like carbon.

3.5 Lift-off Patterning

The lift-off patterning technique shown in Fig. 3.9 is an additive process in which the photoresist mask is deposited and patterned first, followed by a thin-film layer of the desired material. The photoresist is then dissolved by a solvent (i.e., acetone) while any material deposited directly on top of the photoresist is also "lifted" away. The lift-off process only works well if the thin-film layer is much thinner than the photoresist [45]. Unfortunately, lift-off may cause "flagging" and tearing, as shown in Fig. 3.9, depending on the thin film's thickness, adhesion, and breaking strength. Due to the high degree of selectivity to acetone, the lift-off technique is applied to the ITO (or aluminum) source/drain metal layer. If an etching process were to be used for source/drain patterning, then the etchant would most likely etch both the source/drain material as well as the AOS channel material.

Lift-off patterning should always be performed quickly. If the photoresist is allowed to sit on the substrate too long, then the acetone may have difficulty in removing it. Even though the use of HMDS is advised, one might infer that the increased adhesion provided may further inhibit the ability to removed the photoresist. However, this has not been observed. It is the author's opinion that the use of HMDS can only make the photolithography process, either etching or lift-off patterning, better.

Despite the ease of patterning a wide variety of materials without complicated etch chemistry, and the near-perfect selectivity that lift-off patterning provides, indus-

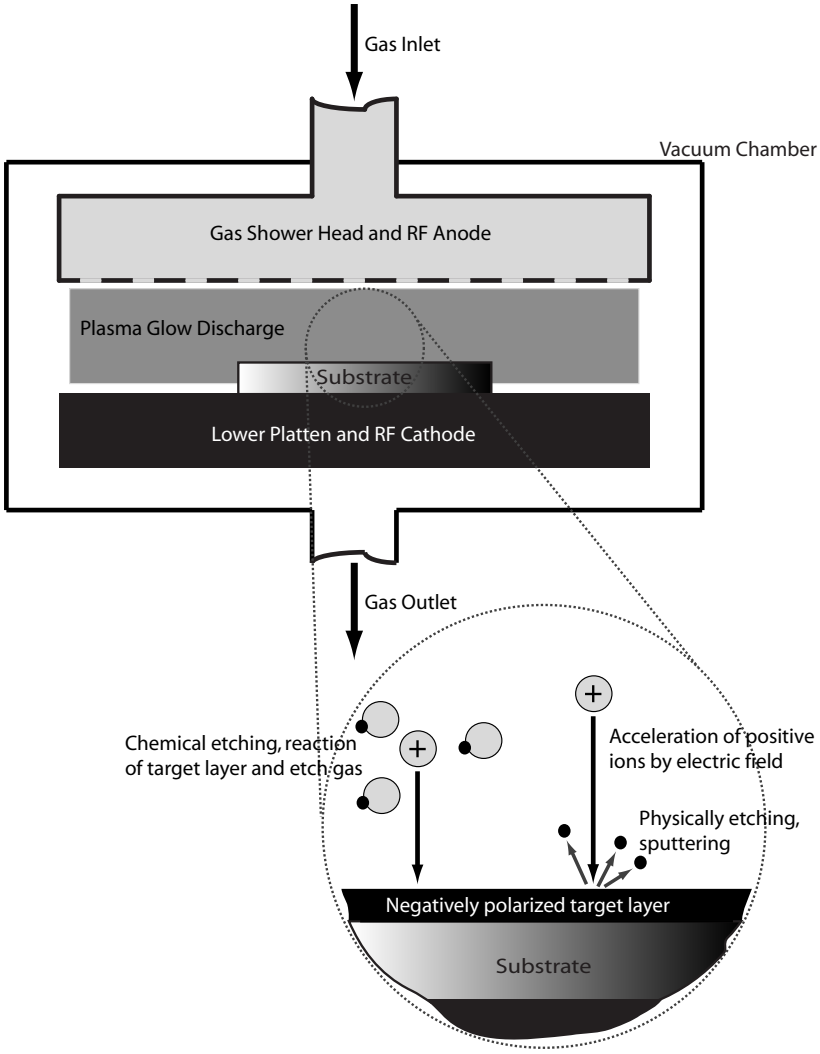

Figure 3.8: Schematic of a reactive ion etch (RIE) reactor showing gas showerhead RF anode, and lower platen RF cathode. The inset shows simultaneous reactive gas chemical etching and physical etching (sputtering or ion milling) of the target layer.

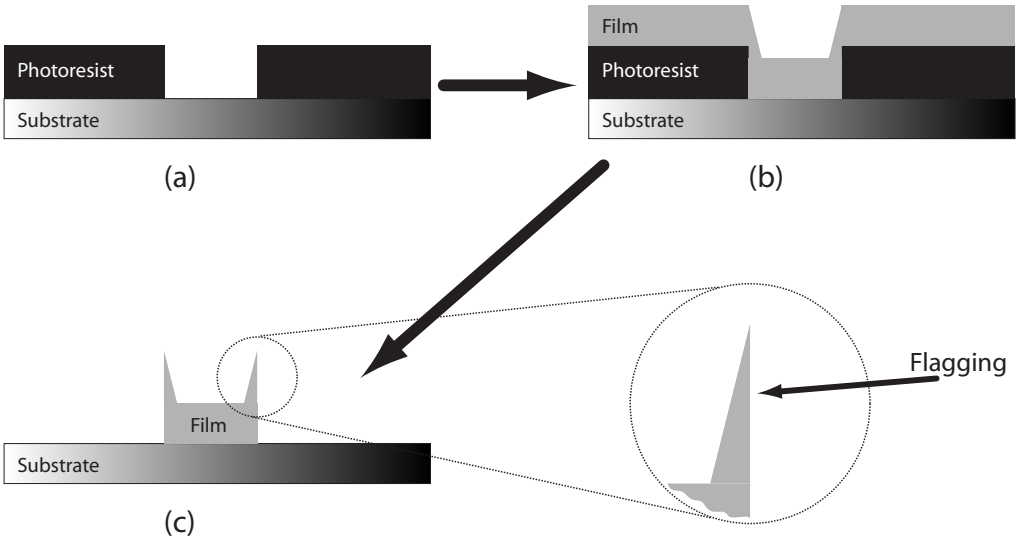

Figure 3.9: Flowchart depicting lift-off patterning. (a) The photoresist mask is deposited and patterned prior to the desired thin film deposition. (b) Addition of the thin-film layer over the pre-patterned photoresist. (c) Photoresist is removed and concomitantly "lifts" away the thin film layer above. Note that the final patterned thin-film layer contains "flagging" after photoresist removal.

try often views lift-off patterning as inappropriate for scaled up production and would rather avoid this technique. To accomplish this, and adhere to industry "standards", the use of a co-planar bottom-gate structure would eliminate the need for lift-off of the source/drain layer. However, in this work, staggered structures are used to avoid contamination from building up at the channel-insulator interface. Thus, the channel layer is deposited following gate insulator deposition with no photolithography steps in between (see *Appendix A: Process Flow*).

3.6 Thin-Film Post-Deposition Annealing

Post-deposition annealing of the AOS channel materials is a critical step which greatly affects the electrical performance of the semiconductor. For this work, the channel material is annealed in air. Air annealing of the channel (staggered bottom-gate design) results in a backside depletion layer which suppresses the electron con-

centration in the channel. As the annealing temperature increases, the TFT mobility and drain current on-to-off ratio increase, while hysteresis, turn-on voltage, and threshold voltage decrease [35]. All annealing is performed using desktop furnaces, specifically, models 47900 and 62700 by Eurotherm or Centurion Qex by Neytech. Anneal temperatures range from 200 °C to 500 °C.

3.7 Device / Circuit Characterization Methods and Metrics

This section discusses methods employed for device and circuit characterization and metrics for device and circuit performance.

3.7.1 Turn-On and Threshold Voltage

The turn-on voltage (V_{ON}) of a TFT is the potential difference between the gate (control terminal) and the source, designated V_{GS}, needed to reach an onset of the flow of drain current, as shown in Fig. 3.10(a). This voltage corresponds to the so-called flat-band voltage, since TFTs are accumulation-mode devices. V_{ON} is a parameter best suited to TFT device physics assessment. The threshold voltage (V_{TH}) of a TFT corresponds to a V_{GS} at which appreciable drain current flows, as estimated using a technique such as that shown in Fig. 3.10(b). V_{TH} is a parameter most appropriate for circuit assessment.

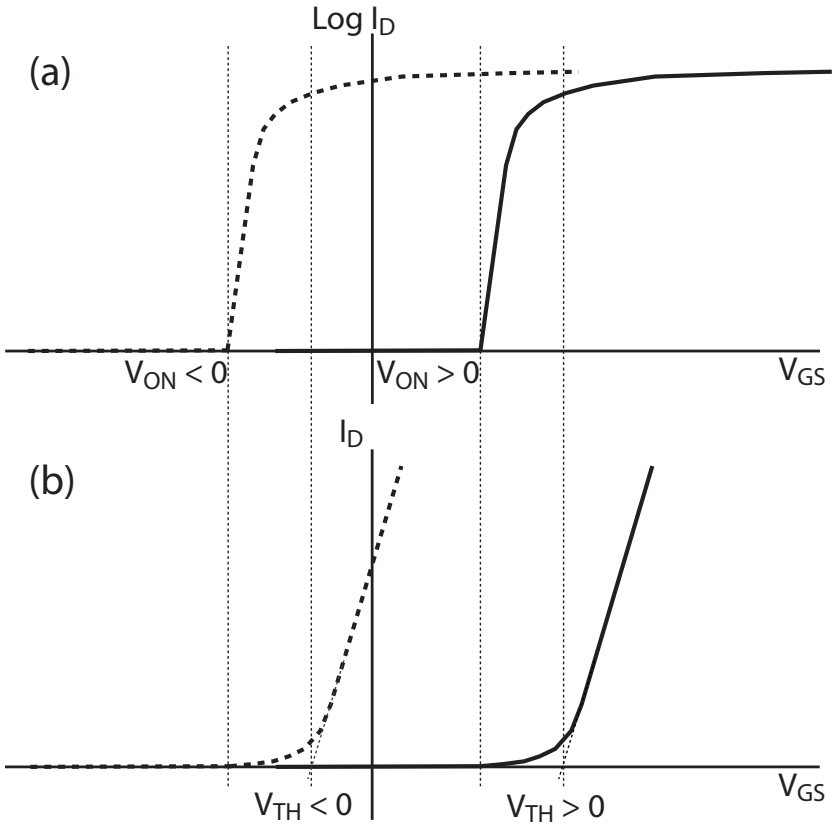

Figure 3.10: Graphical procedures for estimating V_{ON} and V_{TH} for both enhancement-mode (solid) and depletion-mode (dashed) TFTs. (a) V_{ON} is estimated as the onset of appreciable drain current using a $log(I_D)$ - V_{GS} transfer curve. (b) V_{TH} is estimated from linear extrapolation to the x-axis of an I_D-V_{GS} transfer curve for small V_{DS}'s, i.e., when $V_{DS} \leq 1$ V.

3.7.2 Mobility

Mobility estimates are extracted from TFT transfer curves, as shown in Fig. 3.11, where $V_{DS} = 1$ (keeping the TFT in non-saturation) and V_{GS} is swept. The bias sweep range is adjusted to match the TFT according to channel and gate insulator materials (i.e., avoiding high V_{GS} values when very thin dielectrics are used to protect gate insulator integrity). From the transfer curve, two different V_{GS}-dependent mobilities are extracted, incremental mobility (incremental mobility of carriers added to the channel), and average mobility (average mobility of all the carriers in the channel)

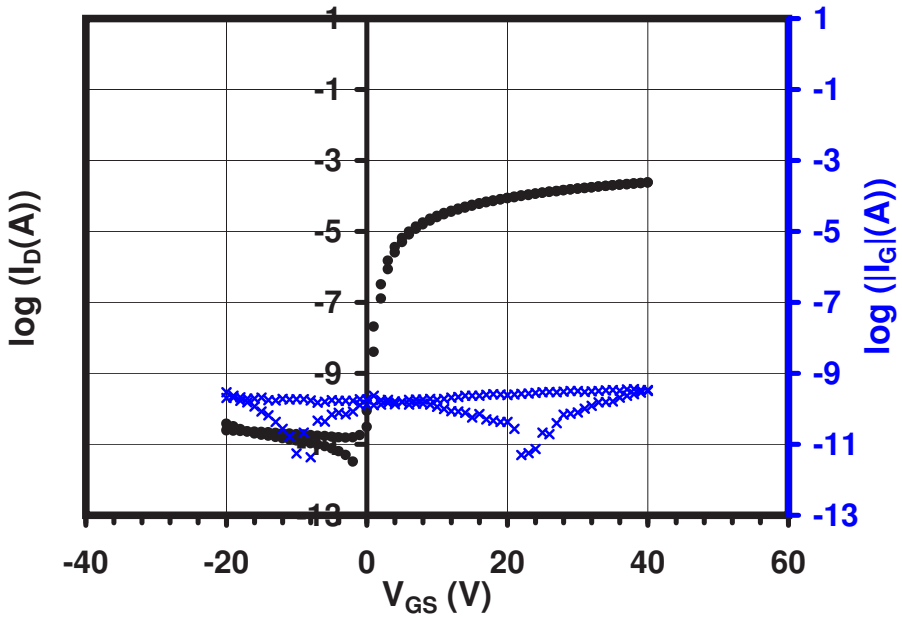

Figure 3.11: $log(I_D) - V_{GS}$ transfer curve for mobility extraction. $V_{DS} = 1$ V while V_{GS} is swept from -20 V $\leq V_{GS} \leq 40$ V. The device under test is a TFT composed of a ZTO channel layer ($\sim$50 nm) annealed at 400 °C in air, thermally grown SiO_2 gate insulator, and aluminum source/drain contacts; $W/L = 10$ with $L = 200$ μm.

[9]. These physically-based channel mobilities can be calculated by,

$$\mu_{INC}(V_{GS}) = \lim_{V_{DS}\to 0}\left[\frac{\frac{\partial G_D(V_{GS})}{\partial V_{GS}}}{\frac{W}{L}\cdot C_G}\right], \tag{3.3}$$

for incremental mobility, where G_D is the channel conductance given by I_D/V_{DS}, and

$$\mu_{AVE}(V_{GS}) = \lim_{V_{DS}\to 0}\left[\frac{G_D(V_{GS})}{\frac{W}{L}\cdot C_G\cdot(V_{GS}-V_{ON})}\right], \tag{3.4}$$

for average mobility [9].

Figure 3.12 shows these mobilities as extracted from Fig. 3.11. It should be noted that average mobility, μ_{AVE}, is best for circuit modeling, while incremental mobility, μ_{INC}, is best for device physics modeling.

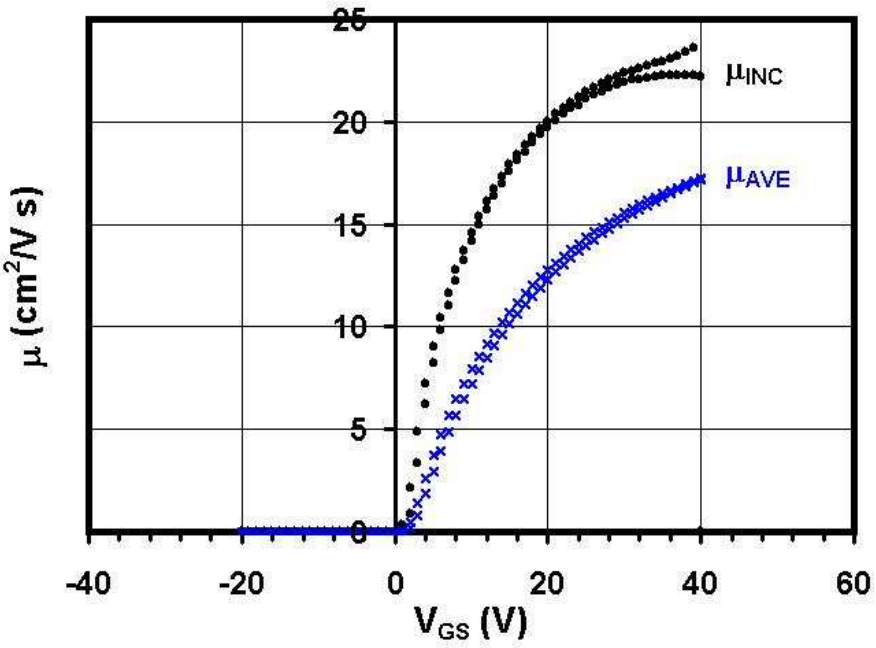

Figure 3.12: Mobility as a function of gate voltage. Data obtained from Fig. 3.11 is used to calculate both incremental (dots) and average (x's) mobility. The device under test is a TFT composed of a ZTO channel layer (∼50 nm) annealed at 400 °C in air, thermally grown SiO_2 gate insulator, and aluminum source/drain contacts; $W/L = 10$ with $L = 200$ μm.

3.7.3 Drain Current On-to-Off Ratio

The drain current on-to-off ratio (I_D^{ON-OFF}), shown in Fig. 3.13, is defined to be the ratio of drain to source current, I_D, of a user defined "on" point, to that of the "off" state as obtained from a TFT $log(I_D) - V_{GS}$ transfer curve at a large value of V_{DS} (i.e., 30 V). Normally, the transfer curve data is generated using the same sweep that is used for the mobility extraction (i.e., for this TFT -10 V $\leq V_{GS} \leq 40$ V), only the V_{DS} bias is increased, forcing the TFT into saturation. I_D^{ON-OFF} ratios are useful for assessing TFT switching capability and noise floor when designing circuits. Typically, I_D^{ON-OFF} ratios greater than 10^6 are considered acceptable.

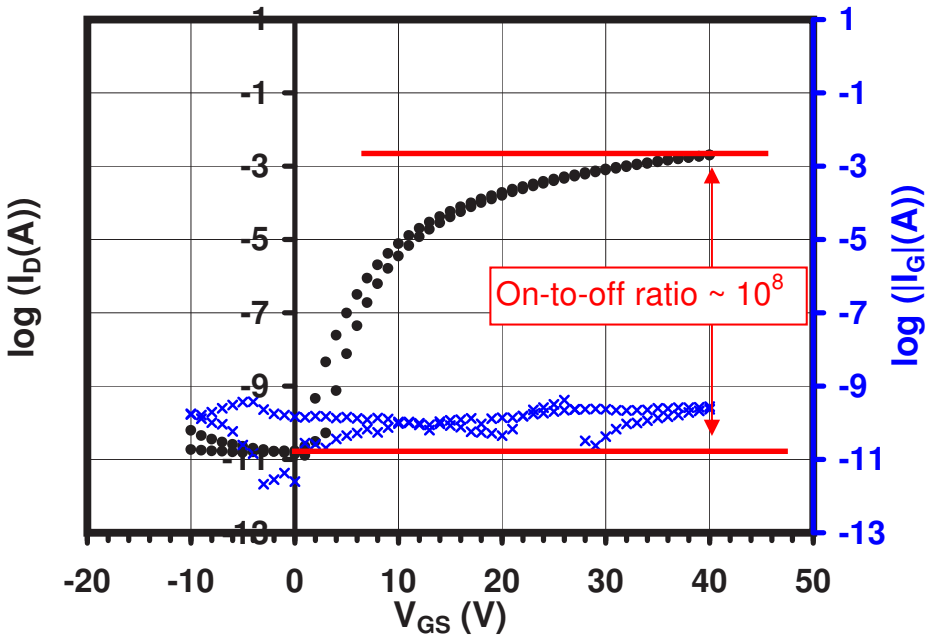

Figure 3.13: $log(I_D) - V_{GS}$ transfer curve for drain current on-to-off ratio extraction. V_{DS} = 30 V while V_{GS} is swept from -10 V $\leq V_{GS} \leq$ 40 V. The device under test is a TFT composed of a ZTO channel layer ($\sim$50 nm) annealed at 500 °C in air, thermally grown SiO_2 gate insulator, and aluminum source/drain contacts; $W/L = 10$ with $L = 200$ μm.

3.7.4 Operating Frequency

For ring oscillator, switching, or small-signal circuits the operating frequency is quite important. The operating frequency relates directly to the time delay of a TFT. In the case of a ring oscillator, the delay per stage (i.e., an inverter stage) previously defined in Chapter 2, can be rewritten as,

$$t_d = \frac{1}{2 \cdot n \cdot f}, \tag{3.5}$$

where n is the number of inverter stages and f is the output frequency of the ring oscillator. When reporting the performance of a ring oscillator, t_d is used for demonstrating TFT performance while output frequency demonstrates "real world" appli-

cation capability (e.g., noting that if the operating frequency is above 13.56 MHz, RF applications become possible).

Integrated circuits require low parasitics (see Section 3.8.1) and high mobility (see Section 3.7.2) to achieve a faster operating frequency, transient times, or switching speeds. Should the mobility be too low, or parasitics too high, then undesirably high power consumption or large bias voltages may be required to increase the operating frequency. Often, AOS researchers quote ring oscillator operating frequencies for benchamarking or material characterization [27]. However, note that with power consumption, applied biases, and parasitics involved, more than just the electrical performance (i.e., mobility) of the AOS channel material is being tested. Actually, with proper circuit layout (i.e., parasitics, number of stages in ring oscillator) and testing (i.e., applied bias, power) higher frequencies can be obtained with rather poor TFT mobility. Therefore, careful scrutiny is required when reviewing such claims of "AOS performance" via ring oscillator operating frequency.

3.7.5 Noise Margins and Inverter Voltage Transfer Characteristic

Noise margins are a measure of the insensitivity of an inverter to the exact value of the input voltage. Noise margin for a high input, NM_H, and noise margin for a low input, NM_L, are defined as

$$NM_H = V_{OH} - V_{IH}, \tag{3.6}$$

and

$$NM_L = V_{IL} - V_{OL}, \tag{3.7}$$

where V_{OH} is the inverter output high value, V_{OL} is the inverter output low value, V_{IL} is the maximum value that the input voltage can have while being interpreted by the inverter as representing a logic low (0), and V_{IH} is the minimum value that

the input voltage can have while being interpreted by the inverter as representing a logic high (1). These four values describe the inverter behavior and provide the voltage transfer characteristic (VTC) of the inverter. [23]. The VTC of an inverter can therefore be approximated and plotted as shown in Fig. 3.14. In a non-ideal VTC

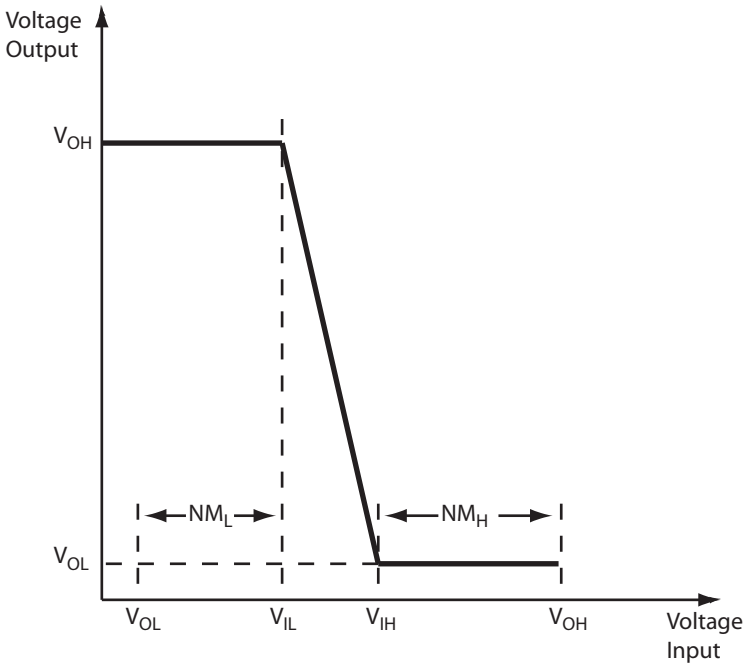

Figure 3.14: Idealized inverter voltage transfer characteristic (VTC) and noise margins (NM_L, NM_H) defined by the four parameters: V_{OH}, V_{OL}, V_{IL}, and V_{IH}. Note that V_{OH} and V_{OL} must be translated from the y-axis to the x-axis to make the noise margin measurements.

(i.e., a VTC such that the transitions are not abrupt, but rather rolls off), V_{IL} and V_{IH} are determined by where the slope of the transfer curve is equal to -1. As shown in Fig. 3.15, an ideal inverter VTC has equal noise margins. Therefore, the ideal inverter transition is centered at mid-rail (i.e., $V_{DD}/2$) with outputs as high as the high supply rail (i.e., V_{DD}) and as low as the low supply rail (i.e., ground). Inverter

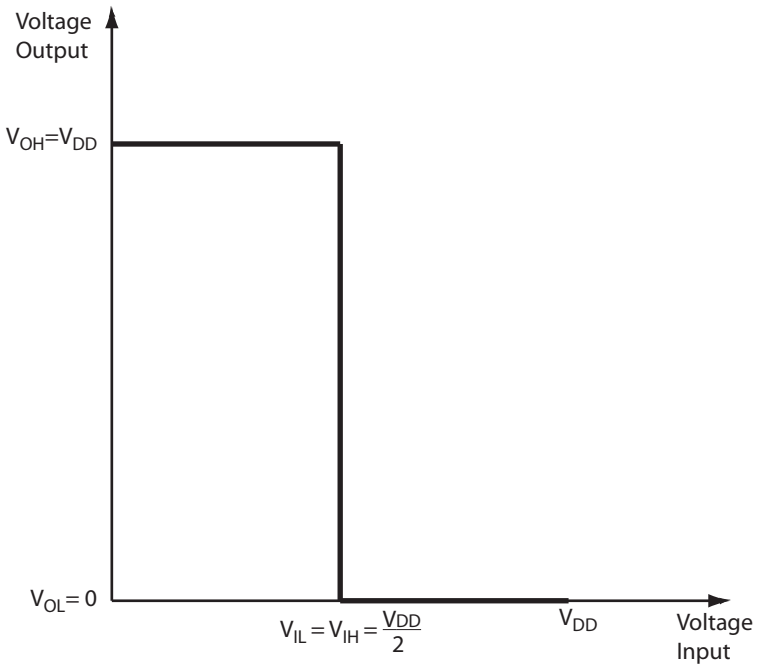

Figure 3.15: Ideal inverter voltage transfer characteristic (VTC) showing a centered transition about $V_{DD}/2$ and outputs ranging from ground (0) to V_{DD}.

characteristics are important since the inverter is the most basic building block for any digital circuit. No other logic gates can be created without an inverter.

3.8 Design and Simulation Considerations

This section discusses methods employed for device and circuit design and simulation.

3.8.1 Parasitics

Parasitics refer to unintentional resistive, capacitive, or inductive contributions which degrade the performance of an electronic device or circuit. Resistive parasitics impact both static DC and dynamic TFT testing testing characteristics (i.e., μ_{AVE}, μ_{INC}, V_{ON}, V_{TH}, I_D^{ON-OFF}). Capacitive and inductive parasitics are usually unimportant for static DC TFT testing characteristics. However, capacitive and inductive

parasitics are found to have a strong negative impact on dynamic TFT testing (i.e., time constants, switching times, and delay times).

For example, a parasitic capacitor, like the one shown in Fig. 3.16, is created though the overlap of the source/drain contact with the gate contact through the gate insulator. This is usually referred to as gate-source (or gate-drain) overlap. Ideally, the gate-source overlap would be zero so that there is no parasitic capacitance. In reality, through photolithography misalignment, over-etching, and other non-idealities, there is always gate-source overlap.

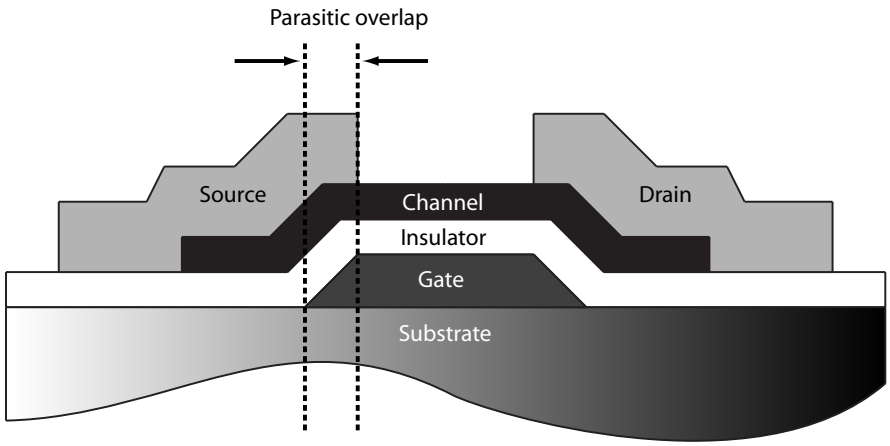

Figure 3.16: TFT cross-section illustrating that a parasitic capacitor is created though overlap of the source/drain contact with the gate contact across the gate insulator.

In addition to gate-source overlap, other common TFT parasitics include intrinsic channel capacitance, channel resistance, parasitic resistance with ITO traces, and parasitic capacitors with overlapping traces. All of these parasitics can be minimized through careful circuit layout and design. However, many times they cannot be eliminated. For example, if two traces must cross (gate layer and source/drain

layer) either the overlapping area can be minimized (i.e., narrow traces) or the interlayer dielectric can be made thicker to reduce the parasitic capacitance. The latter solution is preferred so as not to introduce greater parasitic resistance into the traces by narrowing them. However, adding a thicker dielectric layer adds complexity to the fabrication process.

3.8.2 Device and Circuit Modeling and Simulation

Modeling and simulation are important in determining the design of an integrated circuit prior to layout and processing. For this work, all modeling and simulation is based upon a sixth-order polynomial expression to define TFT *I-V* characteristics. This is referred to as Hoffman's closed form mobility polynomial solution [50]. Figure 3.17 is a simple schematic of a TFT structure, and includes the TFT dimensions and coordinate system used in the derivation of Hoffman's solution. Specifically, Hoffman's solution is derived by first examining the current density, J_n,

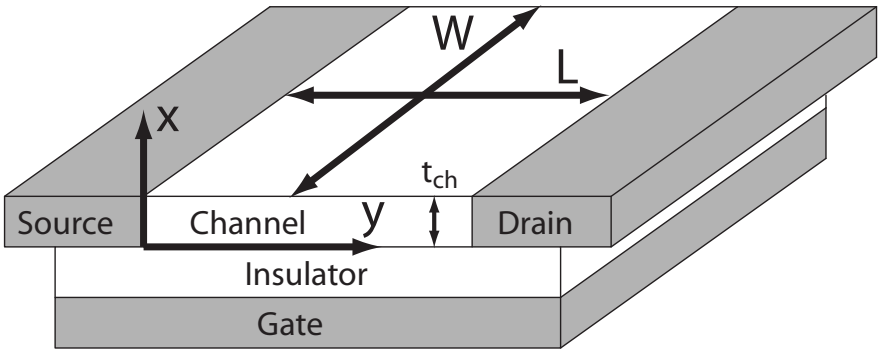

Figure 3.17: Simple schematic TFT structure including the TFT dimensions of channel width, W, length, L, and thickness, t_{ch}. Note the definition of the x, y coordinate system.

(assuming DC steady state throughout) and is given by,

$$J_n(x,y) = -q\mu(x,y)n(x,y)\frac{dV(y)}{dy}, \tag{3.8}$$

where q in the electron charge, and x,y correspond to the coordinates depicted in Fig. 3.17. For this analysis, it is assumed that the source electrode is grounded (i.e., $V \equiv 0$) and is located at $y = 0$. Using this assumption, Eq. 3.8 solves for the total electron current density, including both drift and diffusion [50]. Therefore, the TFT drain current, I_D, can be expressed as,

$$I_D = -W\int_0^{t_{ch}} J_n(x,y)dx, \tag{3.9}$$

where W is the channel width, t_{ch} is the channel thickness as shown in Fig. 3.17. Simplifying Eq. 3.9 with Eq. 3.8 leads to,

$$I_D = qW\frac{dV(y)}{dy}\int_0^{t_{ch}} \mu(x,y)n(x,y)dx. \tag{3.10}$$

Next, the gradual channel approximation is invoked, which states $\frac{dE_x}{dx} \gg \frac{dE_y}{dy}$ throughout the channel, where E_x and E_y are the x- and y-components of the channel electric field respectively. Also, the device must not be in the saturation regime of operation (see *Chapter 5: SCLC* for a detailed description of the requirements for saturation) because then the gradual channel approximation would be violated due to the high-field within the pinch-off region. Now, the electron density, $n(x,y)$, at a given location, y, along the channel is established by the electric field, E_x, induced by the gate-source voltage, V_{GS}. Therefore, the local channel sheet conductance is expressed as,

$$G_{SH}(y) = \int_0^{t_{ch}} q\mu(x,y)n(x,y)dx. \tag{3.11}$$

Equations 3.10 and 3.11 can be combined, yielding,

$$I_D = W\frac{dV(y)}{dy}G_{SH}(y). \tag{3.12}$$

The sheet conductance can be expressed as a function of either distance, y, or voltage, V, since the voltage is a single-valued monotonic function of distance. Thus, Eq. 3.12 can be rewritten as,

$$I_D = W\frac{dV}{dy}G_{SH}(V). \tag{3.13}$$

Next, multiplying Eq. 3.13 through by dy and integrating yields,

$$\int_0^L I_D dy = \int_0^{V_{DS}} WG_{SH}(V)dV. \tag{3.14}$$

Finally, solving Eq. 3.14 for I_D results in,

$$\begin{aligned} I_D &= \frac{W}{L}\int_0^{V_{DS}} G_{SH}(V)dV \\ &= \frac{W}{L}\int_0^{V_{DS}} \mu_{AVE}(V)Q_{IND}(V)dV \end{aligned}, \tag{3.15}$$

where Q_{IND} is the gate-source voltage-induced TFT channel charge per unit area. This solution assumes that all defects and non-idealities can be rolled into the mobility term and be expressed as a gate-source voltage dependent average mobility. Further simplification can be made with a new potential defined as,

$$V_{EFF}(y) \equiv V_{GS} - V_{ON} - V(y), \tag{3.16}$$

where V_{EFF} is the portion of V_{GS} that acts to induce mobile carriers (i.e., electrons if the TFT is n-type) at a given location, y. Now, Q_{IND} may be approximated as,

$$Q_{IND}(V_{EFF}) = C_{INS}V_{EFF}, \tag{3.17}$$

where C_{INS} is the gate capacitance density. With the substitution of V_{EFF} for V (Eq. 3.16) and Q_{IND} defined (Eq. 3.17), Eq. 3.15 can be rewritten as,

$$\begin{aligned} I_D &= \frac{W}{L}\int_{V_{GS}-V_{ON}-V_{DS}}^{V_{GS}-V_{ON}} G_{SH}(V_{EFF})dV_{EFF} \\ &= C_{INS}\frac{W}{L}\int_{V_{GS}-V_{ON}-V_{DS}}^{V_{GS}-V_{ON}} \mu_{AVE}(V_{EFF})V_{EFF}dV_{EFF} \end{aligned} \quad . \tag{3.18}$$

Previously, it was stated that this derivation is only valid if the TFT is not operating in saturation. However, if it is assumed that the TFT is a long-channel device and that the source-drain leakage current is negligible for $V_{GS} < V_{ON}$ (i.e., negligible off current), then Eq. 3.18 can be expanded to include all three modes of operation (i.e., off, pre-saturation, and saturation), expressed as,

$$I_D = \begin{cases} 0 \\ \quad \ldots V_{GS} \leq V_{ON} \\ C_{INS}\frac{W}{L}\int_{V_{GS}-V_{ON}-V_{DS}}^{V_{GS}-V_{ON}} \mu_{AVE}(V_{EFF})V_{EFF}dV_{EFF} \\ \quad \ldots V_{DS} \leq V_{GS}-V_{ON} \\ C_{INS}\frac{W}{L}\int_{0}^{V_{GS}-V_{ON}} \mu_{AVE}(V_{EFF})V_{EFF}dV_{EFF} \\ \quad \ldots V_{DS} > V_{GS}-V_{ON} \end{cases} \quad . \tag{3.19}$$

Note that $\mu_{AVE}(V_{EFF})$ is a shifted data set of the $\mu_{AVE}(V_{VGS})$ data set by a $-V_{ON}$ term, meaning $\mu_{AVE}(V_{EFF}) = \mu_{AVE}(V_{GS}-V_{ON}-V) \approx \mu_{AVE}(V_{GS}-V_{ON})$, where V is negligible since $V_{DS} \sim 0$ for the I_D-V_{GS} transfer curve measurement used to extract μ_{AVE}, and $V \leq V_{DS}$ throughout the channel. What remains of the closed-form solution is a $\mu_{AVE}(V_{EFF})$ relationship to drive Eq. 3.19. It is found that an nth-order polynomial curve fit can be used to reasonably estimate $\mu_{AVE}(V_{EFF})$, and

can be written in the form,

$$\mu_{AVE}(V_{EFF}) \cong \begin{cases} 0 & \ldots V_{EFF} \leq 0 \\ \sum_{i=0}^{n} c_i \left[V_{EFF}\right]^i & \ldots V_{EFF} > 0 \end{cases}, \tag{3.20}$$

where c_i are polynomial coefficients. Therefore, the simplification and integration of Eq. 3.19 results in the closed-form expression,

$$I_D = \begin{cases} 0 \\ \quad \ldots V_{GS} \leq V_{ON} \\ C_{INS}\frac{W}{L}\sum_{i=0}^{n}\left(\frac{c_i}{i+2}\left[\left(V_{GS}-V_{ON}\right)^{i+2} - \left(V_{GS}-V_{ON}-V_{DS}\right)^{i+2}\right]\right) \\ \quad \ldots V_{DS} \leq V_{GS}-V_{ON} \\ C_{INS}\frac{W}{L}\sum_{i=0}^{n}\left(\frac{c_i}{i+2}\left(V_{GS}-V_{ON}\right)^{i+2}\right) \\ \quad \ldots V_{DS} > V_{GS}-V_{ON} \end{cases}. \tag{3.21}$$

This closed-form solution is written as a sixth-order polynomial expression which is embedded into a TFT simulation model using VerilogA code (see Appendix B. VerilogA Code), and is used within the *Cadence, version 5.1.0,* environment. In terms of the model structure, the dependent variable μ_{AVE} can be expressed as,

$$\mu_{AVE}(V_{EFF}\colon c_0, c_1, c_2, c_3, c_4, c_5, c_6), \tag{3.22}$$

where V_{EFF} is the independent variable and $c_0 \ldots c_6$ are model parameters.

Table 3.1 lists the seventeen simulation model parameters used to define a TFT. They are separated into two classifications, geometric parameters and physical parameters. Geometric parameters include channel width, W, channel length, L, gate-source/drain overlap, $GSD_{OVERLAP}$, channel-source/drain overlap, $CSD_{OVERLAP}$,

gate insulator thickness, t_{OX}, and channel thickness, t_{CH}. Physical parameters include the turn-on voltage, V_{ON}, relative dielectric constant, K_{OX}, channel resistivity, $\rho_{CHANNEL}$, contact resistivity, $\rho_{CONTACT}$, and average mobility, μ_{AVE}, which is defined by the polynomial coefficients, $c_0, \ldots, c_6$, as per Eq. 3.22. Figure 3.18 illustrates $GSD_{OVERLAP}$ and $CSD_{OVERLAP}$. Using these parameters and Eq. 3.21, a static,

Table 3.1: Simulation model parameters for TFT definition.

Geometric model parameters	**Symbol**	**Units**
Channel width	W	Meters
Channel length	L	”
Gate-source/drain overlap	$GSD_{OVERLAP}$	”
Channel-source/drain overlap	$CSD_{OVERLAP}$	”
Gate insulator thickness	t_{OX}	”
Channel thickness	t_{CH}	”
Physical model parameters	**Symbol**	**Units**
Turn-on voltage	V_{ON}	Volts
Relative dielectric constant	K_{OX}	—
Zero-order mobility polynomial coefficient	c_0	—
First-order ”	c_1	—
Second-order ”	c_2	—
Third-order ”	c_3	—
Fourth-order ”	c_4	—
Fifth-order ”	c_5	—
Sixth-order ”	c_6	—
Channel resistivity	$\rho_{CHANNEL}$	Ω·cm
Contact resistivity	$\rho_{CONTACT}$	Ω·cm^2

ideal (i.e., no parasitics) DC model emerges, as specified by,

$$I_D(V_{GS}, V_{DS}\colon W, L, t_{OX}, V_{ON}, K_{OX}, c_0, \ldots, c_6), \tag{3.23}$$

where the dependent variable, I_D, depends on the independent variables, V_{GS} and V_{DS}, and the remaining model parameters. Extending the DC model by including TFT capacitive parasitics associated with $GSD_{OVERLAP}$ creates a dynamic model of

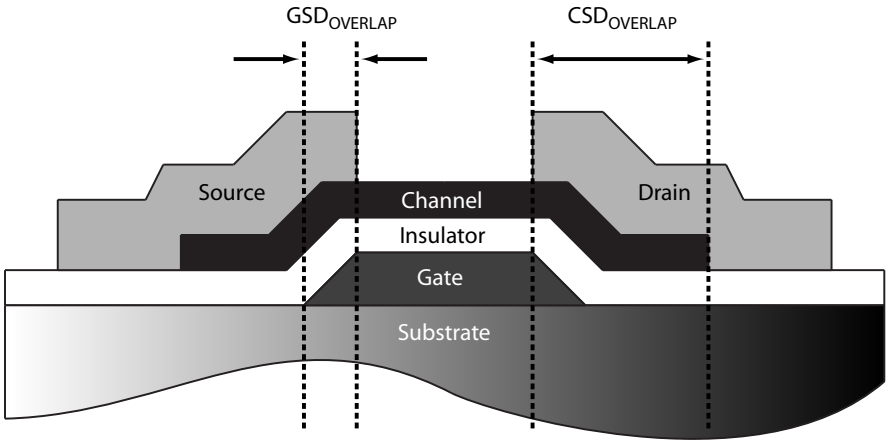

Figure 3.18: Schematic TFT structure illustrating the overlaps $GSD_{OVERLAP}$ and $CSD_{OVERLAP}$ used for parasitic capacitance and contact resistance calculations respectively.

the form,

$$I_D(V_{GS}, V_{DS}\colon W, L, t_{OX}, V_{ON}, K_{OX}, GSD_{OVERLAP}, c_0, \ldots, c_6). \tag{3.24}$$

Note that the dynamic model only includes TFT capacitive parasitics, and neglects resistive parasitics. This is relevant because time constants are calculated from the resistance and capacitive multiplicative product, RC. For example, the cutoff frequency, f_C, of an RC circuit is related to the time constant, τ, by,

$$f_C = \frac{1}{2\pi\tau} = \frac{1}{2\pi RC}, \tag{3.25}$$

where R is the circuit resistance, and C is the circuit capacitance. One neglected resistive parasitic is the contact resistance from the channel to the source/drain contacts. This parasitic resistance is equal to $\frac{\rho_{CONTACT}}{W \cdot CSD_{OVERLAP}}$. Another neglected resistive parasitic is the intrinsic channel resistance equal to $\frac{\rho_{CHANNEL} \cdot L}{W \cdot t_{CH}}$. Non-quasistatic

TFT behavior has also not been accounted for in this version of the model [31]. Therefore, of the seventeen model parameters, those associated with parasitic calculations not currently included in the model. Specifically, $CSD_{OVERLAP}$, $\rho_{CHANNEL}$, $\rho_{CONTACT}$, and t_{CH} are not used. Therefore the dynamic model described should be considered preliminary.

Parasitics not associated with a TFT (i.e., caused by interconnect and contact dimensions and placement) include are interconnect resistance, inductance, and capacitance. These interconnect parasitics can be included in simulation by the addition of discrete elements. Parasitic resistance is likely to be significant when TCOs are used as interconnects. Parasitic capacitance may be of relevance, depending on the interconnect geometry. Parasitic inductance is expected to be of no significance at the relatively low frequencies of interest.

Of the thirteen model parameters actively used (i.e., seventeen total model parameters less the four neglected) within the TFT model, t_{OX}, K_{OX}, V_{ON}, and the μ_{AVE} polynomial coefficients (i.e., $c_0, \ldots, c_6$), are interdependent. This means that one of the parameters cannot be changed without altering the others (e.g., the polynomial fit mobility extraction is dependent upon $V_{EFF} = V_{GS} - V_{ON}$ so that $c_0, \ldots, c_6$ all depend on V_{ON}). Three of the four neglected model parameters, specifically $\rho_{CHANNEL}$, $\rho_{CONTACT}$, and t_{CH}, are also interdependent and, therefore, should be hard-coded. Ten of these interdependent model parameters, with the exception of V_{ON}, makeup the process transconductance parameter, K', which is preferred by circuit designers, and is defined as,

$$K' = \mu_{AVE} \cdot C_{INS}, \tag{3.26}$$

where $C_{INS} = \dfrac{\epsilon_o K_{OX}}{t_{OX}}$, and ϵ_o is the permittivity of free space. Since t_{OX}, K_{OX}, and the μ_{AVE} polynomial coefficients are interdependent, they are hard-coded directly into the VerilogA code (see Appendix B. VerilogA Code). Hard-coding these model

parameters into the VerilogA model also means that each TFT that uses that specific model all have the same values of μ_{AVE}, V_{ON}, and gate insulator parameters. Should variation in these parameters between TFTs be desired, then an additional model (i.e., a copy of the model with different values of t_{OX}, K_{OX}, V_{ON}, and the μ_{AVE} polynomial coefficients $c_0, \ldots, c_6$) must be created. There is no limit to the number of different models that can be created. In fact, each TFT within the schematic can have its own model with individualized hard-coded model parameters.

All of the other model parameters used, specifically W, L, $GSD_{OVERLAP}$, and $CSD_{OVERLAP}$, are independent. They are referred to as "user-defined" parameters. A user-defined parameter can be individually selected for each TFT in a schematic. To set these parameters in a schematic, view the "properties" of each TFT within the Cadence "schematic" view, and insert the values as desired. Note that the units used for these geometrical parameters are meters, not microns.

The procedure for TFT modeling in this work is as follows. First, as shown in Fig. 3.19, a TFT is fabricated, usually by shadow-masking of channels and source/drain contacts onto a thermal silicon dioxide using a blanket (unpatterned) silicon substrate as the gate.

Second, as shown in Fig. 3.20, this TFT is then measured and an I_D - V_{GS} transfer curve is plotted, followed by a corresponding average mobility (μ_{AVE}) curve.

Third, as shown in Fig. 3.21, a sixth-order polynomial is fit to the mobility data. Note that the x-axis is now given by $V_{GS} - V_{ON}$ (i.e., V_{EFF}). Depending on the sign of the highest order polynomial term, the expression either diverges to infinity or decays to zero for extrapolated values of V_{GS} beyond that of the fitted data. For this reason, the polynomial should always be fit over a greater range of V_{GS} that ever experienced by the final device or circuit in operation. This is accomplished by either testing the TFT over a wider range of V_{GS} or by augmenting the data set with well-behaved, extrapolated data points. Data augmentation is acceptable only

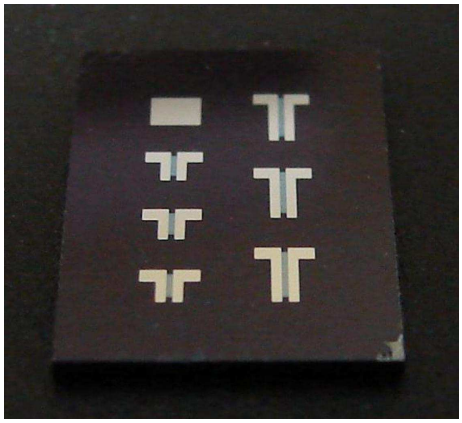

Figure 3.19: TFT fabricated using shadow-masking to pattern AOS channels and source/drain layers contacts onto a thermal silicon dioxide using a blanket (unpatterned) silicon substrate as the gate; $W/L = 10$ with $L = 200$ μm.

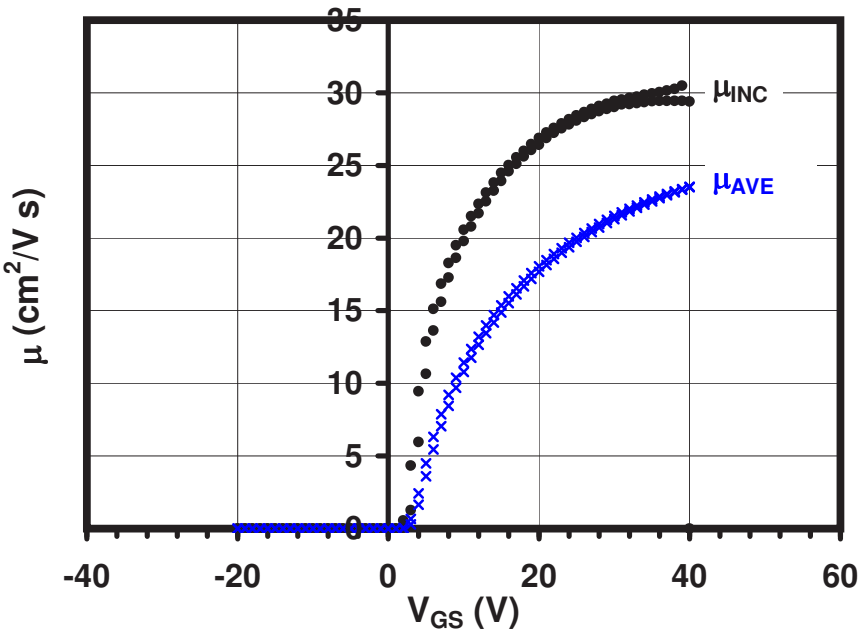

Figure 3.20: Extracted mobility as a function of V_{GS} from a TFT fabricated using shadow-masking to pattern AOS channels and source/drain layers contacts onto a thermal silicon dioxide using a blanket (unpatterned) silicon substrate as the gate; $W/L = 10$ with $L = 200$ μm.

if the simulation does not push into the region of augmented data points (in this example, data was added in the range 40 V $< V_{GS} - V_{ON} <$ 100 V). Restricting the simulation to the domain of the un-augmented region of V_{GS} produces the most accurate simulation. The equation that corresponds to the polynomial fit shown in Fig. 3.21 and written out according to the form given in Eq. 3.20 is,

$$\begin{aligned} \mu_{AVE}(V_{EFF}) &= -5.15 \times 10^{-11}(V_{EFF})^6 + 2.99 \times 10^{-8}(V_{EFF})^5 \\ &\quad -6.45 \times 10^{-6}(V_{EFF})^4 + 7.11 \times 10^{-4}(V_{EFF})^3 \\ &\quad -4.47 \times 10^{-2}(V_{EFF})^2 + 1.59(V_{EFF})^1 \\ &\quad -1.86 \times 10^{-1}(V_{EFF}) \end{aligned} \quad . \tag{3.27}$$

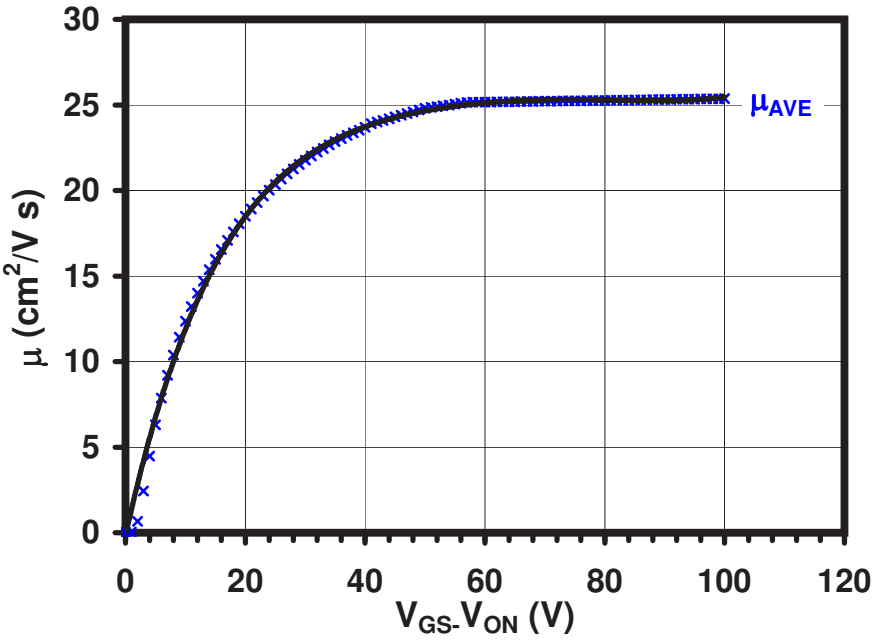

Figure 3.21: Sixth-order polynomial fit to the extracted average mobility versus $V_{GS} - V_{ON}$ (i.e., V_{EFF} as in Eq. 3.27). Note that the experimental mobility data obtained between $0 \leq V_{GS} \leq 40$ V is augmented by extrapolation of well-behaved data points out to 100 V.

Fourth, as shown in Fig. 3.22 the sixth-order polynomial constants obtained from the mobility extraction, V_{ON}, and gate insulator information are added to a segment of VerilogA code (shown in *Appendix B: VerilogA Code*) corresponding to the closed-form mathematical solution of Hoffman [50].

```
//Eric Sundholm (6/4/2009) CURRENTLY USING
//090604F2
c0 = -1.86E-1;
c1 = 1.59E0;
c2 = -4.47E-2;
c3 = 7.11E-4;
c4 = -6.45E-6;
c5 = 2.99E-8;
c6 = -5.15E-11;
von = 1;
tox = 0.1E-6;  /*dielectric thickness, 100nm */
Ko = 3.9;
```

Figure 3.22: Segment of VerilogA code showing the hard-coded parameters which define the TFT model.

Fifth, as shown in Fig. 3.23, the accuracy of the hard-coded parameters (i.e., t_{OX}, K_{OX}, V_{ON}, and the μ_{AVE} polynomial coefficients $c_0, \ldots, c_6$) is tested by simulating the fabricated TFT (from step 1) and applying an appropriate test (i.e., I_D-V_{GS} transfer curve using the same V_{DS} value and V_{GS} range as was used for the average mobility extraction in step 2 above). A schematic can be drawn using SPICE modeled DC voltage sources for V_{DS} and V_{GS}. The value of V_{DS} is known and constant, while the value of V_{GS} should be set as a variable name (e.g. "vgs"). Since a $I_D - V_{GS}$ transfer curve is a DC test, the parameter $GSD_{OVERLAP}$ used in calculating capacitive parasitics is not relevant. However, a correct TFT channel W and L must be input.

Sixth, as shown in Fig. 3.24, a simulated $log(I_D) - V_{GS}$ transfer curve can then be generated and compared to the measured $log(I_D) - V_{GS}$ transfer curve.

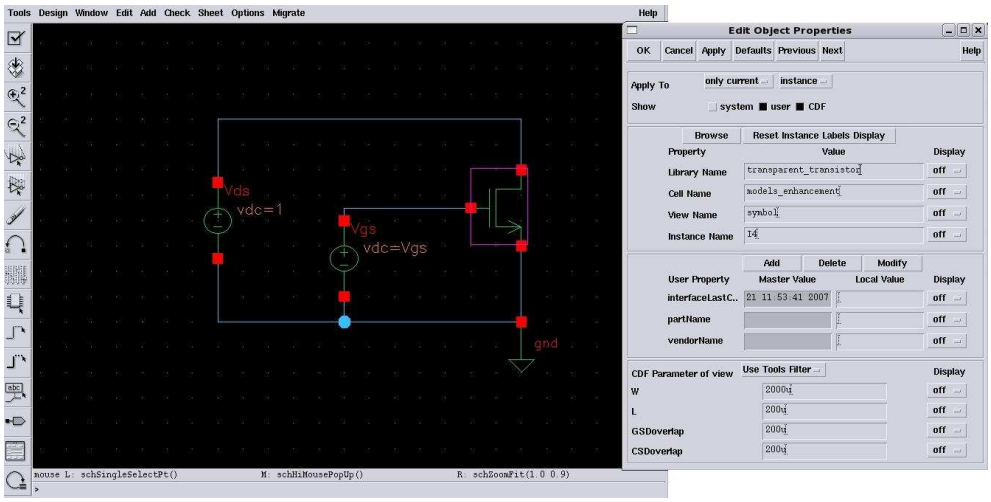

Figure 3.23: The user-defined parameters W, L, $GSD_{OVERLAP}$, $CSD_{OVERLAP}$, and test parameters of the TFT (from step 1) and appropriate transfer curve (i.e., the I_D-V_{GS} transfer curve using the same V_{DS} value and V_{GS} range as is used for the average mobility extraction in step 2 above) are input into Cadence.

To generate the simulated I_D-V_{GS} transfer curve the following steps must be taken. Begin by entering the analog environment window by clicking the "Tools" pull-down menu, followed by "Analog Environment" from within the schematic "cellview" in Cadence. Next, select the simulator called "spectre" which is able to interpret both VerilogA modeled devices (i.e., TFTs) and SPICE modeled devices (i.e., voltage sources, current sources, resistors, capacitors, inductors, ground references, etc.). This is accomplished within the analog environment window by clicking the "Setup" pull-down menu, followed by "Simulator/Directory/Host...", and then selecting "spectre" on the pull-down menu indicating the simulator type. Next, import and arbitrarily set (i.e., any value so that a DC convergence may be found) variables from the schematic by clicking the "Variables" drop-down menu followed by "Copy From Cellview". This includes the independent transfer curve variable "vgs" mentioned above. To set the imported variables arbitrary value, double click the variable in the variable list and input a value in the pop-up window. Next, set the simulation test parameters by clicking the "Analysis" pull-down menu, followed by "Choose...".

Select a DC test from the bullet list, and then set the "Sweep Variable" to "Design Variable". Then, when the "Select Design Variable" button is pressed, a windowed list of the imported schematic variables from the a previous step will appear. Select the variable corresponding to V_{GS} (e.g. "vgs"). The "Sweep Range", "Sweep Type", and "Step Size" can all match the same I_D-V_{GS} transfer curve inputs used to test the fabricated TFT from step one (e.g., -20 V $< V_{GS} <$ 40 V). Next, select outputs to be saved or plotted by clicking the "Outputs" pull-down menu and selecting either "To Be Saved..." or "To Be Plotted..." respectively, followed by "Select on Schematic". Clicking on a node (i.e., wire) selects that node's voltage as an output. Clicking on a device port (e.g., the TFT drain port) selects that port's current (e.g., the TFT drain current). Finally, run the simulation by clicking either the traffic light button, or clicking the "Simulation" pull-down menu, followed by "Netlist and Run". Simulated output can be saved as a comma delimited (CSV) file to be easily compared to the CSV file created by the semiconductor parameter analyzer (SPA) which generated the measured I_D-V_{GS} transfer curve data. If a good match between simulated and measured transfer curves is obtained, then circuit design and simulation can commence.

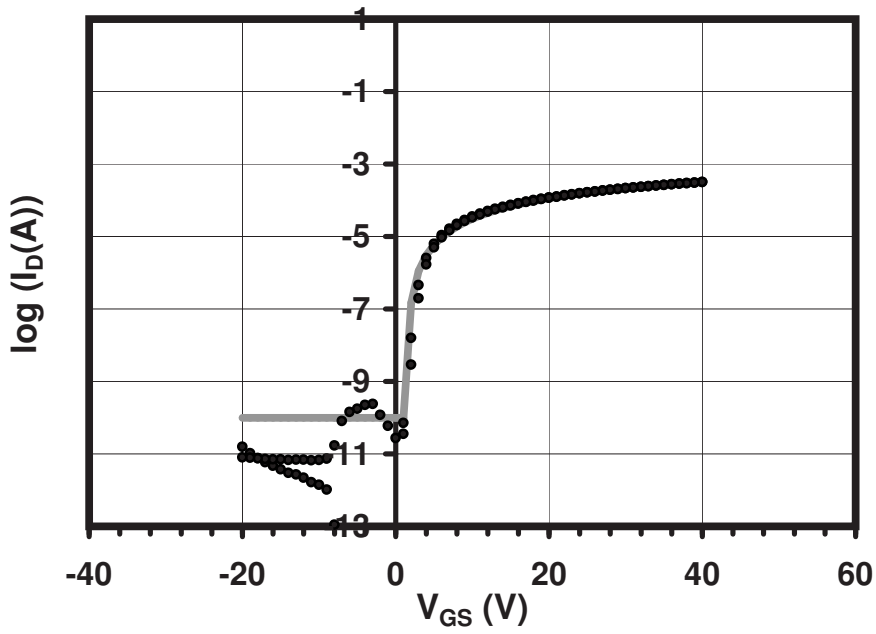

Figure 3.24: Simulated $log(I_D - V_{GS}$ data (grey solid) and measured $log(I_D - V_{GS}$ data (dots) are compared. The agreement between the measured and simulated DC data sets is considered to be quite good. Note that the simulated TFT off current is programmed to 1×10^{-10} A.

4. AOS CIRCUIT REALIZATION AND DESIGN

This chapter presents experimental results related to the realization of a transparent ring oscillator, as well as a discussion of the performance of discrete devices and inverters fabricated on the same substrate. Additionally, preliminary circuit design of a high-performance ring oscillator and an RFID tag are overviewed.

4.1 Ring Oscillator

A 3-stage ring oscillator utilizing bootstrapped inverters is fabricated in order to demonstrate MHz circuit operation using AOS channel layer TFTs. MHz operation leads to the possibility of radio frequency applications, such as RFID tags.

4.1.1 Fabrication

The ring oscillator circuit is fabricated using bottom-gate structure TTFTs and IGO as the AOS channel layer. The circuit is also fabricated using non-transparent TFTs by substituting an opaque source/drain contact metal, i.e., aluminum. The basic fabrication process (see *Appendix A: Process Flow* for detailed process steps) for this single-channel TTFT circuit utilizes four photolithography masks and ten main steps. First, a glass substrate pre-coated with ∼150 nm ITO (from Delta Technologies) is cleaned and dehydrated. Second, the ITO is patterned using photolithography and HCl wet etching to form the gate contacts and traces. Third, 100 nm of PECVD SiO_2 is deposited as the gate insulator. Fourth, ∼50 nm of IGO is deposited as the AOS channel material using RF magnetron sputtering. Fifth, IGO is patterned using photolithography and HCl wet etching. Sixth, the IGO is annealed at 500 °C in air. Seventh, the gate insulator is patterned for vias using photolithography and HF wet etching. Eighth, photo-pattering for lift-off is performed. Ninth, ∼100 nm ITO (or aluminum) is deposited using RF magnetron sputtering (or evaporation). Tenth,

the ITO (or aluminum) is patterned using lift-off to form source/drain contacts and traces.

The channel material is deposited immediately following the gate insulator deposition in an attempt to maintain a pristine channel-insulator interface. Should any via be etched in the gate insulator prior to channel deposition, then chemicals from the photo-processing (e.g., photoresist, acetone, isopropanol alcohol, water, developer, or HMDS) may contaminate the channel-insulator interface. This contamination can lead to electron trapping, causing hysteresis in I-V curves or other electrical non-idealities.

The layout divides the substrate into four quadrants of duplicate devices/circuits, but with varying dimensions. The quadrants differ from each other by the TFT channel length, L, and the parasitic gate-source/drain overlap, $GSD_{OVERLAP}$. Quadrant I has $L = 10$ μm and $GSD_{OVERLAP} = 5$ μm. Quadrants II and IV are identical with $L = 2$ μm and $GSD_{OVERLAP} = 2$ μm. Quadrant III has $L = 5$ μm and $GSD_{OVERLAP} = 5$ μm.

Quadrant II and IV, having the shortest channel lengths and smallest parasitic capacitances, results in low TFT yield due to difficulties associated with source/drain liftoff and source/drain-to-gate alignment. Although using a minimal $GSD_{OVERLAP}$ has the potential to improve the frequency performance of the ring oscillator, processing such devices proved problematic.

The most successful circuits are fabricated in quadrant III, with $L = 5$ μm and $GSD_{OVERLAP} = 5$ μm. Therefore, the results discussed below are all obtained from quadrant IV.

4.1.2 Results: Discrete Devices

Processed in parallel with the ring oscillator circuit are arrays of discrete devices for characterization. Included in these arrays are groups of TFTs of the same dimensions as the TFTs used within the ring oscillator. Figure 4.1 is a representative

$log(I_D) - V_{GS}$ transfer curve of an IGO TFT. The turn-on voltage is slightly negative, as expected, due to a predictable negative V_{ON} shift arising from the channel photo-patterning process. The shadow masked devices were optimized for $V_{ON} = 0$, and, therefore, the photopatterned devices have $V_{ON} \leq 0$.

Of particular interest is the poor performance of the gate insulator. As seen in Fig. 4.1, the gate current, I_G, tracks with the drain current, I_D. This is characteristic of a leaky insulator with pinholes or other major defects. Refer to Chapter 6 for a complete dielectric material assessment.

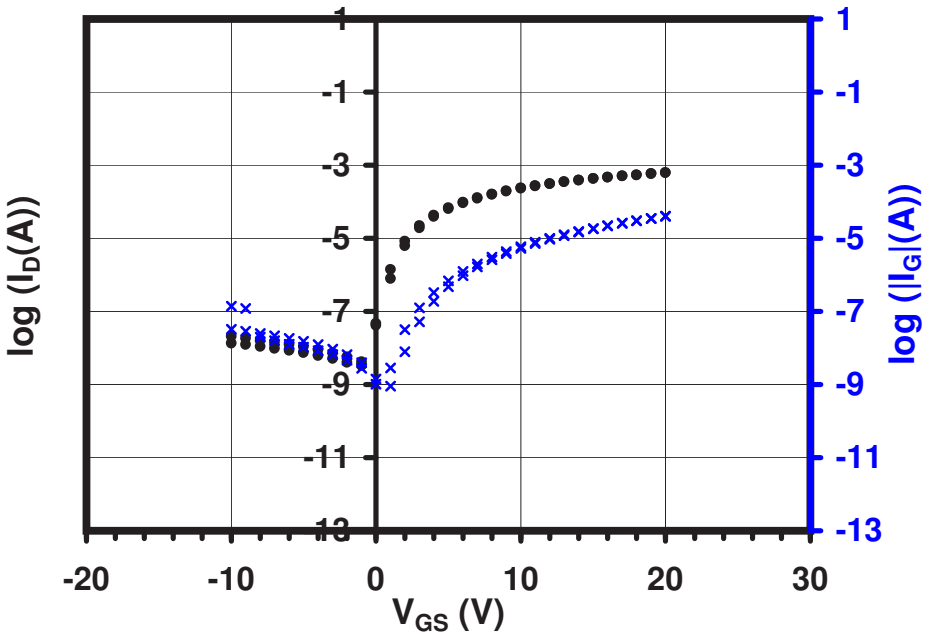

Figure 4.1: $log(I_D) - V_{GS}$ transfer curve for mobility and V_{ON} extraction. $V_{DS} = 1$ V while V_{GS} is swept from -10 V $\leq V_{GS} \leq 20$ V. The device under test is a TFT composed of a IGO channel layer ($\sim$50 nm) annealed at 500 °C in air, PECVD SiO_2 gate insulator (100 nm), ITO gate contact (150 nm), and aluminum source/drain contacts ($\sim$100 nm); $W/L = 40$ with $L = 5$ μm. Note that the gate leakage, I_G, is rather poor and tracks with the drain current, I_D.

Figure 4.2 shows average mobility, μ_{AVE}, and incremental mobility, μ_{INC} as extracted from Fig. 4.1. The mobility most critical to circuit performance, μ_{AVE}, is adequate at ~21 cm^2/Vs at $V_{GS} = 20$ V.

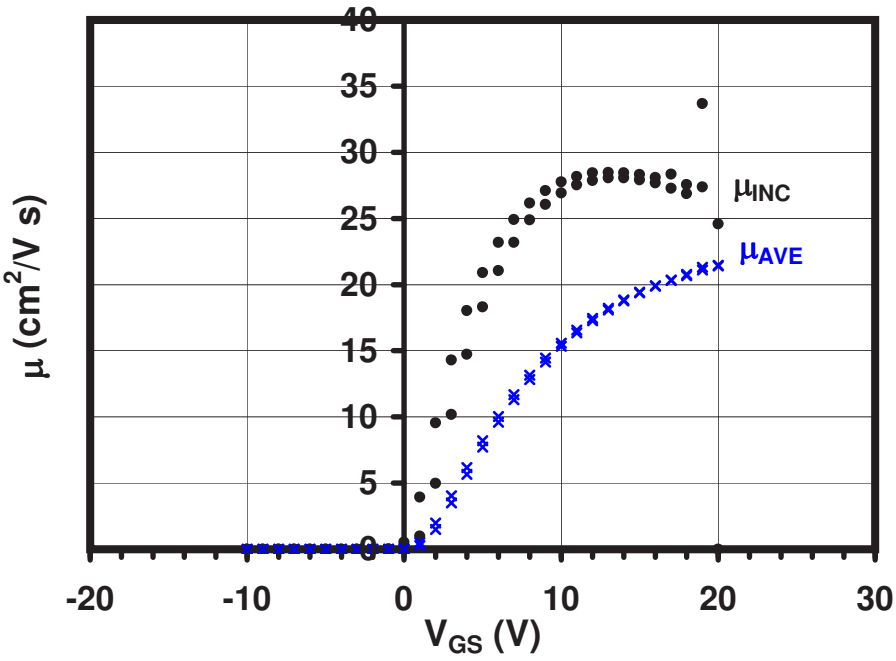

Figure 4.2: Mobility as a function of gate voltage. Data obtained from Fig. 4.1 is used to calculate both incremental (dots) and average (x's) mobility. The device under test is a TFT composed of a IGO channel layer (~50 nm) annealed at 500 °C in air, PECVD SiO_2 gate insulator (100 nm), ITO gate contact (150 nm), and aluminum source/drain contacts (~100 nm); $W/L = 40$ with $L = 5$ μm.

4.1.3 Results: Bootstrapped Inverter

Bootstrapped inverters are utilized for each inverting stage and the buffer stage of the ring oscillator. Like the discrete TFTs, the bootstrapped inverters are processed in parallel with the ring oscillator for diagnostic characterization. Figure 4.3 is a

schematic of the bootstrapped inverter fabricated, displaying the sizing of the TFTs in μm and the value of the bootstrapping capacitor (0.5 pF).

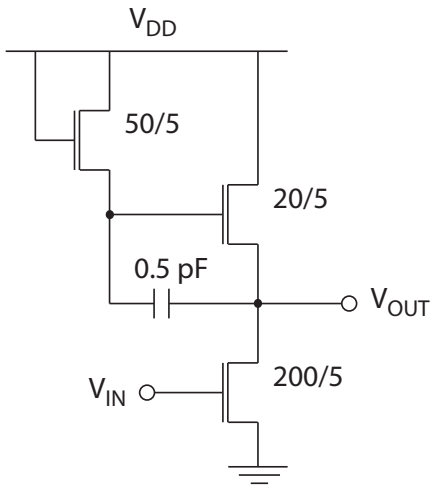

Figure 4.3: Schematic of an n-type only inverter utilizing a bootstrapped design. Transistor sizing is specified in μm. Note that the gate and output terminals of the load transistor are capacitively coupled, creating a dynamic load. $GSD_{OVERLAP} = 5$ μm, $CSD_{OVERLAP} = 10$ μm for the TFTs used in this circuit.

Figure 4.4 is a plot of the time domain response of the bootstrapped inverter of Fig. 4.3. A 29.5 V peak-to-peak 20 Hz triangular wave is applied to the input of the bootstrapped inverter. The bootstrapped inverter is powered by a 30 V supply, i.e., $V_{DD} = 30$ V. The input waveform could not be driven to a 30 V peak-to-peak signal, as desired, due to losses in the external circuit used to amplify the function generator triangle waveform. The same 30 V supply is used to power both the input waveform and the bootstrapped inverter. The asymmetrical nature of the bootstrapped inverter output waveform is characteristic of an enhancement-mode loaded inverter.

Figure 4.5 is a plot of the bootstrapped inverter voltage transfer characteristic (VTC) (lines) as extracted from Fig. 4.4. Since Fig. 4.4 contains data from > 3 oscillating periods, Fig. 4.5 displays several complete sweeps (i.e., forward and backward

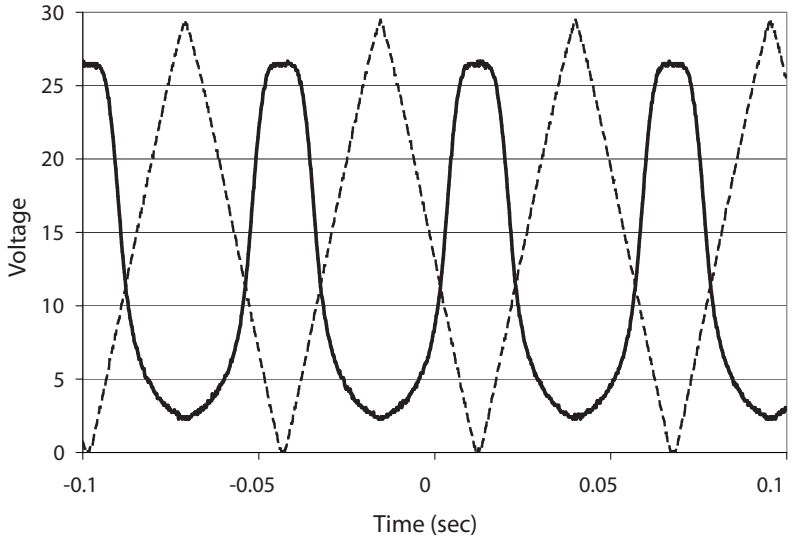

Figure 4.4: Time domain response of an IGO TFT bootstrapped inverter fabricated using the architecture specified in Fig. 4.3. The input is a 29.5 V peak-to-peak 20 Hz triangular voltage waveform; V_{DD} = 30 V, V_{IN-Max} = 29.5 V, V_{IN-Min} = 0 V, $V_{OUT-Max}$ = 26.5 V, $V_{OUT-Min}$ = 2.5 V. The asymmetrical output waveform is characteristic of an enhancement-mode loaded inverter.

input voltage sweeps). The hysteresis of the bootstrapped inverter is shown to be minimal.

Also included in Fig. 4.5 is a gain plot of the bootstrapped inverter (dots). Gain is calculated using the absolute value of the derivative of the VTC output. The average maximum gain is ∼2.6. As discussed in Chapter 2, the gain per stage required for a three stage ring oscillator to maintain oscillation is 2. With the variance in the average maximum gain taken into account, it is found that this bootstrapped inverter's gain is dangerously close to the minimum.

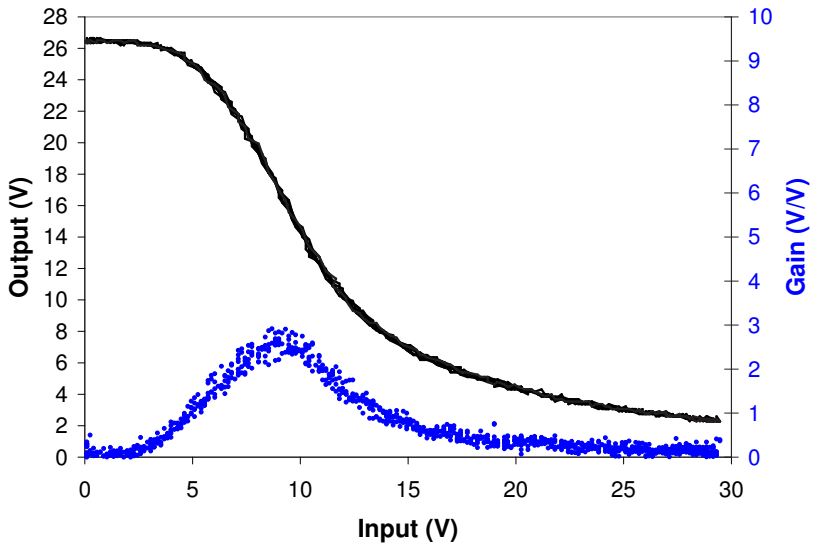

Figure 4.5: Voltage transfer characteristic (VTC) (lines) of an IGO TFT bootstrapped inverter, extracted from Fig. 4.4. Hysteresis is minimal, as evident by the ≥ 3 sweeps (i.e., > 3 periods of the input waveform) displayed in the output waveform. The gain of the bootstrapped inverter (dots) is calculated from the absolute value of the derivative of the VTC output. The average maximum gain is ∼2.6. Note that the variance in the maximum gain results in values that approach the minimum gain per stage needed to sustain oscillation in a three-stage ring oscillator (i.e., 2) as discussed in Chapter 2.

Figure 4.6 is a reproduction of the VTC shown in Fig. 4.5 with the noise margins and appropriate parameters labeled. V_{IL} and V_{IH} are determined by where the slope of the transfer curve is equal to -1. For calculation of noise margins, the output values of V_{OL} and V_{OH} are translated onto the x-axis from the y-axis. The noise margins are asymmetrical, i.e., $NM_L \approx 2.50$ V and $NM_H \approx 12.66$ V. Again, this asymmetry is typical of an enhancement-mode loaded inverter.

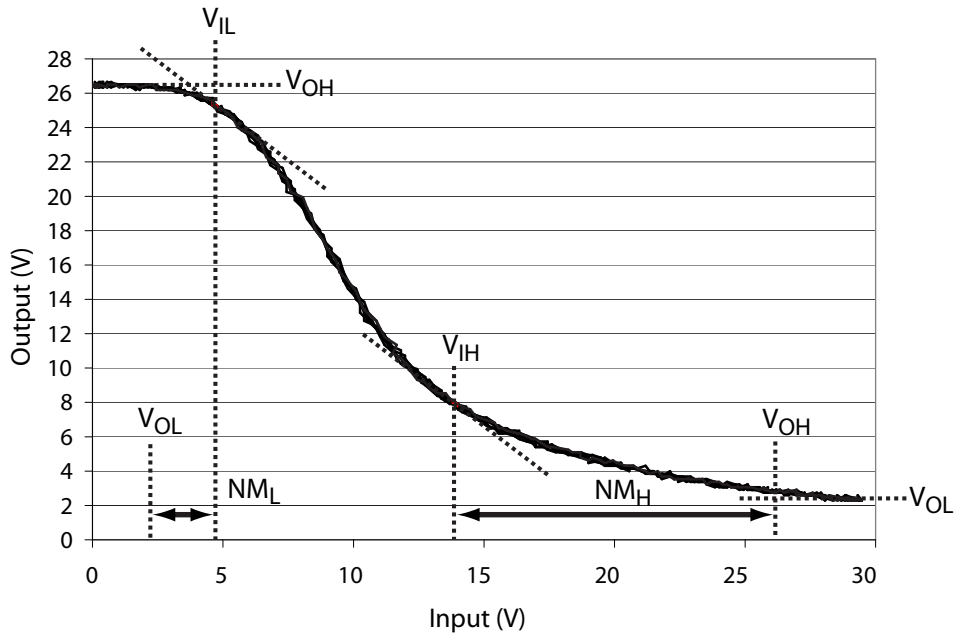

Figure 4.6: Voltage transfer characteristic (VTC), noise margins, and appropriate parameters of the IGO TFT bootstrapped inverter extracted from Fig. 4.4; $V_{IL} \approx 4.78$ V, $V_{IH} \approx 14.00$ V, $V_{OL} \approx 2.28$ V, $V_{OH} \approx 26.66$ V, $NM_L \approx 2.50$ V, $NM_H \approx 12.66$ V. V_{IL} and V_{IH} are determined by where the slope of the transfer curve is equal to -1.

4.1.4 Results: Ring Oscillator

The bootstrapped inverters of Fig. 4.3 are linked together into a three stage (i.e., three inverters) ring in order to produce a ring oscillator. The output is buffered

by a fourth identical inverter to shield the ring oscillator from loading during testing (as discussed in Chapter 2). Figure 4.7 is a top-down photograph of the ring oscillator, showing all three inverting stages and the buffered output. The same sizing

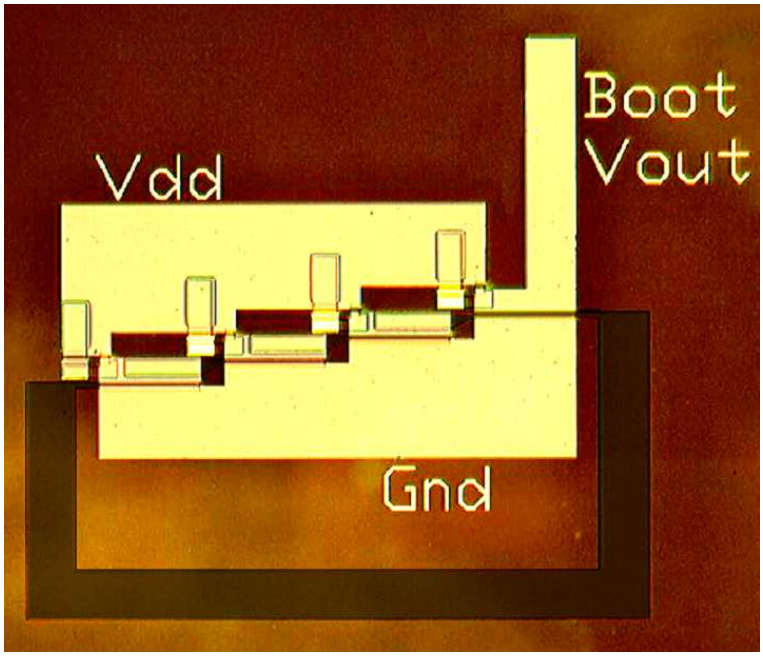

Figure 4.7: Top-down photograph of an IGO TFT buffered three-stage ring oscillator. At the time of its fabrication, this was the fastest AOS ring oscillator reported.

and geometry is used in ring oscillator bootstrapped inverters as in discrete bootstrapped inverters of Fig. 4.3. Therefore, $L = 5$ μm, $GSD_{OVERLAP} = 5$ μm, and $CSD_{OVERLAP} = 10$ μm.

Figure 4.8 is the ring oscillator output in the time domain. The ring oscillator is powered with a 30 V supply (i.e., $V_{DD} = 30$ V) and oscillates at 2.16 MHz. The time delay per stage, t_d, is 77 ns. The output swing, V_{OUT-pp}, is 1.35 V. The ring oscillator behaves normally, with output swing and output frequency being directly

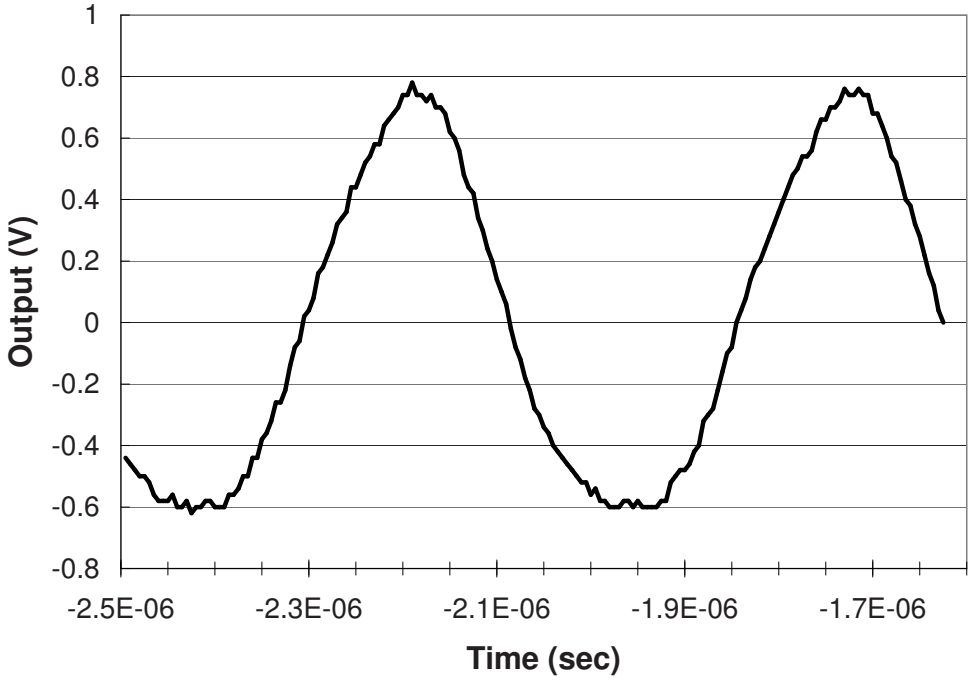

Figure 4.8: Output waveform of an IGO TFT buffered three-stage ring oscillator measured from the device pictured in Fig. 4.7. The circuit is powered with a 30 V supply (i.e., $V_{DD} = 30$ for each inverter stage, including the buffer); $f = 2.16$ MHz, $V_{OUT-pp} = 1.35$ V, $t_d = 77$ ns, $L = 5$ μm, $GSD_{OVERLAP} = 5$ μm, $CSD_{OVERLAP} = 10$ μm. At the time of its fabrication, this was the fastest AOS ring oscillator reported.

proportional to the power supply. The output waveform appears to be much more symmetrical than that of the discrete bootstrapped inverters.

While the discrete TFTs and bootstrapped inverters obtained near 100% yield, the ring oscillators had a near-0% yield. This discrepancy is attributed to the leaky gate insulator (Fig. 4.1), and the fact that the gain-per-stage requirement is so close to the actual gain (Fig. 4.5).

At the time of its fabrication (July 2007), this was the fastest oxide electronics ring oscillator reported, with an output frequency of 2.16 MHz, and $t_d = 77$ ns. However, as discussed in Chapter 2, in December 2007, Sun et al. [27] published a paper using ZnO TFTs to fabricate a ring oscillator with a reported $t_d = 75$ ns. Sun et al.'s power supply is similar, 32 V. Sun et al.'s reported time delay per stage is from a 7-stage ring oscillator which, due to the number of stages, should oscillate at approximately half the frequency as a 3-stage ring oscillator. The 7-stage ring oscillator oscillated at 1.04 MHz. As discussed in Chapter 2, any performance improvements compared to that reported herein are likely due to having less parasitic overlap capacitance, $GSD_{OVERLAP}$. Sun et al.'s 7-stage ring oscillator has $GSD_{OVERLAP} = 2$ μm, whereas the 3-stage ring oscillator reported herein has $GSD_{OVERLAP} = 5$ μm. A direct comparison between the work reported herein and that reported by Sun et al., in which the power supply, time delay per stage, and output frequency (relative to the number of stages) are all approximately equal, reveals that the performance of these two ring oscillator designs are basically equivalent. While Sun et al. has lesser parasitic overlap capacitance, the work reported herein employs a bootstrapped design, thus resulting is similar performance.

4.2 Circuit Design: High-Performance Ring Oscillator

In an effort to create a ring oscillator with a > 10 MHz output frequency, a cross-coupled bootstrapped design was created, with the help of Peter Kurahashi. Figure 4.9 is a schematic of an individual cross-coupled inverter stage using a bootstrapped

design. Notice that the individual inverter stage is actually two parallel inverters that bootstrap one another. Therefore, two ring oscillators in parallel are created when these inverter stages are linked to form a ring oscillator. Each of the two parallel inverters within a single inverter stage must be in opposite states (high or low) in order for the dynamic loading effect of the bootstrapping to work.

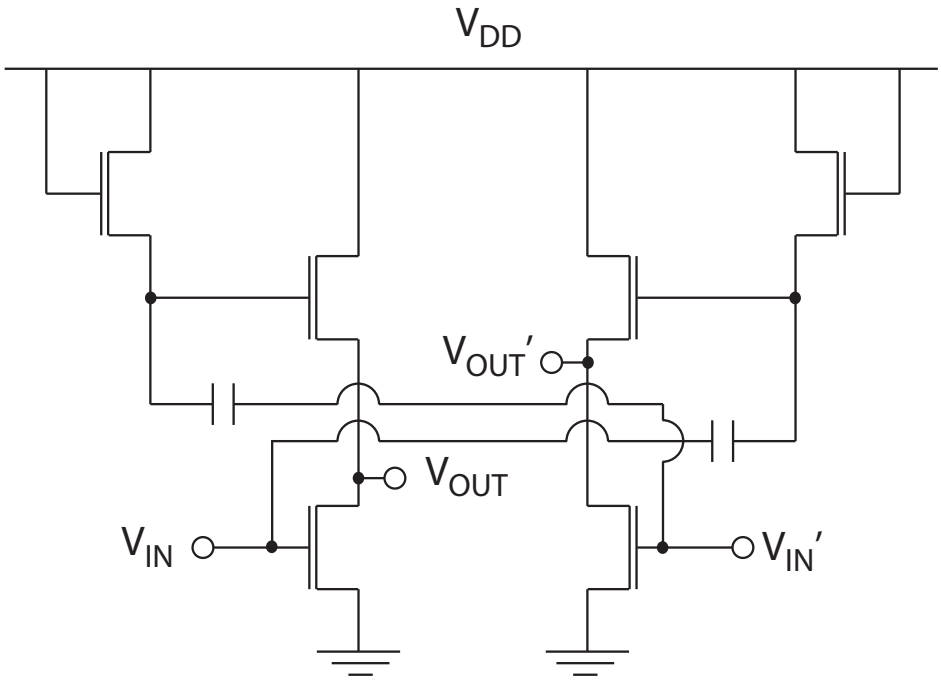

Figure 4.9: Schematic of a high-performance bootstrapped inverter utilizing both the bootstrapped and cross-coupled designs. Note that the inverter is actually two parallel inverters that bootstrap one another.

With respect to the ring oscillator design fabricated in this work, additional improvements applied to the new high-performance ring oscillator includes, the addition of more stages to decrease the gain per stage requirement, and the addition of a long buffer/amplifier inverter chain at the output to increase the output swing. To avoid loading the ring oscillator, thereby decreasing the output frequency, the

buffer/amplifer inverter chain uses very small devices (low parasitic capacitance) attached directly to the ring oscillator output. The chain then steps up the device size progressively to obtain the output swing desired. Figure 4.10 is a top-down layout view (Cadence) of the ring oscillator (5-stage) and buffer/amplifier inverter chain.

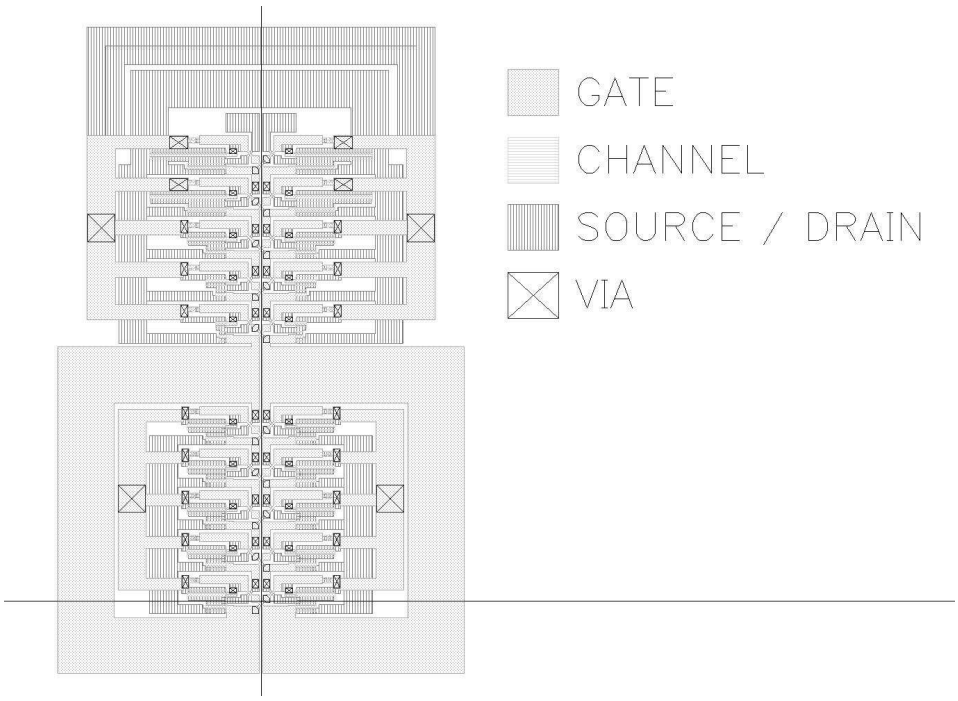

Figure 4.10: Layout of a high-performance ring oscillator utilizing both bootstrapped and cross-coupled designs. Note that the circuit consists of two main blocks, the ring oscillator (top) and buffer/amplifier inverter chain for output boosting (bottom).

Although the preliminary design of the high-performance ring oscillator has been completed, fabrication of this circuit was not attempted, for two main reasons. First, the dimensions required for high speed operation prove to be very difficult to obtain by manual alignment during photolithography patterning. For high yield processing via liftoff or wet etch patterning and manual alignment of small overlaps

between layers, 15 μm minimum dimensions (e.g., channel length, L) with 5 μm minimum overlaps (e.g., gate-source/drain overlap, $GSD_{OVERLAP}$) is suggested. Second, the maximum frequency of operation of a TFT is approximated by the unity-gain frequency,

$$f_T \approx \frac{\mu V}{2\pi L^2}, \tag{4.1}$$

where, for a TFT, μ is the mobility, V is the drain-source voltage, and L is the channel length [31]. Therefore the maximum theoretical frequency with 15 μm dimensions, and a 10 V power supply is $\sim$7 MHz. Should the channel length shrink to 2 μm and the power supply be increased to 30 V, then the maximum theoretical frequency becomes $\sim$1.2 GHz. However, this calculation does not include parasitics (e.g., overlap capacitance, trace resistance, channel capacitance, and channel resistance). See Chapter 3 for a discussion of parasitics. Without specifying these parasitics, it is difficult to accurately predict the actual maximum frequency of a device or circuit.

4.3 Circuit Design: RFID Tag

Motivated by to the RFID tag paper of Cantatore et al., as discussed in Chapter 2 [39], an AOS *transparent* RFID tag was designed, again with the help of Peter Kurahashi.

Figure 4.11 is a schematic illustrating the basic operation of a capacitively-coupled RFID tag. Capacitive coupling is chosen instead of the more common inductive coupling due to the lack of availability of a low resistance transparent inductor. The basic operation of this circuit is as follows. The power supply is located in the reader and, through the capacitively coupled antenna, transfers RF power to the RFID tag. The RFID tag contains a rectifier so that the incident RF power can be converted to DC power for use within the code generator. The code generator also modulates the rectifier, producing a coded signal that uses the RF power as a carrier

wave. Once the RF wave and modulated code return to the reader, a demodulator extracts the code.

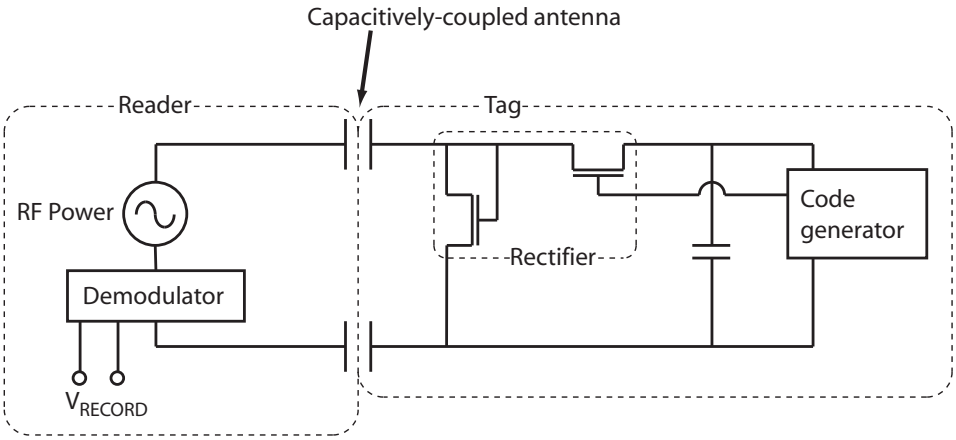

Figure 4.11: Schematic of a capacitively-coupled RFID tag and reader.

As illustrated in Fig. 4.12, the code generator operation can be broken down into five main parts, a data array, synchronization block, power on reset block, ring oscillator, and rectifier/modulator block.

The code generating data array is a grid of TFTs with hard coded data bits (i.e., 1's or 0's) placed on their drain contacts. The data bits are accessed by clock-controlled shift registers for both the column and row indexing. Each shift register contains one SR latch (i.e., a set/reset flip-flop) for each row/column. The data array of Fig. 4.12 is a 16 bit array.

Figure 4.13 is the simulated output from the 16 bit array. The top plot shows the output of the row indexing shift register. The middle plot shows the output of the column indexing shift register. The column indexing is performed four times slower than the row indexing to allow for individual indexing of any single bit. The

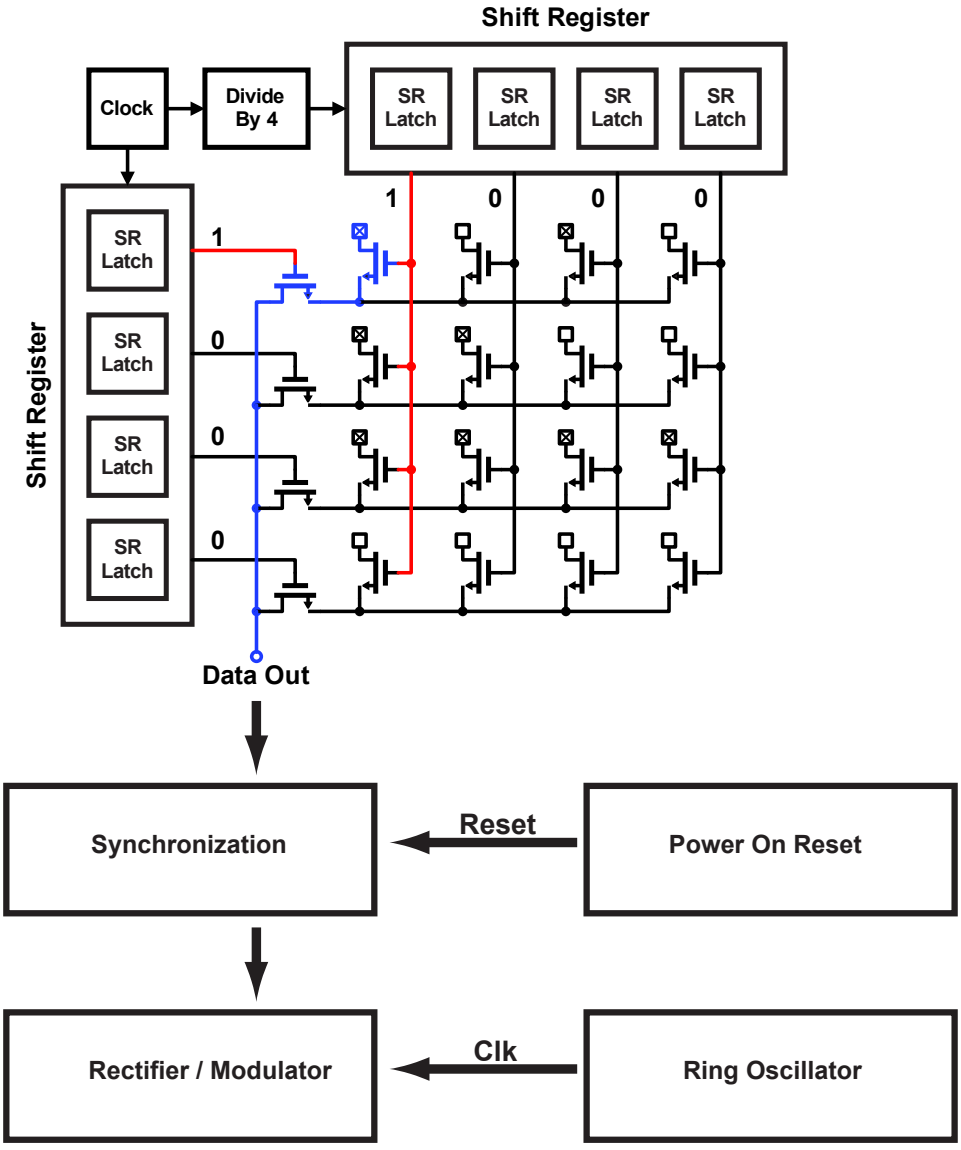

Figure 4.12: Schematic of a 16 bit RFID tag code generator.

bottom plot is the final generated code output, showing the combination of the row and column indexing, as well as the hard-coded data bits.

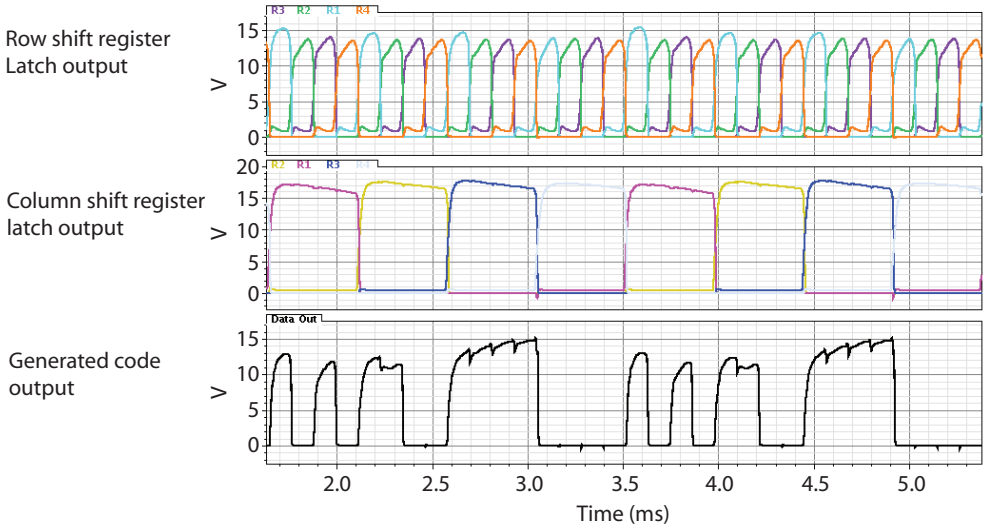

Figure 4.13: Simulated output of a 16 bit RFID tag code generator.

The synchronization block serves to synchronize the data from the 16 bit array to the RF carrier wave. The power on reset block serves to reset all the SR latches and data back to zero. The ring oscillator provides the clock signal for all signal processing. The rectifier/modulator block is the same rectifier that is used for RF-to-DC power conversion, as well as for inputting the 16 bit coded signal onto the RF carrier wave that is shown in Fig. 4.11.

The major difference between the organic TFT-based and the AOS TFT-based RFID tag, besides the channel material, involves the core circuit design approach. The organic TFT circuit uses conventional CMOS-derived designs and modifies them to work with p-type only organic TFTs. In contrast, the AOS TFT circuit was designed from scratch, using new n-type only designs which achieve better electrical

performance while using less power. Figure 4.14 is an example schematic and simulated waveforms of a bootstrapped SR latch used within the row/column indexing shift registers of the code generator. The additional transistors (grey) act to decrease the supply current. The disadvantage of using these additional TFTs is that the switching speed of the latch is reduced.

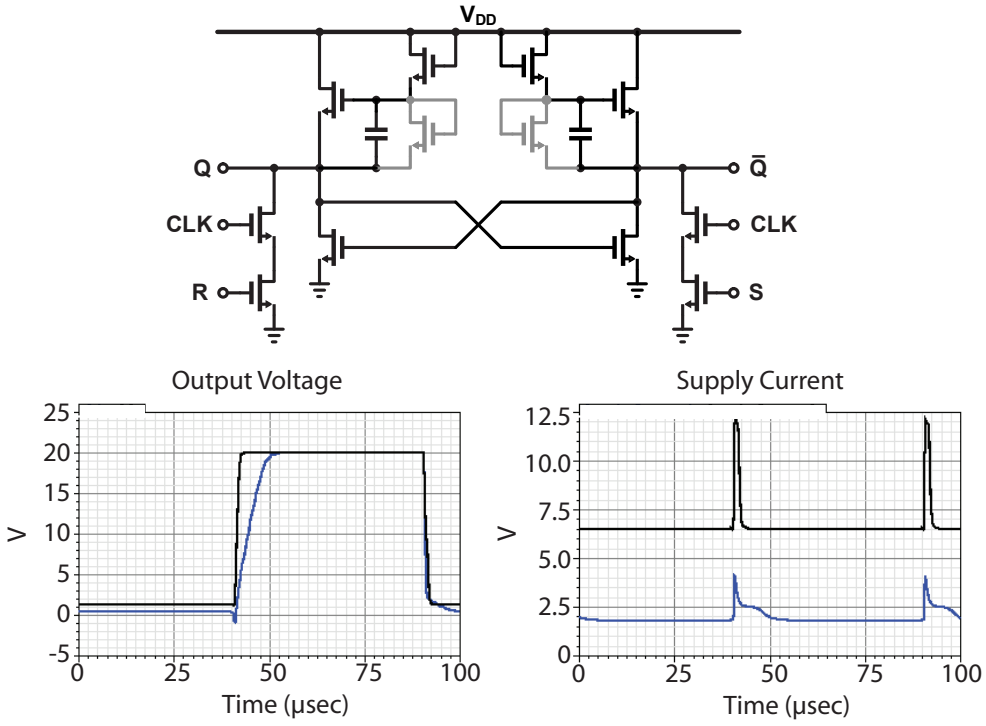

Figure 4.14: Schematic and simulated output of a SR latch. Note that the additional transistors (grey) dramatically reduce the supply current, but at a cost of reduced switching speed.

Table 4.1 is a direct comparison between the measured performance of the organic TFT-based RFID tag and the simulated performance of the AOS TFT-based RFID tag. The AOS TFT-based RFID tag, compared to the organic TFT-based RFID tag, operates with five times less power consumed and at least one order of

magnitude faster. This performance gain is possible despite the larger minimum feature size of the AOS TFT-based RFID tag. However, the number of data bits transmitted by the AOS TFT-based RFID tag is four times less. It should be noted that the power consumption does not directly scale with the number of data bits transmitted.

Table 4.1: Comparison of measured organic TFT-based RFID tag and simulated AOS TFT-based RFID tag performance.

Channel material	**Organic**	**AOS**
Min. feature size	4 μm	10 μm
# Transistors	60 per latch	12 per latch
Power consumption	5 μA at 60 V 300 μW	$\sim$3 μA at 20 V 60 μW
Read distance	"Close proximity"	Unknown
Data bits	64	16
Output frequency	150 bits/sec	$\sim$1-5 Kbits/sec

The circuit design of the AOS TFT-based RFID tag is currently $\sim$50% finished. The design of the flip-flops, code generator, and oscillator components are complete. Components yet to be designed include the RF front end (i.e., the rectifier/modulator), the return-to-zero constant power encoder, and the startup circuit (i.e., the latch reset).

5. SPACE-CHARGE-LIMITED-CURRENT MEASUREMENTS OF THIN-FILM TRANSISTORS

This chapter discusses of the use of space-charge-limited-current measurements of thin-film transistors as a transistor characterization tool. The discussion includes the necessary space-charge-limited current and transistor background information, as well as recommendations for test setup and results interpretation.

5.1 Introduction

A recent study [51] has reported the use of two-terminal (floating gate) space-charge-limited-current (SCLC) measurments of indium gallium zinc oxide (IGZO) thin-film transistors (TFTs) for the assessment of the band tail state properties of the IGZO semiconductor layer. Furthermore, Pete Erslev, University of Oregon, has attempted to extend these measurements by performing three-terminal measurements as a function of temperature. The goal of the undertaking described in this chapter is to extend this work in order to develop a simple and effective means of performing SCLC measurements using three-terminal TFT structures in order to correlate physical SCLC parameters - equilibrium carrier concentration (n_{co}), band tail state density (N_0), total trap density (N_t), characteristic trap energy (E_T), and characteristic trap temperature (T_t) - to TFT device properties - V_{ON}, V_{TH}, μ_{INC}, μ_{AVE}, hysteresis, and drain current on-to-off ratio [51]. Typically, a SCLC measurement is performed using a two-terminal resistive structure (i.e., a semiconductor layer with two ohmic contacts) and not with a three-terminal field-effect transistor (FET) device. The following discussion is an assessment of the viability of several possible SCLC measurement methods using different TFT configurations.

The following discussion exclusively assumes the use of an n-channel TFT.

5.2 SCLC Background

Space-charge-limited current (SCLC) occurs when injected carriers (electrons, for the situations considered herein) create a space-charge region which reduces the electric field near the injecting contact, thereby limiting further electron injection [52]. When the injected electron concentration is larger than the equilibrium concentration in the semiconductor, n, then space-charge effects become relevant [53]. Thus, SCLC is a dominant current transport mechanism only when efficient injection is possible.

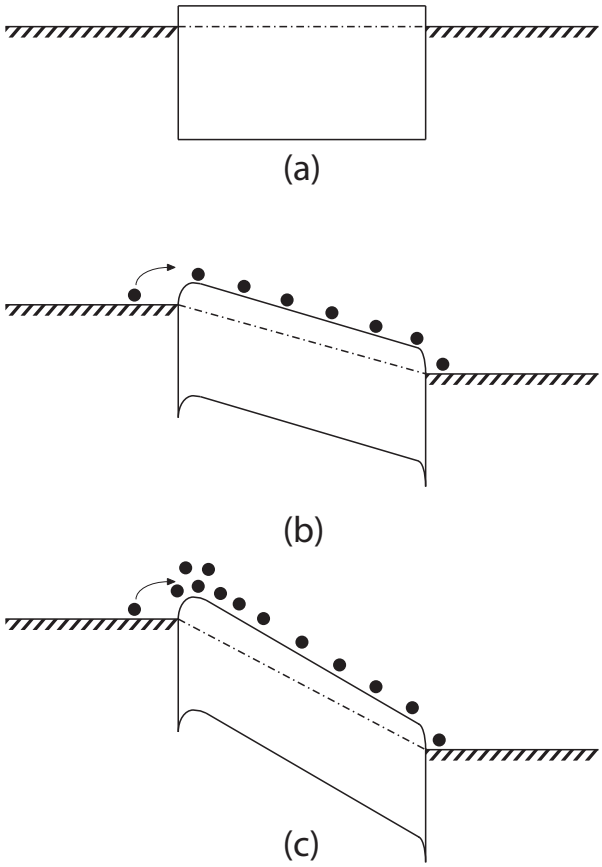

Figure 5.1: Energy band diagram of a two-terminal semiconductor structure with ohmic contacts. (a) The equilibrium situation. (b) Under a modest applied field such that electron injection occurs. (c) Under a larger applied field such that the current is space-charge limited.

Figure 5.1 shows several energy band diagrams for an ideal semiconductor free of defects or traps which could inhibit current flow. Figure 5.1(a) shows the equilibrium case. Notice that the electron injection barrier is quite small, which is for obtaining efficient electron injection. A modest rate of electron injection is indicated in Fig. 5.1(b). This case corresponds to ohmic conduction, prior to the onset of SCLC. Finally, Fig. 5.1(c) illustrates the SCLC situation in which the space charge associated with a high rate of electron injection leads to a suppression of further electron injection because of the repulsive electric field associated with the space charge.

Trap-free, SCLC flow, such as that illustrated in Fig. 5.1 is a highly idealized situation. In practice, real semiconductors have traps. Thus, a realistic SCLC model will include the effects of trapping [54]. However, first consider an ideal, trap-free SCLC model in the low-field mobility regime, which is given by,

$$J = \frac{9\varepsilon_S \mu V^2}{8L^3}, \tag{5.1}$$

where J is the current density, V is the applied voltage, μ is the mobility, L is the sample length in the direction of current flow, and ε_S is the dielectric permittivity of the semiconductor [53, 55]. Equation 5.1 shows that ideal-theory SCLC is characterized by the current density of current being proportional to the voltage to the power of two (i.e., $I \propto V^2$). If the power is found to be greater than two in the actual measurement of a real device, then this deviation is attributed to traps [54]. A material with an exponential trap distribution, such as an amorphous oxide semiconductor (AOS), as suggested by Hong [51], is characterized by [51, 55]

$$I = W \cdot t_s \cdot N_C \cdot \mu \cdot q^{(1-m)} \cdot \left(\frac{\varepsilon_S \cdot m}{N_t \cdot (m+1)}\right)^m \cdot \left(\frac{2m+1}{m+1}\right)^{(m+1)} \cdot \frac{V^{(m+1)}}{L^{(2m+1)}}, \tag{5.2}$$

where W and t_s are the width and thickness of the semiconductor respectively, q is the charge of an electron, N_C is the effective density of states in the conduction band, μ is the electron mobility, ε_S is the dielectric permittivity of the semiconductor, N_t

is the total trap density, V is the applied voltage, and L is the device length. The variable m is defined as

$$m = \frac{T_t}{T}, \tag{5.3}$$

where T is the measurement temperature and T_t is a temperature parameter characterizing the trap distribution which can be related to the characteristic trap energy, E_T, via Boltzmann's constant, k_B, i.e., $E_T = k_B \cdot T_t$ [51].

5.3 Square-Law Modeling

TFT behavior is often modeled using the square-law equations [56],

$$I_D = 0, \tag{5.4}$$

for a TFT in cut-off,

$$I_D = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot \left[(V_{GS} - V_{ON}) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right], \tag{5.5}$$

for a TFT in pre-saturation, and

$$I_D = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (V_{GS} - V_{ON})^2, \tag{5.6}$$

for a TFT in saturation, where I_D is the drain current, V_{GS} is the voltage difference between the gate and source, V_{DS} is the voltage difference between the drain and source, V_{ON} is the turn-on voltage, W is the channel width, L is the channel length, μ is the majority carrier mobility, and C_{INS} is the gate capacitance density.

The cut-off equation, Eq. 5.4, is established by the condition that $V_{GS} < V_{ON}$. The pre-saturation equation, Eq. 5.5 applies when $V_{GS} \geq V_{ON}$ and $V_{DS} < V_{GS} - V_{ON}$, whereas the saturation equation, Eq. 5.6, is applicable when $V_{GS} \geq V_{ON}$ and $V_{DS} \geq V_{GS} - V_{ON}$. The last two V_{DS} equations are alternatively written as $V_{DS} < V_{DSAT}$ and

$V_{DS} \geq V_{DSAT}$, respectively, where V_{DSAT} denotes the drain-source voltage defining the demarkation between pre-saturation and saturation. Quantitatively, $V_{DSAT} = V_{GS} - V_{ON}$.

Although these square-law equations do not explicitly define which terminal is the drain or source, it turns out that this distinction is of critical importance in the SCLC assessment which follows.

The source is the injecting contact from which electrons enter the TFT channel. The drain is the extracting contact from which electrons exit the TFT channel. To properly function as a source (drain), this electrode must be maintained at a lower (higher) potential so that it efficiently injects (extracts) electrons into (from) the channel. These considerations mandate that the polarity of V_{DS} is always positive if the square-law equations are to be properly employed.

In order to proceed with this SCLC assessment, it is useful to clarify the following terms - turn-on voltage, V_{ON}, threshold voltage, V_{TH}, enhancement-mode, and depletion-mode.

V_{ON} of a TFT is the potential difference between the gate (control terminal) and the source, designated V_{GS}, needed to reach an onset of the flow of drain current, as shown in Fig. 5.2(a). This voltage corresponds to the so-called flat-band voltage, since TFTs are accumulation-mode devices. V_{ON} is a parameter best suited to TFT device physics assessment. V_{TH} of a TFT corresponds to a V_{GS} at which appreciable drain current flows, as estimated using a technique such as that shown in Fig. 5.2(b). V_{TH} is a parameter most appropriate for circuit assessment.

A TFT is enhancement-mode if $V_{ON} > 0$. In this case, a positive V_{GS} is needed to form an accumulation channel. At $V_{GS} = 0$ the channel is sufficiently depleted so that negligible drain current flows upon application of an appropriate V_{DS}. A TFT is depletion-mode if $V_{ON} < 0$. In this case, a negative V_{GS} is required to deplete the channel so that the drain current is turned off. At $V_{GS} = 0$, a conducting channel is already formed so that drain current flows upon application of an appropriate V_{DS}.

For this assessment, it is assumed that both V_{ON} and V_{TH} have the same sign, i.e., that both are positive, or both are negative. However, this is not always the case.

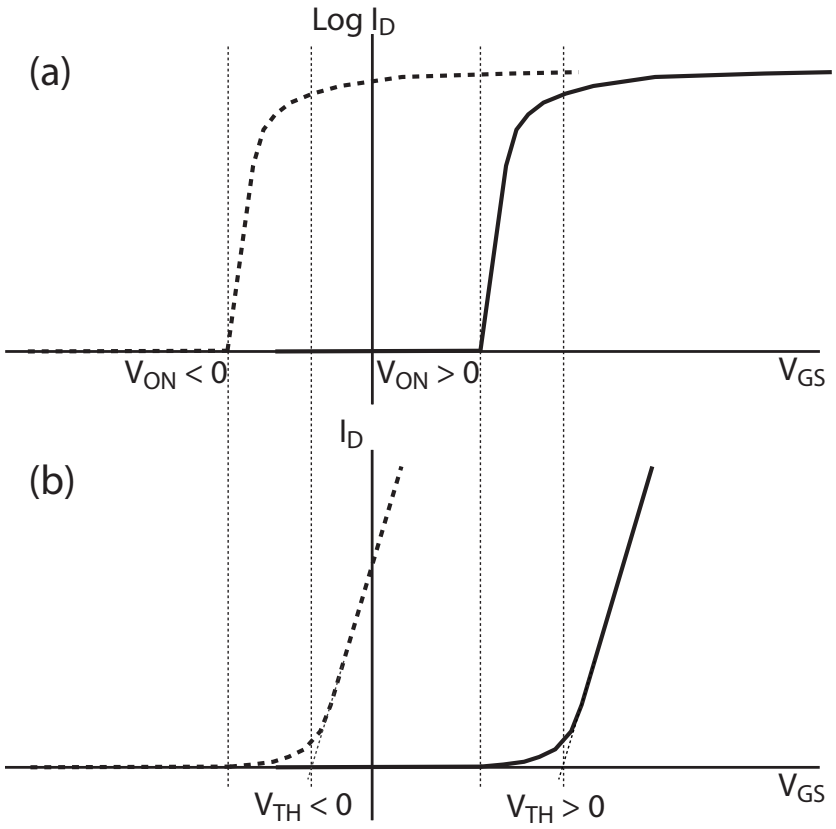

Figure 5.2: Graphical procedures for estimating V_{ON} and V_{TH} for both enhancement-mode (solid) and depletion-mode (dashed) TFTs. (a) V_{ON} is estimated as the onset of appreciable drain current using a $log(I_D)$ - V_{GS} transfer curve. (b) V_{TH} is estimated from linear extrapolation to the x-axis of an I_D-V_{GS} transfer curve for small V_{DS}'s, i.e., when $V_{DS} \leq 1$ V.

5.4 TFT Testing Configurations

Three TFT configurations are considered for undertaking SCLC assessment: (1) floating gate, (2) diode-tied (i.e., gate tied to the drain), and (3) source-tied. The last two configurations, it turns out, are physically identical. Thus, these two configurations are discussed together.

5.4.1 Floating Gate Configuration

With the gate floating, it is expected that the gate should have no effect. Thus, a three-terminal TFT is anticipated to simply behave as a two-terminal resistor. This configuration, shown in Fig. 5.3, is symmetrical. Thus, the polarity of V_{DS} is irrelevant since, according to the convention employed in this assessment, V_{DS} is always positive with respect to the extracting contact (i.e., the drain).

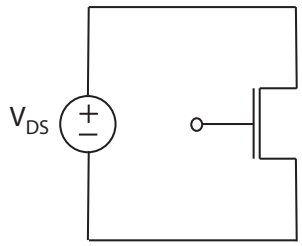

Figure 5.3: Schematic representation of the floating gate measurement configuration. Note that the drain is the positively biased terminal and the source is the negatively biased terminal. If the polarity of the V_{DS} source is reversed, the drain is still defined to be the positively biased terminal.

Actually, it is found experimentally that when the gate is left floating, a history dependence or memory effect may occur due to "gate charging." That is, after an initial SCLC measurement on a virgin device, the gate can appear to become charged by application of a high V_{DS}. Subsequent SCLC measurements exhibit a larger I_D at a given V_{DS} when compared to an earlier sweep. This "gate charging" could,

in principle, be the result of either trapped charge within the semiconductor or of electron injection and charge storage within the gate insulator. This topic is revisited in section 5.6.

5.4.2 Diode-Tied / Source-Tied Configuration

Figure 5.4 shows that diode-tied and source-tied configurations are actually identical, once it is recognized that injecting (source) and extracting (drain) contacts are defined by the polarity of V_{DS}. Thus, only one assessment is required for these two seemingly different circuit configurations. Subsequently these physically-equivalent configurations are collectively denoted as diode-tied.

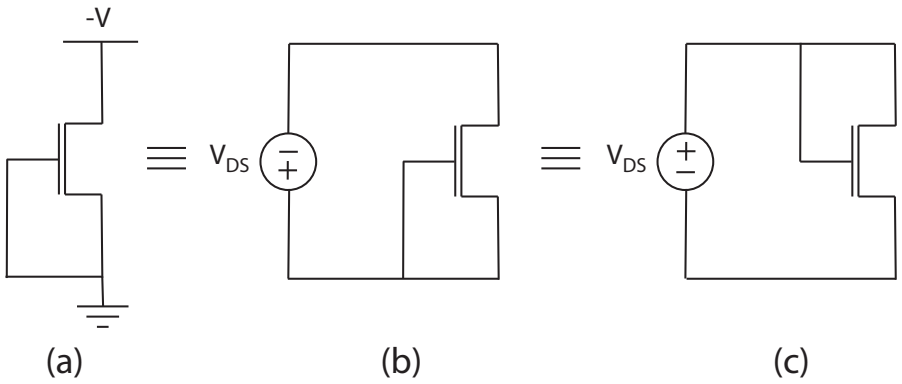

Figure 5.4: Equivalence of diode-tied and source-tied configurations. (a) A source-tied configuration with a negative drain bias applied to the "drain". However, the drain cannot be at a lower potential than the source and remain the extracting contact. Therefore, the negative applied voltage polarity defines this terminal to actually be the source due to its injecting nature. (b) The same configuration as shown in (a) except with a two-polarity V_{DS} source. (c) A diode-tied configuration. Notice that (a), (b) and (c) are identical.

5.5 Expected *I-V* Output Curves

Figure 5.5 shows expected output *I-V* curves of a diode-tied TFT for both a depletion- and an enhancement-mode TFT. The nature of these *I-V* plots is elucidated in the following discussion.

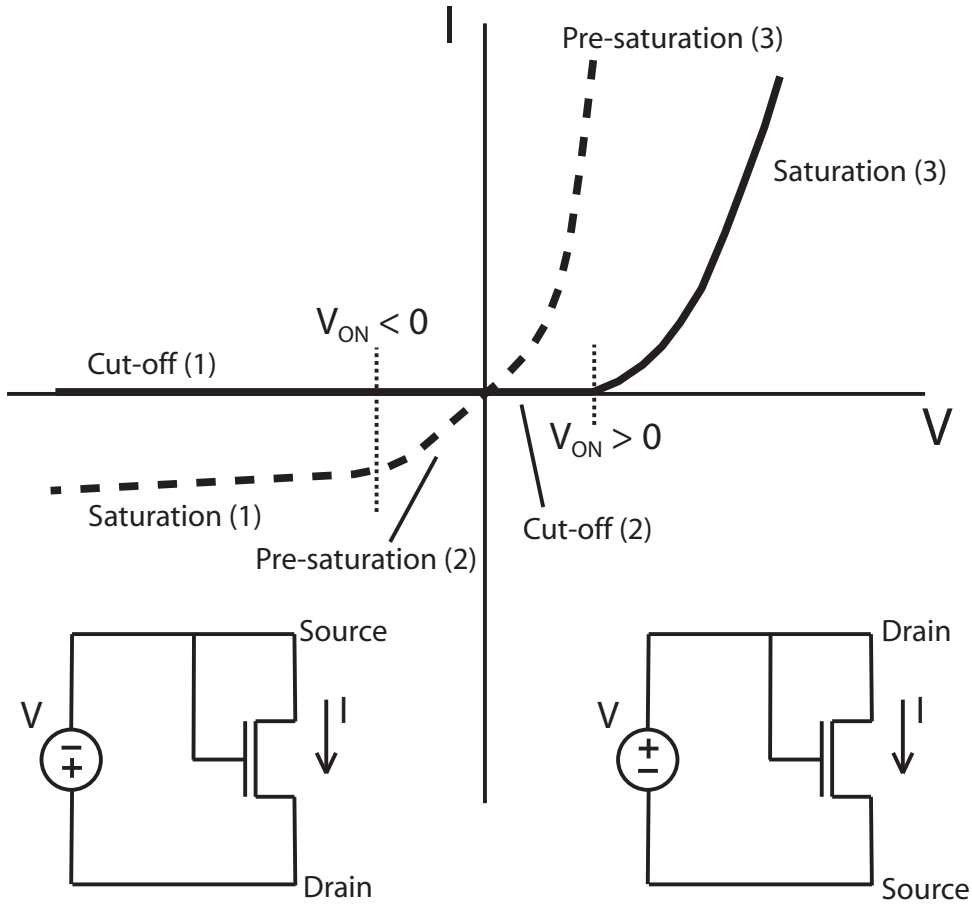

Figure 5.5: Expected output *I-V* curves for a diode-tied TFT for both a depletion-mode (dashed) and an enhancement-mode (solid) TFT.

Table 5.1 is a summary of operating conditions and square-law-based equations leading to the diode-tied *I-V* characteristics given in Fig. 5.5. Note that each *I-V*

curve is divided up into three regions for both the depletion- and enhancement-mode TFT. A detailed discussion of each region of operation for both types of devices, i.e., depletion- and enhancement-mode is provided as follows.

Table 5.1: A summary of operating conditions and square-law-based equations leading to the diode-tied I-V characteristics shown in Fig. 5.5.

TFT Type	**Region** *(see Fig. 5.5)*	**Applied** V	V_{GS}, V_{DS}, I_D	**On?** (i.e., $V_{GS} \geq V_{ON}$)	**Saturation?** (i.e., $V_{DS} \geq V_{GS} - V_{ON}$)	I-V **Equation**
Enhancement (i.e., $V_{ON} > 0$)	(1)	$V < 0$	$V_{GS} = 0$ $V_{DS} \equiv \lvert V \rvert$ $I_D \equiv -I$	No	—	$I = 0$
”	(2)	$0 < V < V_{ON}$	$V_{GS} = V_{DS} \equiv V$ $I_D \equiv I$	No	—	$I = 0$
”	(3)	$V > V_{ON}$	$V_{GS} = V_{DS} \equiv V$ $I_D \equiv I$	Yes	Yes	$I = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (V - V_{ON})^2$
Depletion (i.e., $V_{ON} < 0$)	(1)	$V < V_{ON}$	$V_{GS} = 0$ $V_{DS} \equiv \lvert V \rvert$ $I_D \equiv -I$	Yes	Yes	$-I = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (\lvert V_{ON} \rvert)^2$
”	(2)	$V_{ON} < V < 0$	$V_{GS} = 0$ $V_{DS} \equiv \lvert V \rvert$ $I_D \equiv -I$	Yes	No	$-I = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot \ \lvert V_{ON} \rvert \cdot \lvert V \rvert - \frac{\lvert V \rvert^2}{2}$
”	(3)	$V > 0$	$V_{GS} = V_{DS} \equiv V$ $I_D \equiv I$	Yes	No	$I = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot \ (V + \lvert V_{ON} \rvert) \cdot V - \frac{V^2}{2}$

5.5.1 Diode-Tied, Enhancement-Mode TFT

For the diode-tied enhancement-mode case, the TFT is either off or in saturation as shown by the I-V output curve labels in Fig. 5.5 and as summarized in Table 5.1. This assertion is elucidated in the following discussion.

5.5.1.1 Regions 1 and 2: Applied Voltage Less than V_{ON}

By definition, V_{ON} is positive for an enhancement-mode TFT. Also, by definition $I_D = 0$ when $V_{GS} \leq V_{ON}$. Therefore, $I = 0$ for for positive $V_{GS} \leq V_{ON}$.

Next, recognize from the left-hand insert included in Fig. 5.5 that the gate is tied to the negative injecting, or source terminal when the applied voltage is negative. This means that $V_{GS} = 0$. Substituting this and $V_{ON} > 0$ into the condition for the TFT to be on (i.e., $V_{GS} \geq V_{ON}$), results in the TFT being in cut-off since $V_{GS} < V_{ON}$. Therefore, for any value of $V \leq V_{ON}$ the enhancement-mode TFT is in cut-off and $I = 0$, where I_D is replaced by I in order to conform with the inserts shown in Fig. 5.5.

5.5.1.2 Region 3: Positive Applied Voltage Greater Than V_{ON}

First, recognize from the right-hand insert included in Fig. 5.5 that the gate is tied to the positive (extracting, or drain) terminal. This means that $V_{GS} = V_{DS} \equiv V$. Thus, replacing V_{GS} and V_{DS} with V in the constraining equation defining saturation (i.e., $V_{DS} \geq V_{GS} - V_{ON}$) leads to $V \geq V - V_{ON}$. This inequality is *always true* for any positive value of V for an enhancement-mode TFT. Therefore, for positive applied voltages greater than V_{ON}, the enhancement-mode TFT is in saturation. The saturation regime equation, Eq. 5.6, can be rewritten as

$$I = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (V - V_{ON})^2 , \tag{5.7}$$

where I_D is replaced by I and V_{GS} is replaced by V in order to conform with the right-hand insert shown in Fig. 5.5.

The I-V relationship specified by Eq. 5.7 is such that $I \propto V^2$, and could potentially be confused with the $I \propto V^{(m+1)}$ relationship characteristic of SCLC.

5.5.2 Diode-Tied, Depletion-Mode TFT

For the diode-tied depletion-mode case, the TFT is either in pre-saturation or saturation as shown in Fig. 5.5 and as summarized in Table 5.1. This assertion is proven in the following discussion.

5.5.2.1 Region 1: Negative Applied Voltage Less Than V_{ON}

In this case, the applied voltage is *more negative* than V_{ON} (depletion-mode). Recognize from the left-hand insert included in Fig. 5.5 that the gate is tied to the negative injecting, or source terminal when the applied voltage is negative. This means that $V_{GS} = 0$ and $V_{DS} \equiv |V|$. Substituting this and $V_{ON} < 0$ (depletion-mode) into the condition for saturation, $(V_{DS} \geq V_{GS} - V_{ON})$, results in $|V| \equiv V_{DS} \geq -V_{ON}$. This inequality is *always true* for negative values of V where $|V| \equiv V_{DS} > |V_{ON}|$ and $V_{ON} \leq 0$ (depletion-mode). Therefore, for negative applied voltages more negative than V_{ON}, the depletion-mode TFT is in saturation. The saturation regime equation, Eq. 5.6, can be rewritten as,

$$-I = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (|V_{ON}|)^2 \,, \tag{5.8}$$

where I_D is replaced by $-I$ and V_{GS} is replaced by 0 in order to conform with the insert shown in Fig. 5.5. Thus, the current is constant and given by Eq. 5.8 for a depletion-mode TFT in which the applied voltage is less than V_{ON}.

5.5.2.2 Region 2: Negative Applied Voltage Between Zero and V_{ON}

Recognize from the left-hand insert included in Fig. 5.5 that the gate is tied to the negative injecting, or source terminal when the applied voltage is negative. This means that $V_{GS} = 0$ and $V_{DS} \equiv -V$. Substituting this and $V_{ON} < 0$ (depletion-

mode) into the condition for saturation, (i.e., $V_{DS} \geq V_{GS} - V_{ON}$), results in $-V \equiv V_{DS} \geq -V_{ON}$. This inequality is *only false for* negative values of V between zero and V_{ON}. Therefore, for negative applied voltages, where $V_{ON} < V < 0$ the depletion-mode TFT is in pre-saturation. The pre-saturation regime equation, Eq. 5.5, can be rewritten as,

$$-I = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot \left[|V_{ON}| \cdot |V| - \frac{|V|^2}{2} \right], \tag{5.9}$$

where I_D is replaced by $-I$ and V_{GS} and V_{DS} is replaced by $|V|$ in order to confirm with the left-hand insert shown in Fig. 5.5.

The I-V relationship specified by Eq. 5.9 is such that $I \propto V^2$, and could potentially be confused with the $I \propto V^{(m+1)}$ relationship characteristic of SCLC.

5.5.2.3 Region 3: Positive Applied Voltage

First, recognize from the right-hand insert included in Fig. 5.5 that the gate is tied to the positive extracting, or drain terminal. This means that $V_{GS} = V_{DS} \equiv V$. Substituting this and $V_{ON} < 0$ (depletion-mode) into the condition for saturation, (i.e., $V_{DS} \geq V_{GS} - V_{ON}$), results in $V \geq V - V_{ON}$. This inequality is *always false* for any positive value of V for an depletion-mode TFT. Therefore, for positive applied voltages, the depletion-mode TFT is in pre-saturation. The pre-saturation regime equation, Eq. 5.5, can be rewritten as,

$$I = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot \left[(V + |V_{ON}|) \cdot V - \frac{V^2}{2} \right], \tag{5.10}$$

where I_D is replaced by I and V_{GS} and V_{DS} are replaced by V in order to conform with the right-hand insert shown in Fig. 5.5.

The I-V relationship specified by Eq. 5.10 is such that $I \propto V^2$, and could potentially be confused with the $I \propto V^{(m+1)}$ relationship characteristic of SCLC.

5.5.3 $I \propto V^2$ Slope Comparisons For Enhancement- and Depletion-Mode Devices

Note that the slope of Eq. 5.7 and Eq. 5.10 can be rewritten respectively as,

$$\frac{\partial I}{\partial V} = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (V - |V_{ON}|)\,, \tag{5.11}$$

and

$$\frac{\partial I}{\partial V} = \frac{W}{L} \cdot \mu \cdot C_{INS} \cdot (V + |V_{ON}|)\,. \tag{5.12}$$

Thus, the slope of a diode-tied depletion-mode TFT when it is turned on (in pre-saturation) is larger than that of a diode-tied enhancement-mode TFT when it is turned on (in saturation).

5.5.4 The Equivalence of Diode-Tied and Source-Tied Configurations

The I-V characteristics for an enhancement-mode and a depletion-mode TFT are illustrated in Fig. 5.6 for both a diode-tied and a source-tied configuration. The equivalence of the diode-tied and source-tied configurations is readily evident.

5.6 Discussion

The I-V curves presented in Fig. 5.5 and the mathematical relationships given in Eq. 5.7 and Eq. 5.10 show that $I \propto V^2$. Thus, if a SCLC measurement is performed using a gate biased (i.e., diode-tied) TFT structure, it will be very difficult if not impossible to distinguish whether a measured $I \propto V^{(m+1)}$ characteristic arises from SCLC or simply from normal transistor action. Notice that the diode-tied TFT assessment undertaken herein, and which leads to a prediction of $I \propto V^2$ characteristics, is formulated using simple square-law theory. Square-law theory ignores electron trapping. A more realistic model would account for electron trapping. Although such a model has not yet been formulated, it is likely that it might lead to a $I \propto V^{(m+1)}$ power-law behavior. If it did, it is not clear whether this $I \propto V^{(m+1)}$

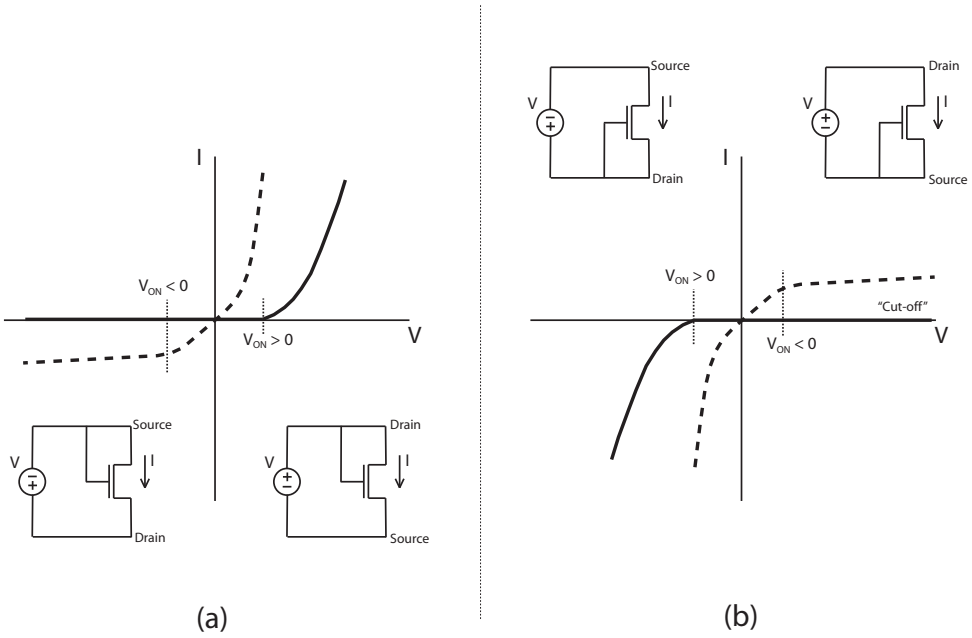

Figure 5.6: Expected output I-V curves for (a) a diode-tied and (b) source-tied TFT. Depletion-mode (dashed) and enhancement-mode (solid) TFT configurations are indicated for both situations.

behavior would be directly ascribed to an exponential trap distribution mechanism or to a more complicated trap-related type of transistor action.

Given these concerns, it is recommended that SCLC assessment not be undertaken using a gate-biased TFT structure. Rather, it is recommended that SCLC assessment be accomplished using a floating-gate TFT structure, as originally employed by Hong [51].

The floating-gate TFT structure for accomplishing SCLC assessment has two primary advantages. First, it employs the same TFT structure which is used to evaluate V_{ON}, V_{TH}, μ, I_D^{ON-OFF}, hysteresis, and other relevant transistor properties. Thus, band tail state information extracted from SCLC measurements can be directly correlated to TFT properties obtained from an assessment of the same device. Second, ambiguities associated with discriminating between SCLC or transistor action as the mechanism responsible for $I \propto V^{(m+1)}$ behavior are avoided.

A demerit associated with using a floating-gate TFT structure for accomplishing SCLC assessment is the history-dependent or memory effect due to "gate charging," as alluded to in section 5.4.1. Recall that "gate charging" manifests itself as an increase of I, for a given V, when a SCLC measurement is repeated more than once. In other words, the SCLC I-V curve does not retrace itself when measured multiple times. Moreover, there is a systematic tendency for I to increase for the second measurement.

At first, this behavior seemed puzzling and made questionable the viability of floating-gate TFT measurements since these measurements appeared to lack reproducibility. However, in retrospect, this history-dependent phenomena appears to have a simple explanation. SCLC measurements involve trap filling. After a SCLC measurement has been conducted, some of the traps which were empty in the virgin device remain persistently filled. The deeper the trap energy, the longer it takes for the filled trap to re-emit. If traps remain persistently filled after an initial SCLC measurement, a subsequent SCLC measurement will yield a larger I at a given V since fewer of the injected electrons are required to fill traps so that they can contribute to an enhancement of the current. This appears to be the simplest explanation of the history-dependent or memory effect.

In principle, "gate charging" could be ascribed to electron injection through the gate insulator and charge storage on the floating gate. This mechanism seems unlikely since 100nm thick thermal silicon dioxide is used as the gate insulator. For the gate oxide fields used (≤ 5 MV/cm) charge injection through the gate oxide seems unlikely.

If persistent trap filling is indeed responsible for the history-dependent trends witnessed in SCLC measurements of floating-gate TFT structures, it should be possible to reset the test device back towards its virgin state. This could be accomplished by heating the device to an elevated temperature to thermally assist the trap emptying process. Alternatively, the device could simply be left in the dark for a prolonged

period of time prior to be retested. Both of these strategies have been employed, with some success, by Hoshino [57] in his study of IGZO TFT stability. His studies provide evidence of deep traps with very long re-emission times ($\geq 10^5$ sec), which is consistent with the trap filling mechanism advocated herein to explain the history-dependent or memory effect.

Recent SCLC measurements performed on "gateless" structures shown in Fig. 5.7 do not show the onset of SCLC and instead show an $I \propto V$ (i.e., ohmic) relationship with applied voltages as high as 100 V. This suggests that the floating gate in

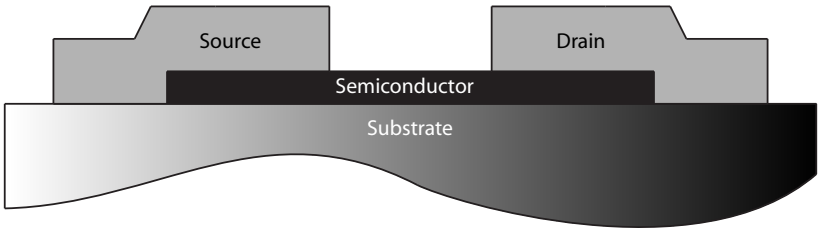

Figure 5.7: Gateless structure based on three-terminal TFT devices where the semiconductor and source/drain dimensions are equal to that of a staggered bottom-gate TFT. Note that the substrate is quartz, and when placed on a testing chuck, will act as an extremely thick gate insulator.

present with SCLC measurements performed on three-terminal devices influences on the onset of SCLC. Research into the ZTO band structure performed by Erslev [58] utilizing transient photocapacitance spectroscopy (TPC), drive level capacitance profiling (DLCP), and modulated photocurrent spectroscopy (MPC) suggests that the SCLC parameters extracted using measurements on three-terminal devices are actually measured from within a small "intrinsic channel" or accumulation region within the semiconductor at the semiconductor-insulator interface. The working theory is that trapped charge within the non-ideal (i.e., exponential trap distribution) semicon-

ductor under test perturbs the charge balance and ultimately creates an accumulation region within the semiconductor through capacitive coupling with the floating gate. It should be noted that this theory needs more work and empirical analysis.

5.7 Conclusions

The objective of this work is to ascertain whether a three-terminal device (i.e., a TFT) is an appropriate structure for conducting SCLC measurements. A major finding of this chapter is that it is not appropriate to use a diode-tied or gate-biased TFT configuration for conducting a SCLC assessment since square-law theory shows that transistor action alone gives rise to $I \propto V^2$ characteristics which can easily be mistakenly attributed to a SCLC mechanism. Instead, a floating gate TFT configuration is recommended for accomplishing SCLC assessment of AOS channel layers. Even though this approach is subject to a history-dependent or memory effect, it is argued that this phenomena is inherent to SCLC measurements due to the persistence of trap filling.

6. DIELECTRIC ASSESSMENT

This chapter focusses on dielectric leakage characteristics. Specifically, interpretation and assessment of non-ideal electrical characteristics and corresponding material properties are considered.

6.1 Introduction

As observed in Fig. 4.1 in Chapter 4, poor quality TFT gate insulators cause gate leakage, which, in turn, results in low circuit yield and poor reliability. Additionally, gate leakage can lead to an overestimation of the channel mobility in a TFT. The objective of this chapter is to present an approach to dielectric leakage assessment.

6.2 Dielectric Measurements

Figure 6.1 illustrates a commonly used dielectric assessment test structure. The structure consists of a heavily-doped, p-type silicon substrate that acts as a backside "metal", a blanket-coated dielectric, and shadow-masked aluminum $\sim$1 mm^2 dots. Each dot, along with the heavily-doped substrate, represents a contact to a metal-insulator-metal (MIM) capacitor. This structure is attractive because of the

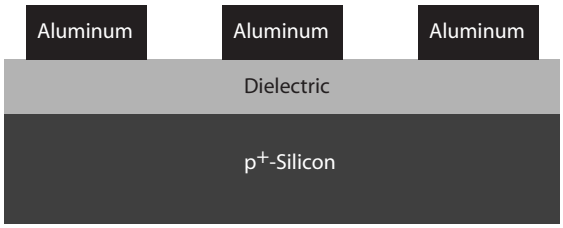

Figure 6.1: Metal-insulator-metal (MIM) structures for dielectric testing and assessment.

pristine nature and smoothness of its interfaces so that it does not contain any sidewall dielectric coverage non-idealities (i.e., step coverage non-idealities).

As shown in Fig. 6.2, each MIM capacitor is subjected to a logarithmic current density, J, versus applied electric field, ξ, test, i.e., $log(J)$-ξ, from which the dielectric leakage and breakdown characteristics are extracted. The test is terminated when the current density reaches 10 μA/cm^2. It is the results of the $log(J)$-ξ test, examining

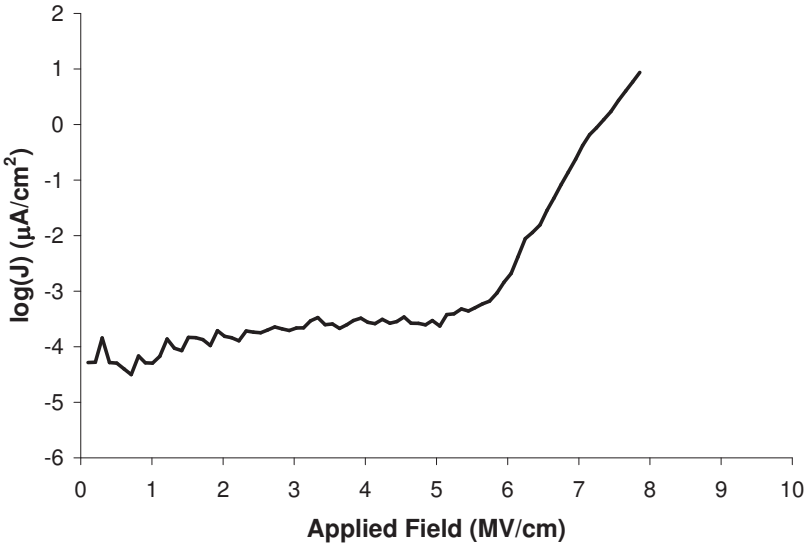

Figure 6.2: Logarithmic current density versus applied DC electric field plot for a metal-insulator-metal (MIM) capacitor. The dielectric under test is an excellent quality 100 nm thick SiO_2 thermally grown on a heavily-doped silicon substrate

the leakage characteristics, that is the focus of this chapter.

The test structure is denoted to be a MIM device, even though it could alternatively be referred to as a metal-insulator-semiconductor (MIS) device. However,

since the silicon substrate is heavily (degenerately) doped, it is assumed to be metal-like in electrical behavior. The validity of the MIM designation is supported by the observation that switching the polarity of the applied voltage in either a capacitance-frequency or $log(J)$-ξ test results in no significant change in the assessed electrical performance of the insulator under test.

An example of a $log(J)$-ξ curve of a high-quality dielectric is given in Fig. 6.3. Often, the electrical quality of such a device is summarized by specifying two quantities, the leakage current density, J_{LEAK}, at an applied electric field of 1 MV/cm, and the breakdown electric field, ξ_{BREAK}, which is often operationally defined as the applied electric field at which a current density of 10 μA/cm^2 is measured.

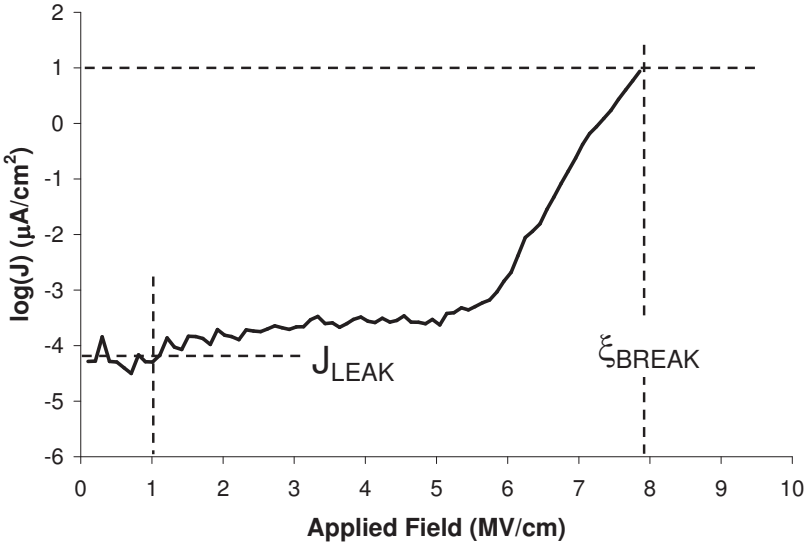

Figure 6.3: The insulator quality of the dielectric specified by the $log(J)$-ξ curve of Fig. 6.2 is summarized by specifying the leakage current density, J_{LEAK}, at an applied electric field of 1 MV/cm and the breakdown field, ξ_{BREAK}, which is defined as the electric field at which a current density of 10 μA/cm^2 is measured.

Figure 6.4 illustrates a basic flaw in the J_{LEAK}, ξ_{BREAK} approach for assessing dielectric electrical quality. Although all three $log(J)$-ξ curves shown have very similar values of J_{LEAK} and ξ_{BREAK}, the pre-breakdown dielectric quality of these three dielectrics are clearly different when $log(J)$-ξ curves are compared. The dielectric associated with the dotted $log(J)$-ξ curve results in unacceptable TFT gate insulator performance. TFTs fabricated using this type of dielectric display gate currents whose $log(I_G)$-V_{GS} leakage curves track with $log(I_D)$-V_{GS} transfer curves. The solid curve results in excellent quality TFT gate insulator performance. TFTs fabricated using this type of dielectric display gate currents whose $log(I_G)$-V_{GS} leakage curves appear flat (i.e., independent of V_{GS}) and whose values are at or below the drain off-current. The dielectric associated with the dashed $log(J)$-ξ curve results in acceptable TFT gate insulator performance. TFTs fabricated using this type of dielectric display gate currents whose $log(I_G)$-V_{GS} leakage curves appear nearly flat (i.e., very little dependence on V_{GS}) and whose values are at or near the drain off-current. Therefore, an alternative approach to dielectric assessment is presented. This approach utilizes $log(J)$-ξ curves, qualitatively assessing their performance based on the basic shape of the curve. The $log(J)$-ξ curves displayed subsequently are referred to as leakage characteristics. The following discussion focuses primarily on the leakage characteristics and associated conduction mechanisms.

6.3 Dielectric Assessment via the Shape of a $log(J)$-ξ Curve

As shown in Fig. 6.5, qualitative assessment of the electrical performance of a dielectric may be accomplished by identifying a knee in a $log(J)$-ξ curve. This knee is believed to establish the initial onset of breakdown, and is explicitly denoted as defining the breakover knee, $\xi_{BREAKOVER}$. Thus, the $log(J)$-ξ curve below the knee is denoted as pre-breakover, while above the knee is referred to as post-breakover. The breakover knee of Fig. 6.5 occurs at $\sim$5.5 MV/cm, while the 10 μA/cm^2 breakdown occurs at $\sim$7.9 MV/cm. If a knee is not clearly evident in a $log(J)$-ξ curve, the

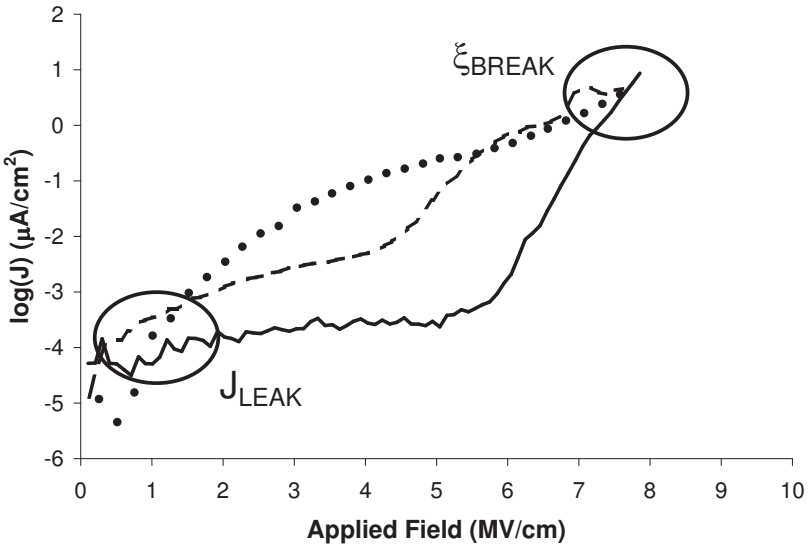

Figure 6.4: A comparison of $log(J)$-ξ curves for three dielectrics of varying quality. Although J_{LEAK} and ξ_{BREAK} are approximately equal for all three curves, their $log(J)$-ξ characteristics, and hence their performance as TFT gate insulators, differ dramatically.

measured current density at low applied electric fields tends to be significantly larger than witnessed in Fig. 6.5, and the dielectric is labeled leaky. Dielectrics that do not exhibit a distinct knee are of lower quality.

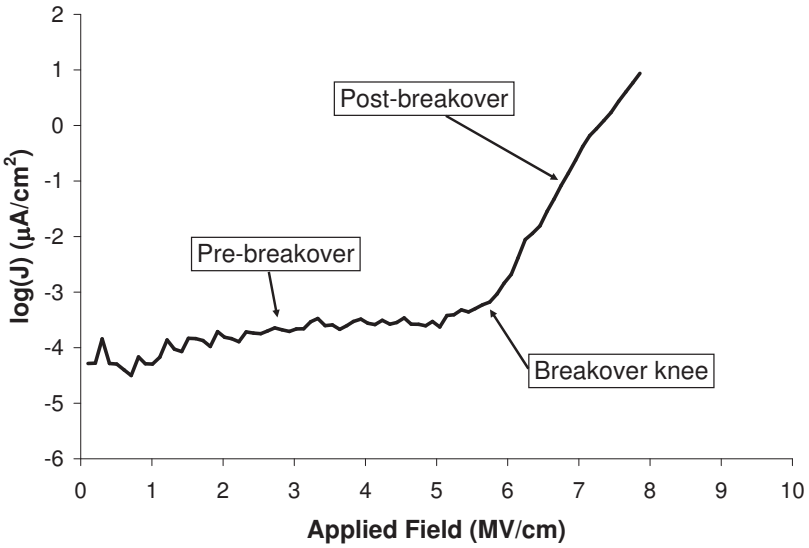

Figure 6.5: A knee in a $log(J)$-ξ dielectric leakage curve defines breakover, establishing pre-breakover from post-breakover. For the MIM capacitor under test, the knee breakover electric field is $\sim$5.5 MV/cm, while the 10 μA/cm^2 breakdown field is $\sim$7.9 MV/cm.

Figure 6.6 is a re-plot of the same $log(J)$-ξ curves which are shown in Fig. 6.4. Three representative $log(J)$-ξ curves are illustrated, and are labeled A, B, and C for identification. The following is a detailed description of each type of curve and its leakage characteristics.

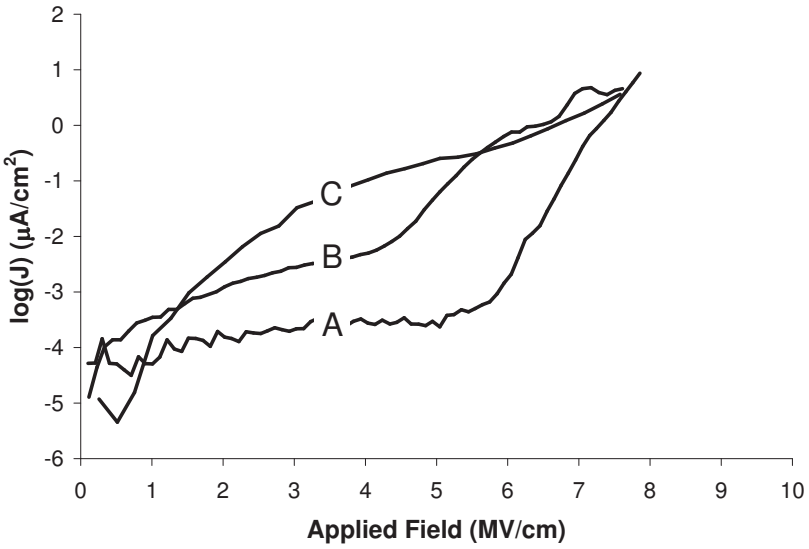

Figure 6.6: $log(J)$-ξ leakage characteristics for (A) an excellent quality 100 nm SiO_2 thermally grown on a heavily-doped silicon substrate, (B) an acceptable quality 90 nm PECVD SiO_2 on an ITO-coated glass substrate, and (C) an unacceptable quality 90 nm PECVD SiO_2 on an ITO-coated glass substrate.

Curve A is an excellent quality 100 nm SiO_2 thermally grown on a heavily-doped silicon substrate. Curve A's leakage characteristic is near ideal because the dielectric is of excellent quality and the interfaces are atomically smooth. When used as a gate insulator, a curve A dielectric produce a TFT with a minimal gate leakage which does not track with the drain current in a $log(I_D)$-V_{GS} transfer curve. Thus, this dielectric is excellent in terms of its TFT gate leakage performance.

Curve B is an acceptable quality 90 nm PECVD SiO_2 on an ITO-coated glass substrate. The physical difference between a MIM device that produces curve A and curve B is that the dielectric for curve A is thermally grown on an atomically smooth silicon substrate, while the dielectric for curve B is an optimized PECVD process on an ITO-coated glass substrate with a relatively rough surface (i.e., atomic force microscopy (AFM) peak-to-peak roughness of $\sim$20 nm). Curve B's leakage characteristic is not ideal because the dielectric is believed to possess pinhole-like shunt defects due to the PECVD process, and the interfaces are rough due to the use of an ITO bottom contact. When used as a gate insulator, a curve B dielectric produces a TFT with a moderate gate leakage which does not track with the drain current in a $log(I_D)$-V_{GS} transfer curve. Thus, this dielectric is acceptable in terms of its TFT gate leakage performance.

Curve C is an unacceptable quality 90 nm PECVD SiO_2 on an ITO-coated glass substrate. The physical difference between a MIM device that produces curve B and curve C is that the PECVD recipe for curve B is optimized, while the PECVD recipe for curve C is un-optimized. The un-optimized process is silane, SiH_4, deficient and deposited at too high of a pressure. Curve C's leakage characteristic is undesirable because, as discussed in Section 6.5, the dielectric is believed to possess pinhole-like shunt defects due to the un-optimized PECVD process and/or due to interfacial roughness associated with the ITO bottom contact. When used as a gate insulator, a curve C dielectric produces a TFT with a severe gate leakage which tracks with the

drain current in a $log(I_D)$-V_{GS} transfer curve. Thus, this dielectric is unacceptable in terms of its TFT gate leakage performance.

6.4 Simulation

To clarify the conduction mechanisms responsible for the shapes of the $log(J)$-ξ curves indicated in Fig. 6.6, a MATLAB-based simulation is performed using the parameters listed in Table 6.1.

Table 6.1: Dielectric $log(J)$-ξ test simulation parameters.

Parameter	**Symbol**	**Nominal Values**	**Units**
Dielectric thickness	d	90-100x10^{-7}	cm
Effective dielectric thickness	d_{EFF}	70x10^{-7}	cm
Mobility	μ	20	cm^2/Vs
Effective mass	m^*	$0.3 \cdot m_o$	kg
Dielectric barrier height	ϕ_B	5.21x10^{-19}	J
Relative dielectric Constant	K_{OX}	3.9	—
Dielectric band gap	E_g	1.44x10^{-18}	J
Dielectric effective density of states in the conduction band	N_c	1x10^{18}	cm^{-3}
Total trap density in the dielectric	N_t	7x10^{18}	cm^{-3}
Trap modeling parameter	m	2-3.3	—
Capacitor area	A_{CAP}	0.011	cm^2
Pinhole-like shunt path defect area	A_{DEFECT}	0.1-1.0x10^{-9}	m^2
Dielectric resistivity	ρ_{OX}	1x10^{16}	Ω-cm
Applied voltage	$V_{APPLIED}$	1-100	V

Curves A, B, and C of Figs. 6.6 are accurately reproduced using Ohmic conduction (linear in ξ), space-charge-limited current (SCLC) (power law in ξ; i.e., ξ^m), and/or Fowler-Nordheim tunneling (exponential in ξ) mechanisms. Figure 6.7 is the simulation output. Simulated curve A is a combination of Ohmic conduction and Fowler-Nordheim tunneling. Simulated curve B is a combination of SCLC and Fowler-Nordheim tunneling. Simulated curve C is entirely dominated by SCLC.

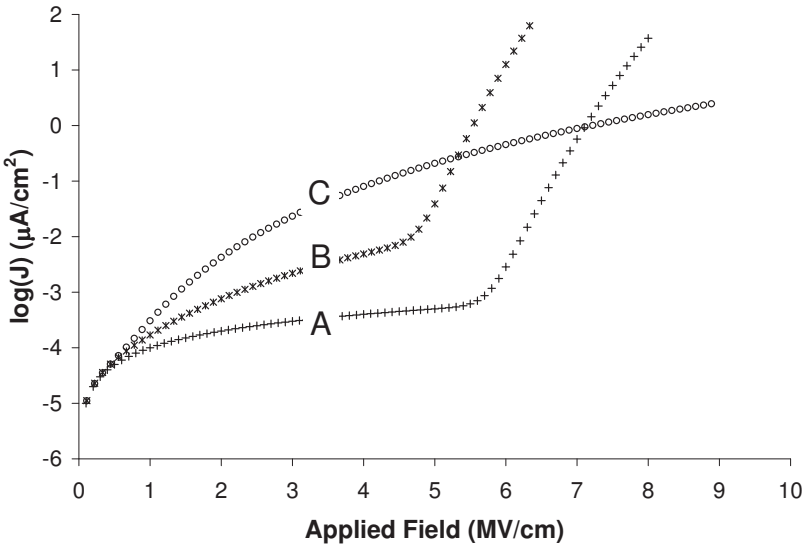

Figure 6.7: Simulated $log(J)$-ξ curves using Ohmic, SCLC, and Fowler-Nordheim tunneling conduction mechanisms.

Figure 6.8 is a single figure comparison of Figs. 6.6 and 6.7, illustrating the good correlation between the measured and simulated $log(J)$-ξ curves. This simulation accurately accounts for the location of the easily distinguishable breakover knee for curve A and curve B, as well as the lack of a breakover knee in curve C.

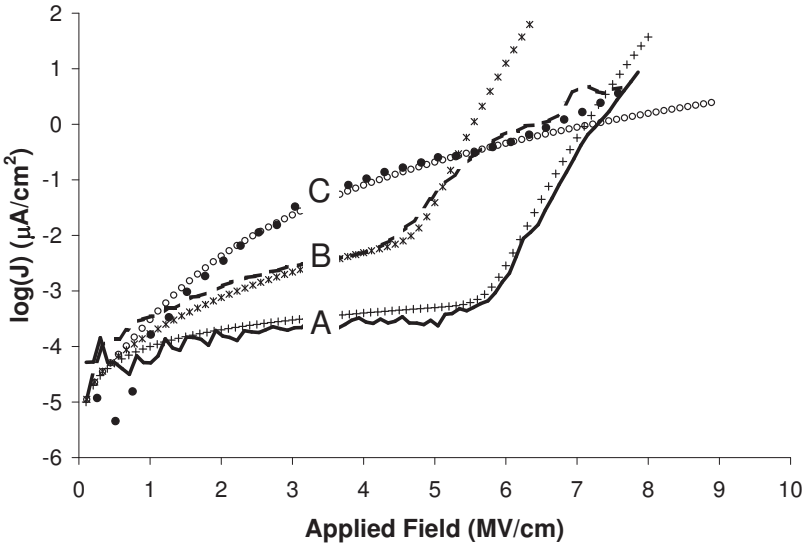

Figure 6.8: Comparison of measured and simulated $log(J)$-ξ curves replotted from Figs. 6.6 and 6.7.

Although the overall correlation is good, there is one major discrepancy between the measured and simulated $log(J)$-ξ curves presented in Fig. 6.8. Most notably, the measured and simulated $log(J)$-ξ versions of curve B drastically diverge from one another beyond ~5.5 MV/cm. This discrepancy is believed to be a manifestation of

charge trapping within the dielectric during the $log(J)$-ξ test. The permanent damage phenomenon is described in detail in *Appendix C. Dielectric Charge Trapping.*

6.5 Detailed Assessment of Curves A, B, and C from Fig. 6.8

The measured and simulated $log(J)$-ξ leakage curves for A, B, and C from Fig. 6.8 are separated and labeled according to their proposed conduction mechanisms in Figs. 6.9, 6.11, and 6.14. The following is a detailed discussion of each of these figures.

6.5.1 Curve A

As noted in Fig. 6.9, the breakover knee for curve A occurs at ~5.5 MV/cm. This is an ideal case dielectric, employing thermal SiO_2. The breakover knee is very clearly defined and is located at a large electric field.

For an applied electric field less than 5.5 MV/cm, curve A is described by Ohmic conduction [53], i.e.,

$$J_{OHMIC} = \frac{\xi}{\rho_{OX}}, \tag{6.1}$$

where J_{OHMIC} is the Ohmic conduction current density in A/cm^2, ξ is the appled electric field in V/cm, and ρ_{OX} is the dielectric resistivity in Ω-cm. The dielectric resistivity used in the simulation is chosen to be 1×10^{16} Ω-cm based on a value commonly reported in the literature [59]. As evident from Fig. 6.9, Ohmic conduction appear to adequately describe the essential pre-breakover leakage trend for curve A.

Notice, however, that the noise associated with curve A in Fig. 6.9 is greater at lower applied electric fields. Also, note that the near-zero electric field current density of the measured data is somewhat larger than that simulated. Moreover, the simulated curve trends towards zero current density at zero electric field, as required by Ohm's law, in contrast to the near-constant current density of the measured curve. These discrepencies between the measured and simulated $log(J)$-ξ curves in pre-breakover are attributed to contributions from a measurement artifact associated

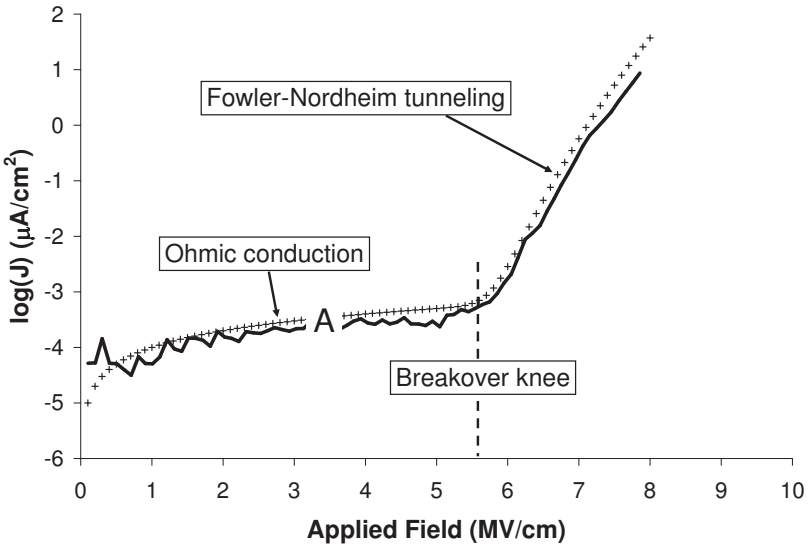

Figure 6.9: $log(J)$-ξ characteristics of an excellent quality 100 nm thick SiO_2 thermally grown on a heavily-doped silicon substrate.

with the displacement current density,

$$J_{DIS} = C\frac{dV}{dt}, \tag{6.2}$$

where J_{DIS} is the displacement current density in A/cm^2, C is the dielectric capacitance density in F/cm^2, and dV/dt is the ramp rate of the applied voltage waveform in V/s during the $log(J)$-ξ test. Note from Eq. 6.2 that a constant displacement current density is expected for a constant applied voltage ramp rate. However, in practice the applied voltage waveform generated by the measurement instrumentation is a voltage staircase, rather than a voltage ramp. Moreover, for better accuracy, the measurement system uses a larger integration time for assessment of lower current densities. These instrumentation issues mean that the ramp rate, and hence the displacement

current, is not necessarily well defined or constant at low measured current densities. Even though this displacement current artifact makes curve A in Fig. 6.9 somewhat noisy at low applied electric fields, the overall $log(J)$-ξ pre-breakover trend appears to be accurately simulated assuming that Ohmic conduction predominates.

As indicated in Fig. 6.9, the post-breakover $log(J)$-ξ characteristic for curve A beyond 5.5 MV/cm is described by Fowler-Nordheim tunneling [53, 60, 61], i.e.,

$$J_{FN} = \frac{q^3 \cdot \xi^2}{16 \cdot \pi \cdot \hbar \cdot \phi_B} exp \left[\frac{-4 \cdot \sqrt{2 \cdot m^*} \cdot \phi_B^{\frac{3}{2}}}{300 \cdot \hbar \cdot q \cdot \xi} \right], \tag{6.3}$$

where J_{FN} is the Fowler-Nordheim tunneling current density in A/cm^2, ξ is the applied electric field in V/cm, q is the charge of an electron in coulombs, $\hbar$ is the reduced Planck's constant (i.e., $\frac{h}{2\pi}$) in joule-seconds, ϕ_B is the dielectric barrier height in joules, and m^* is the effective mass of an electron in SiO_2 in kg. The value of 300 in the denominator of the exponential in Eq. 6.3 is changed from a value of 3 in the original Fowler-Nordheim equation to accommodate the use of V/cm as the units for the applied electric field, as opposed to V/m.

Fowler-Nordheim tunneling is very sensitive to the electron effective mass and dielectric barrier height, which are selected as $0.3 \cdot m_o$ [62] and 3.25 eV respectively. Figure 6.9 shows good correlation between the measured and simulated data, leading to the conclusion that the effective mass and dielectric barrier height values employed are appropriate for the simulation. Small changes in the electron effective mass and/or the dielectric barrier height result in large shifts of the breakover knee. For example, if m^* is changed to $0.42 \cdot m_o$ [63] while ϕ_B is held constant, the simulated breakover knee becomes ~6.6 MV/cm, indicating a shift of > 1 MV/cm. An assessment of the literature suggests that ϕ_B is well established, while the most appropriate value of m^* for SiO_2 is subject to some debate [62, 63].

At first, it might seem that tunneling is an unlikely physical mechanism for current transport through a 100 nm thick, thermally grown SiO_2 dielectric. How-

ever, Fig. 6.10 illustrates that the effective tunnel barrier thickness is greatly reduced at high applied voltages and is indeed consistent with Fowler-Nordheim tunneling. Figure 6.10, using similar triangles, leads to a geometrical relationship,

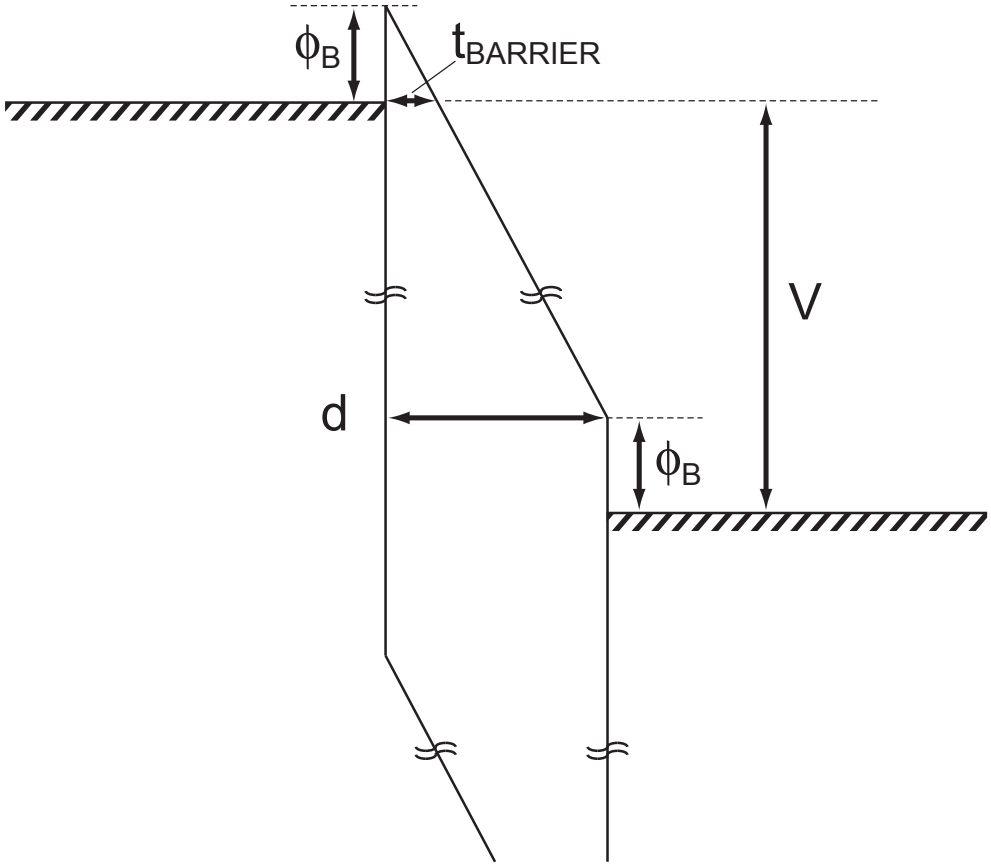

Figure 6.10: Fowler-Nordheim tunneling energy band diagram for a metal-insulator-metal (MIM) capacitor, where $t_{BARRIER}$ is the dielectric tunnel barrier thickness, ϕ_B is the dielectric barrier height, d is the dielectric thickness, and V is the applied voltage between the two MIM metal contacts.

$$t_{BARRIER} = \frac{\phi_B}{V} \cdot d, \tag{6.4}$$

where $t_{BARRIER}$ is the dielectric tunnel barrier thickness in nm, ϕ_B is the dielectric barrier height in eV, d is the dielectric thickness in nm, and V is the applied voltage between the two MIM metal contacts. Equation 6.4 is used only to *approximate* the dielectric tunnel barrier thickness and does not take into account other band bending phenomenon such as image force lowering [60]. Using Eq. 6.4, the dielectric tunnel barrier thickness is approximately reduced to a tunnelable thickness of ∼5.9 nm at an applied bias of ∼55 V and a dielectric barrier height of 3.25 eV. The use of similar triangles and the geometric relationship defined in Eq. 6.4 is only valid if it is assumed that the dielectric barrier height is the same as seen from both MIM contacts. The assumption of equal barrier heights is reasonable considering the work function of the aluminum top contact (4.28 eV) is similar to that of Si bottom contact (4.52 eV).

6.5.2 Curve B

As shown in Fig. 6.11, the breakover knee for curve B occurs at ∼4.25 MV/cm. This is lower than curve A's breakover knee of ∼5.5 MV/cm. This decrease in the breakover knee is attributed to the roughness of the ITO surface. Figure 6.12 illustrates that if the ITO bottom contact has an AFM peak-to-peak roughness of ∼20 nm, then the effective thickness of the dielectric, d_{EFF}, is reduced to ∼70 nm, while the average thickness, d, remains at 90 nm. Scaling the smooth-surface breakover knee of ∼5.5 MV/cm by d_{EFF}/d results in an expected rough-surface breakover knee of ∼4.28 MV/cm. This is in excellent agreement with the ∼4.25 MV/cm breakover knee measured for curve B.

As shown in Fig. 6.11, the pre-breakover $log(J)$-ξ characteristic for curve B up to 4.25 MV/cm is described by a SCLC mechanism, i.e.,

$$J_{PH} = \frac{A_{DEFECT}}{A_{CAP} \cdot 100^2} \cdot N_C \cdot 100^3 \cdot \frac{\mu}{100^2} \cdot q^{1-m} \cdot \left(\frac{\varepsilon_S \cdot 100 \cdot m}{N_t \cdot 100^3 \cdot (m+1)} \right)^m \cdot \left(\frac{2m+1}{m+1} \right)^{(m+1)} \cdot \frac{(\xi \cdot d)^{(m+1)}}{\left(\frac{d}{100}\right)^{(2m+1)}}, \tag{6.5}$$

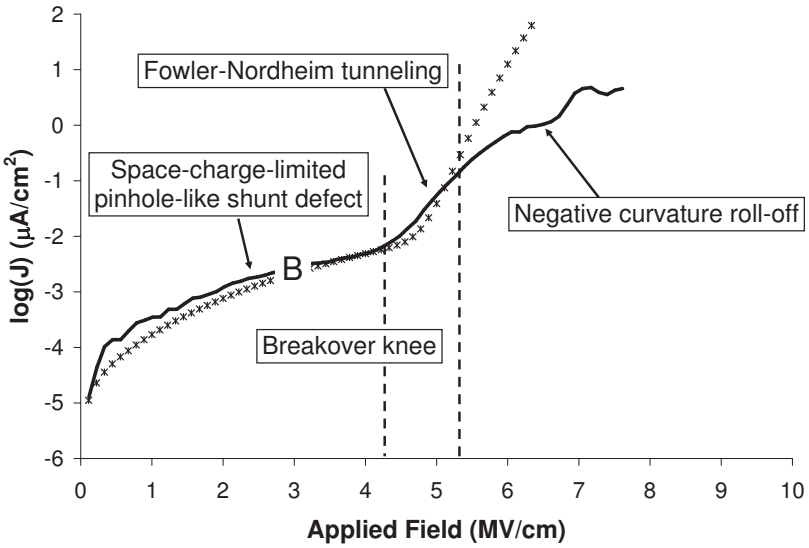

Figure 6.11: $log(J)$-ξ characteristics of an acceptable quality 90 nm thick PECVD SiO_2 on an ITO-coated glass substrate.

where J_{PH} is the SCLC density in A/cm^2, ξ is the applied electric field in V/cm, A_{DEFECT} is the total area of pinhole-like shunt defects in cm^2, A_{CAP} is the area of the capacitor in cm^2, q is the charge of an electron in coulombs, N_C is the effective density of states in the conduction band of the dielectric in cm^{-3}, μ is the electron mobility in the dielectric in cm^2/Vs, ε_S is the dielectric permittivity in F/cm, N_t is the total trap density in the dielectric in cm^{-3}, and d is the dielectric thickness in cm. The variable m is defined as

$$m = \frac{T_t}{T}, \tag{6.6}$$

where T is the measurement temperature and T_t is a temperature parameter characterizing the assumed exponential trap distribution which can be related to the characteristic trap energy, E_T, via Boltzmann's constant, k_B, i.e., $E_T = k_B \cdot T_t$ [51].

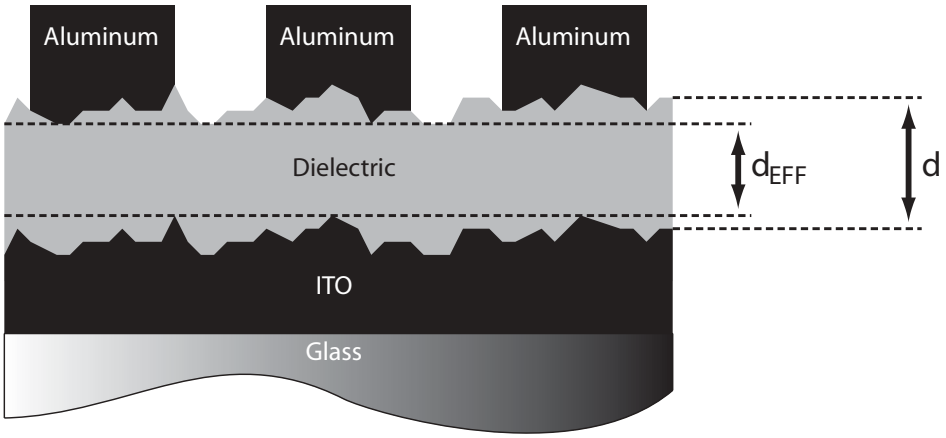

Figure 6.12: Effect of rough interfaces on effective dielectric thickness.

The various occurrences of 100^x constants in Eq. 6.5 are included for unit conversion purposes so that model parameters can be inserted into Eq. 6.5 using conventional units (e.g., electron mobility in the dielectric in cm^2/Vs). The original form of Eq. 6.5 as given in [55], for example, requires exclusive use of mks units.

Equation 6.5 is very similar to the SCLC equation employed in Chapter 5. SCLC implies that the barrier height, ϕ_B, is low enough to allow for efficient carrier injection. However, the $\sim$3 eV barrier associated with SiO_2 is too large for efficient injection. Therefore, as shown in Fig. 6.13, a small-area shunt path (i.e., a pinhole-like defect) is postulated to exist. As current flows through the shunt path, the small area creates a buildup of negative charge (i.e., negative space charge). This space charge inhibits further injection (i.e., limits the current), leading to the power law SCLC relationship, $J \propto \xi^{(m+1)}$. The total area of pinhole-like defects assumed for the curve B simulation is 0.1 nm^2. This is an extraordinarily small value for the total defect area. Of the simulation parameters listed in Table 6.1, μ, N_C, and A_{CAP} are considered to be relatively unimportant and/or well defined. Fitting to measured data in the simulation is accomplished by adjusting m, N_t, and A_{DEFECT}. For curve B, $m = 2$ in the simulation. This value is established by an EXCEL power law fit to the

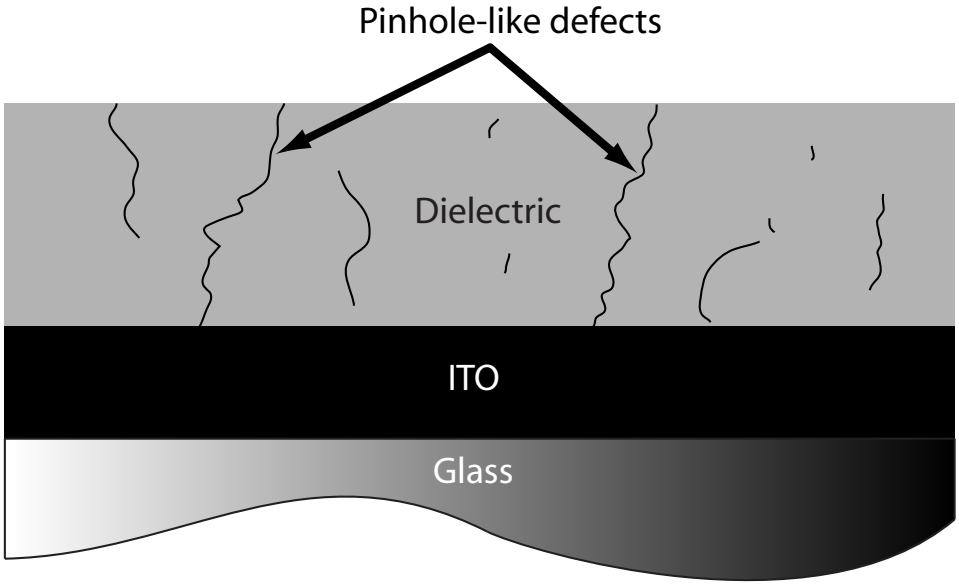

Figure 6.13: Pinhole-like defects acting as small-area shunt paths.

measured data and by recognizing that SCLC theory prescribes that $J \propto \xi^{m+1}$. The parameter m sets the basic shape of the power law SCLC simulated curve. Using Eq. 6.6 and $m = 2$, it is found that the characteristic trap temperature is ∼600 K, which corresponds to a characteristic trap energy of 52 meV. This characteristic trap energy is very similar to the 50 meV value deduced from SCLC measurements of IGZO TFTs annealed at 600 °C [51]. N_t and A_{DEFECT} are SCLC scaling parameters which are used to adjust the overall magnitude of the simulated current density so that it matches that of the measured data. Although $N_t = 7 \times 10^{18}$ cm^{-3} and $A_{DEFECT} = 0.1$ nm^2 are used in the simulation included in Fig. 6.11, these model parameters are not unique. Variation of N_t from ∼10^{15} - 10^{20} cm^{-3}, i.e., over its range of physical viability, would require $A_{DEFFECT}$ to be ∼2.04×10^{-9} - 20.4 nm^2. Thus, while N_t and A_{DEFECT} cannot be considered to be uniquely specified, any physically reasonable choice for N_t leads to a very small value for A_{DEFECT}.

As noted in Fig. 6.11, the post-breakover $log(J)$-ξ characteristic of curve B beyond 4.25 MV/cm to ~5.25 MV/cm is described by Fowler-Nordheim tunneling [53, 60, 61], i.e., Eq. 6.3, except that d has been replaced by d_{EFF} in the calculation of ξ. Fowler-Nordheim tunneling dominates post-breakover due to the relatively low defect density and small cross-sectional area of the pinhole-like shunt paths.

The discrepancy Fig. 6.11 in which the measured and simulated $log(J)$-ξ curves dramatically diverge from one another beyond ~5.5 MV/cm is believed to be a manifestation of charge trapping within the dielectric during the $log(J)$-ξ test. This phenomenon is considered in *Appendix C: Permanent Damage in a MIM Capacitor During $log(J)$-ξ Tests.*

6.5.3 Curve C

As observed in Fig. 6.14, curve C does not display a breakover knee and its $log(J)$-ξ characteristic is dominated by a power law SCLC mechanism attributed to pinhole-like shunt defects. When SCLC contributions to the measured current density are so large that a breakover knee is not detectable, this is indicative of an unacceptable quality dielectric. The total area of the pinhole-like defects for curve C is fit as 1 nm^2 in the simulation if it is assumed that $N_t = 7 \times 10^{18}$ cm^{-3}, i.e., identical to that assumed in Fig. 6.11. While this is an order of magnitude larger than the value used for curve B, this is still a very small value for the total defect area, suggesting that it takes only a few pinhole-like defects to dominate a $log(J)$-ξ curve. The parameter $m = 3.3$ for the simulated curve C, based on EXCEL data fitting to obtain an initial estimate of m. Using Eq. 6.6 and $m = 3.3$, it is found that the characteristic trap temperature is ~990 K, which corresponds to a characteristic trap energy of 85 meV. The higher characteristic trap energy calculated for curve C ($m = 3.3$) than in curve B ($m = 2$) leads to the conclusion that the abruptness of the assumed exponential density of states is less in curve C than in curve B.

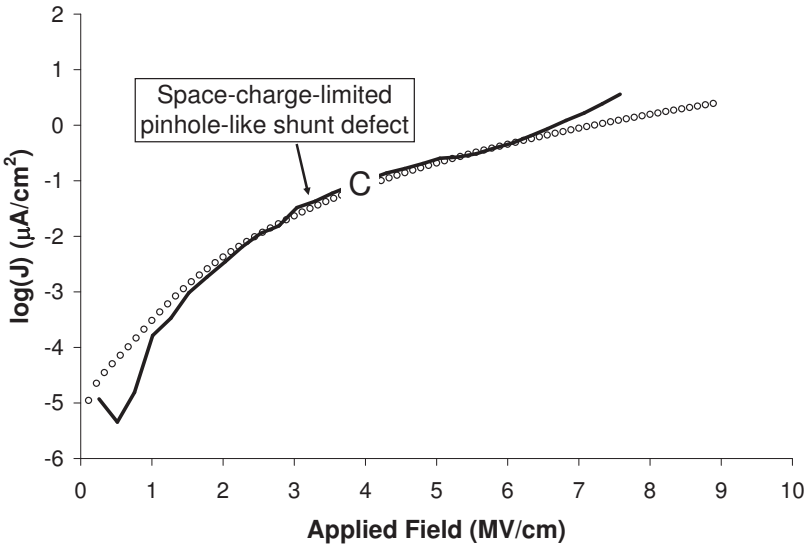

Figure 6.14: $log(J)$-ξ characteristics of an unacceptable quality 90 nm thick PECVD SiO_2 on an ITO-coated glass substrate.

Note that in Fig. 6.14 that the measured and simulated curves diverge from one another somewhat at applied electric fields greater than ∼6.3 MV/cm. This is attributed to Fowler-Nordheim tunneling. Fowler-Nordheim tunneling does not play an important role in establishing the $log(J)$-ξ characteristic for this case due to the increased density of the pinhole-like shunt defects.

6.6 Conclusions

The objective of this chapter is to describe an assessment procedure appropriate for determining if a dielectric is suitable for use as a TFT gate insulator. A major finding of this chapter is that it is critical to examine the shape of a MIM capacitor's $log(J)$-ξ leakage behavior. An appropriate dielectric for use as a TFT gate insulator

should have a $log(J)$-ξ curve that expresses a clear breakover knee, indicative of a high-field conduction mechanism dominated by Fowler-Nordheim tunneling. Such a dielectric produces TFTs with minimal gate leakage which does not track with the drain current in a $log(I_D)$-V_{GS} transfer curve. An inappropriate dielectric for use as a TFT gate insulator will possess a $log(J)$-ξ curve that does *not* express a clear breakover knee, indicating that the dominate conduction mechanism is defect driven (i.e., pin-hole like shunt paths) and, therefore, that the dielectric is leaky. Leaky dielectrics produce poor TFTs with gate leakage current which tracks the drain current in a $log(I_D)$-V_{GS} test. A high level of TFT gate leakage may lead to an overestimation of the channel mobility in a TFT. It is shown that experimental $log(I_D)$-V_{GS} leakage curves can be accurately simulated using Ohmic, space-charge-limited current (SCLC), and Fowler-Nordheim tunneling conduction mechanisms.

Simply stated, in a $log(J)$-ξ curve of a dielectric "shape matters", as it gives direct insight into the dielectric conduction mechanisms and, ultimately, TFT gate insulator leakage and electrical performance characteristics.

7. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

This chapter is a summary of the conclusions drawn from the experimental results of the amorphous oxide semiconductor (AOS) circuit realization and design (Chapter 4), space-charge-limited-current measurements of thin-film transistors (Chapter 5), and dielectric assessment (Chapter 6). In addition, this chapter also discusses suggestions for future work.

7.1 Conclusions

The focus of this research is towards the widespread use and ultimate commercialization of AOS thin-film transistors (TFTs) and AOS *transparent* thin-film transistors (TTFTs). As such, there are three primary focuses of this work, the use of AOS TFTs to create circuits demonstrating the potential of this technology, presentation of a novel approach to characterize TFTs, and presentation of a material assessment approach to aid in identifying dielectrics suitable for TFT gate insulators.

7.1.1 AOS Circuit Realization and Design

The realization of a transparent three-stage ring oscillator with buffered output and an output frequency in the megahertz range. This leads to the possibility of transparent radio frequency applications, such as transparent RFID tags. At the time of its fabrication, this ring oscillator was the fastest oxide electronics ring oscillator reported, with an output frequency of 2.16 MHz, and $t_d = 77$ ns.

The ring oscillator is fabricated using indium gallium oxide (IGO) as the active channel material, plasma enhanced chemical vapor deposition (PECVD) SiO_2 as the gate dielectric, and indium tin oxide (or aluminum) as the gate/drain/source electrodes and traces.

The layout of the ring oscillator circuit proves to be of high importance, as the parasitic capacitors and resistors within the circuit dominate its performance. Therefore, with increased photolithography patterning precision and optimized layout, high performance AOS-based circuits can be realized.

In addition, designs for a high performance AOS-based ring oscillator with > 10 MHz output frequency, and a transparent AOS-based RFID tag are presented. Both circuit designs use a novel approach that does not rely on CMOS-based, or classic, architectures. This novel design approach allows for increased performance with minimal power consumption and number of devices used while being constrained to n-type only architecture (i.e., AOS-based TFTs are limited to n-type conduction only).

7.1.2 Space-Charge-Limited-Current Measurements of Thin-Film Transistors

The objective of this work is to ascertain whether a three-terminal device (i.e., a TFT) is an appropriate structure for conducting space-charge-limited-current (SCLC) measurements. SCLC measurements using three-terminal TFT structures are performed in order to correlate physical SCLC parameters - equilibrium carrier concentration (n_{co}), band tail state density (N_0), total trap density (N_t), characteristic trap energy (E_T), and characteristic trap temperature (T_t) - to TFT device properties - V_{ON}, V_{TH}, μ_{INC}, μ_{AVE}, hysteresis, and drain current on-to-off ratio.

A major finding of Chapter 5 is that it is not appropriate to use a diode-tied or gate-biased TFT configuration for conducting a SCLC assessment since square-law theory shows that transistor action alone gives rise to $I \propto V^2$ characteristics which can easily be mistakenly attributed to a SCLC mechanism. Instead, a floating gate TFT configuration is recommended for accomplishing SCLC assessment of AOS channel layers. Even though this approach is subject to a history-dependent or memory effect, it is argued that this phenomena is inherent to SCLC measurements due to the persistence of trap filling.

7.1.3 Dielectric Material Assessment

The objective of this task is to describe an assessment procedure appropriate for determining if a dielectric is suitable for use as a TFT gate insulator. A major finding of Chapter 6 is that it is critical to examine the shape of a MIM capacitor's $log(J)$-ξ leakage behavior. An appropriate dielectric for use as a TFT gate insulator should have a $log(J)$-ξ curve that expresses a clear breakover knee, indicative of a high-field conduction mechanism dominated by Fowler-Nordheim tunneling. Such a dielectric produces TFTs with minimal gate leakage which does not track with the drain current in a $log(I_D)$-V_{GS} transfer curve. An inappropriate dielectric for use as a TFT gate insulator will possess a $log(J)$-ξ curve that does *not* express a clear breakover knee, indicating that the dominate conduction mechanism is defect driven (e.g., pin-hole like shunt paths) and, therefore, that the dielectric is leaky. Leaky dielectrics produce poor TFTs with gate leakage current which tracks the drain current in a $log(I_D)$-V_{GS} test. A high level of TFT gate leakage may lead to an overestimation of the channel mobility in a TFT. It is shown that experimental $log(I_D)$-V_{GS} leakage curves can be accurately simulated using Ohmic, space-charge-limited current (SCLC), and Fowler-Nordheim tunneling conduction mechanisms.

Simply stated, in a $log(J)$-ξ curve of a dielectric "shape matters", as it gives direct insight into the dielectric conduction mechanisms and, ultimately, TFT gate insulator leakage and electrical performance characteristics.

7.2 Future Work

The following sections outline and explain the motivation for several future work projects. Much of the research into these projects has been carefully planned, or in some cases tested, as evident from the detailed discussions below. Still, the following discussions are considered preliminary as these projects are not complete. The projects include the incorporation of depletion-mode TFTs as load devices into circuit design, substrate considerations for large-area low-cost applications, interlayer

dielectrics and passivation, and a novel vertical transport TFT device design and fabrication.

7.2.1 Depletion-Mode Load Circuits

A major improvement to any single-channel (i.e., n-type only) circuit is the use of a depletion-mode transistor for the load [23]. Unfortunately this adds processing complexity as two different channel behaviors must be produced (i.e., enhancement- and depletion-mode). The advantage of this design is, unlike enhancement-mode transistor loads, depletion-mode loads allow the output of the circuit to reach the high supply rail (i.e., a depletion-mode load inverter output can equal V_{DD}, the high supply rail) and have exceptionally large DC gain [23].

7.2.2 A "Jelly Doughnut" Vertical Transport TFT

During the course of the work reported herein a tangential topic on vertical transport TFT design emerged. Having precise control of film thickness lends itself to the fabrication of a vertical transport TFT. An example of a vertiacl transport TFT structure is shown in Fig. 7.1, and corresponds to a TFT rotated on its side [9]. In this configuration, the channel material deposited thickness now dictates the TFT

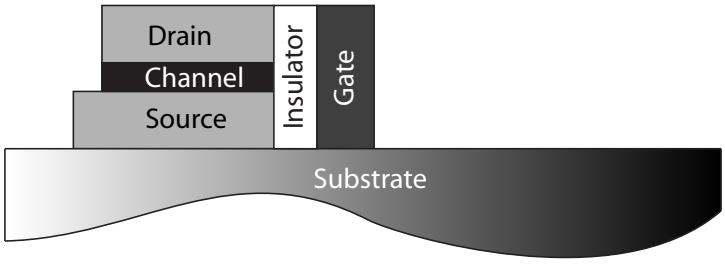

Figure 7.1: A vertical transport TFT in which the channel material deposited thickness dictates the TFT channel length, L.

channel length, L.

An alternative "jelly doughnut" design for a vertical transport TFT is shown in Fig. 7.2. The depth, or channel width, W, is created by revolving the structure about the right-hand side (i.e., the gate contact).

Figure 7.3 outlines a sequence of processing steps for fabricating the "jelly doughnut". First, a transparent glass substrate is chosen for use in a self-aligned photolithography process, as discussed in step three below. Second, an amorphous metal, being opaque, smooth, and etch resistant, for the source contact is deposited and patterned using conventional PVD techniques (e.g., thermal evaporation, electron beam, or sputtering) and photolithography (or lift-off if etching is too difficult). Etch resistance is required so that the source contact layer can be an etch stop layer. Third, using the glass substrate and amorphous metal layer as a photomask, lift-off patterning can be performed for the next two layers, channel and drain contact. Fourth, an AOS channel material is deposited using sputtering. Fifth, a chromium drain contact is deposited using a non-sputtering PVD technique (e.g., thermal evaporation or electron beam) to avoid plasma processing, and associated issues, on top of the channel material. Chromium, a high temperature metal, is chosen so that the channel material can be annealed. Sixth, the AOS and chromium layers are patterned via lift-off patterning. Seventh, the device stack is annealed to improve the channel materials electrical performance. Eighth, a contact area to the source contact is opened up using conventional photolithography and dry etching, using the amorphous metal as an etch stop. Ninth, an aluminum oxide (Al_2O_3) dielectric as the gate insulator is deposited via atomic layer deposition (ALD). The Al_2O_3 dielectric also serves as the initial passivation layer. Tenth, an aluminum gate "plug" is deposited and wet etched using hydrochloric acid (HCl). The Al_2O_3 dielectric should provide good selectivity and etch resistance with respect to HCl. Eleventh, a PECVD silicon nitride (Si_3N_4) dielectric as a final passivation layer is deposited. The thick Si_3N_4 dielectric layer also serves to decrease the parasitic capacitance created from the overlapping

interconnects of the gate and source/drain. Twelfth, vias to the source/gate/drain contacts are patterned and wet etched through both the Si_3N_4 and Al_2O_3 dielectrics using phosphoric acid (H_3PO_4). Thirteen, interconnects are deposited and patterned.

Figure 7.4 outlines an alternate sequence of processing steps with the objective to eliminate the lift-off patterning step. To eliminate lift-off patterning, the amorphous metal source contact, AOS channel, and chromium drain contact layers can be deposited sequentially and patterned simultaneously via conventional photolithography and dry etching. This alternate sequence of processing steps no longer requires the substrate to be transparent, as it is no longer used as a photomask. The self-aligned nature of the device is preserved since the insulator-source/channel/drain interfaces are all defined simultaneously. First, a smooth substrate is chosen. Unlike the process listed above, this substrate is not required to be transparent. Second, an amorphous metal, being opaque, smooth, and etch resistant, for the source contact is deposited using conventional PVD techniques (e.g., thermal evaporation, electron beam, or sputtering). Etch resistance is required so that the source contact layer can be an etch stop layer. Third, a AOS channel material, is deposited using sputtering. At this point, it seems logical to anneal the channel material. However, due to the difficulty in etching annealed amorphous oxides, annealing is performed post-etch. Fourth, a chromium drain contact is deposited using a non-sputtering PVD technique (e.g., thermal evaporation or electron beam) to avoid plasma processing, and associated issues, on top of the channel material. Chromium, a high temperature metal, is chosen so that the channel material can be annealed. Fifth, an etch mask is created using conventional photolithography. Sixth, the entire source/channel/drain stack is etched using dry etching and the etch mask is removed. Step seven and beyond are identical to the processing steps detailed above. A disadvantage of this alternate processing method is smearing of the source/channel/drain layers during

dry etching which has the potential of creating shunt paths between the source and drain contacts.

There are several advantages of the "jelly doughnut" design. First, the W/L ratio can be quite large since L, dictated by the channel material deposited thickness, is very small (i.e., ∼50 nm), while W, dictated by the circumference of the insulator-drain/channel/source interface, can be very large (i.e., many microns). Second, the decreased L dramatically improves high-frequency operation and small signal gain. Third, parasitic capacitance is minimized, because the gate-source/drain overlap, $GSD_{OVERLAP}$, has been reduced to that of the source/drain deposited material thickness. This reduction of the parasitic capacitance also greatly improves high-frequency operation, switching times, and transient response. Fourth, self-aligned photolithography processes are possible using the technique previously described. Fifth, passivation of devices/circuits is simple because the Al_2O_3 dielectric completely surrounds the AOS channel material and serves as the initial passivation, or capping layer. Then, an additional PECVD Si_3N_4 dielectric for a hermetic seal, using the Al_2O_3 capping layer as a barrier to the PECVD plasma and the associated negative processing effects the plasma has on the channel layer.

A similar design approach was published by Garnier et al. in 1998, in which organic semiconductor-based TFTs were created using a circular geometry [64]. However, key differences exist. Most importantly, Garnier et al.'s design focuses on electroluminescent films and liquid crystal displays, which require maximum drain electrode area. The specific design produces TFTs with very large gate-source/drain overlaps, $GSD_{OVERLAP}$, which contributes to a very large parasitic capacitance. The suggested "jelly doughnut" design does not suffer from the same design restrictions and therefore has minimal parasitic capacitance.

Additionally, De Lima et al. in 2009 proposed a circular-gate transistor [65]. De Lima et al.'s design has the same advantages of a large W/L ratio and minimized parasitic capacitance as the proposed "jelly doughnut" design. However, De Lima

et al.'s design is realized using conventional silicon-based transistor technology that requires processes such as ion implantation or diffusion to create source/drain wells. The suggested "jelly doughnut" design uses oxide electronics materials and therefore has the advantage of low-cost and large-area processes.

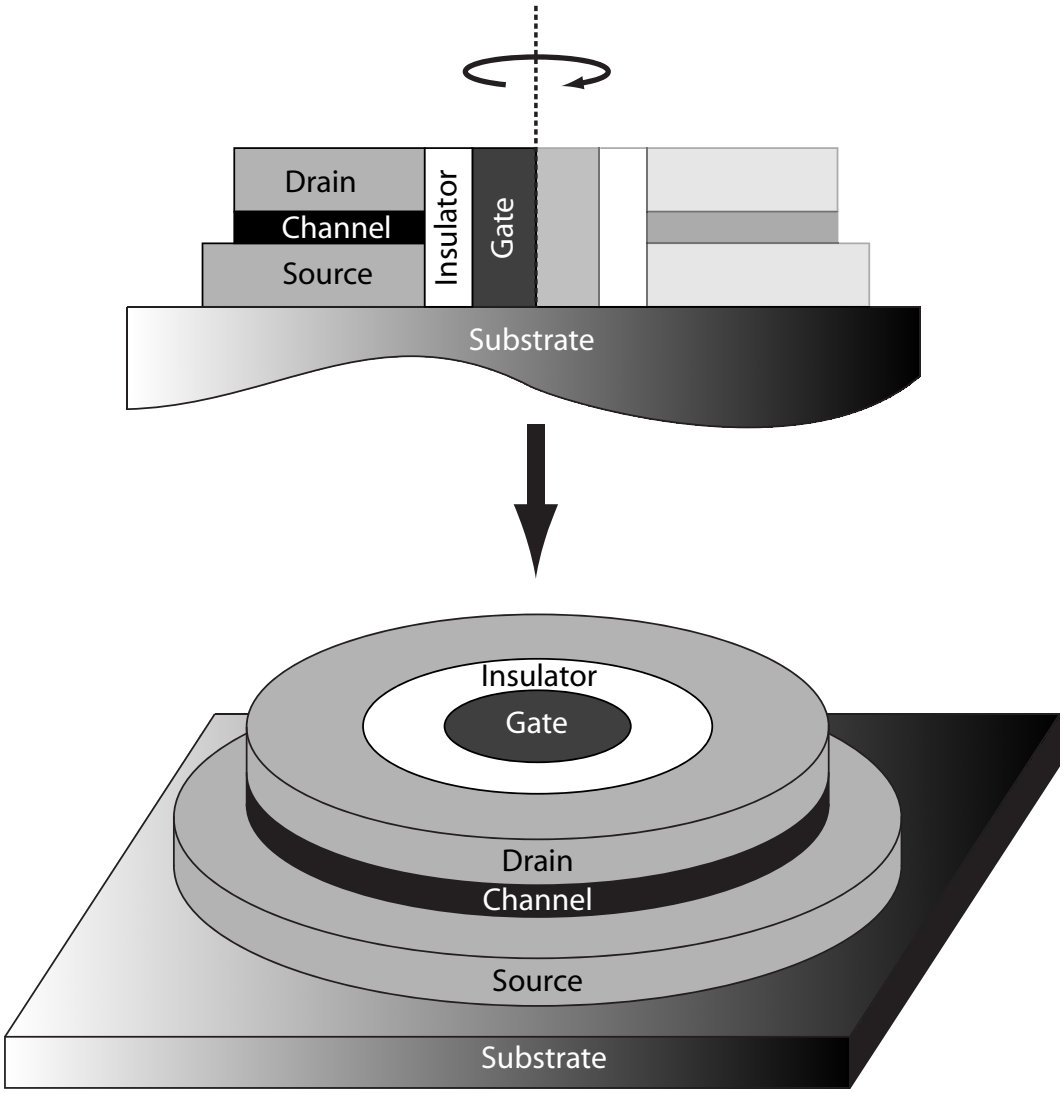

Figure 7.2: An idealized "jelly doughnut" vertical transport TFT, in which the TFT channel width, W, is created by revolving the structure about the gate contact.

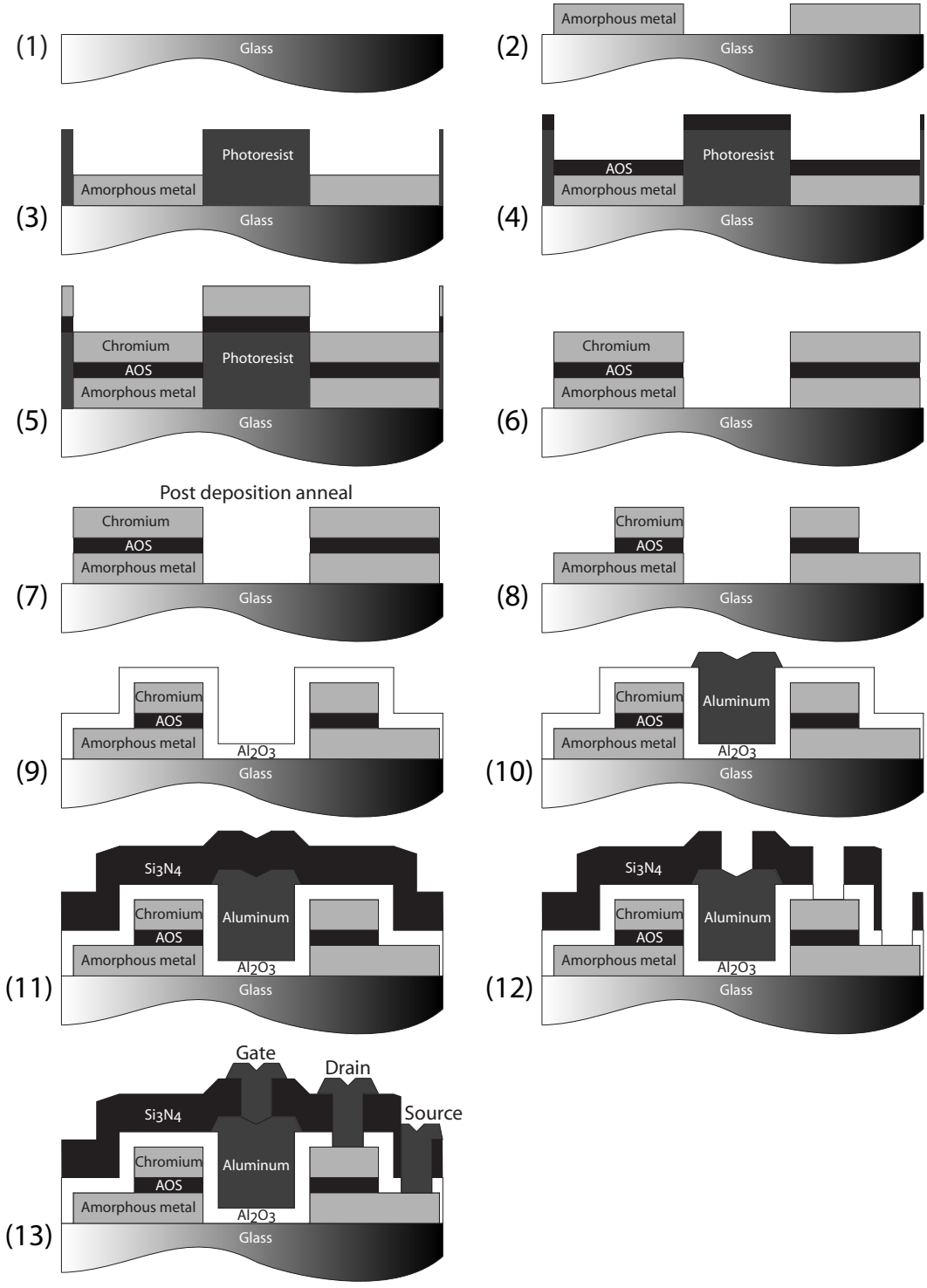

Figure 7.3: "Jelly doughnut" vertical transport TFT processing steps.

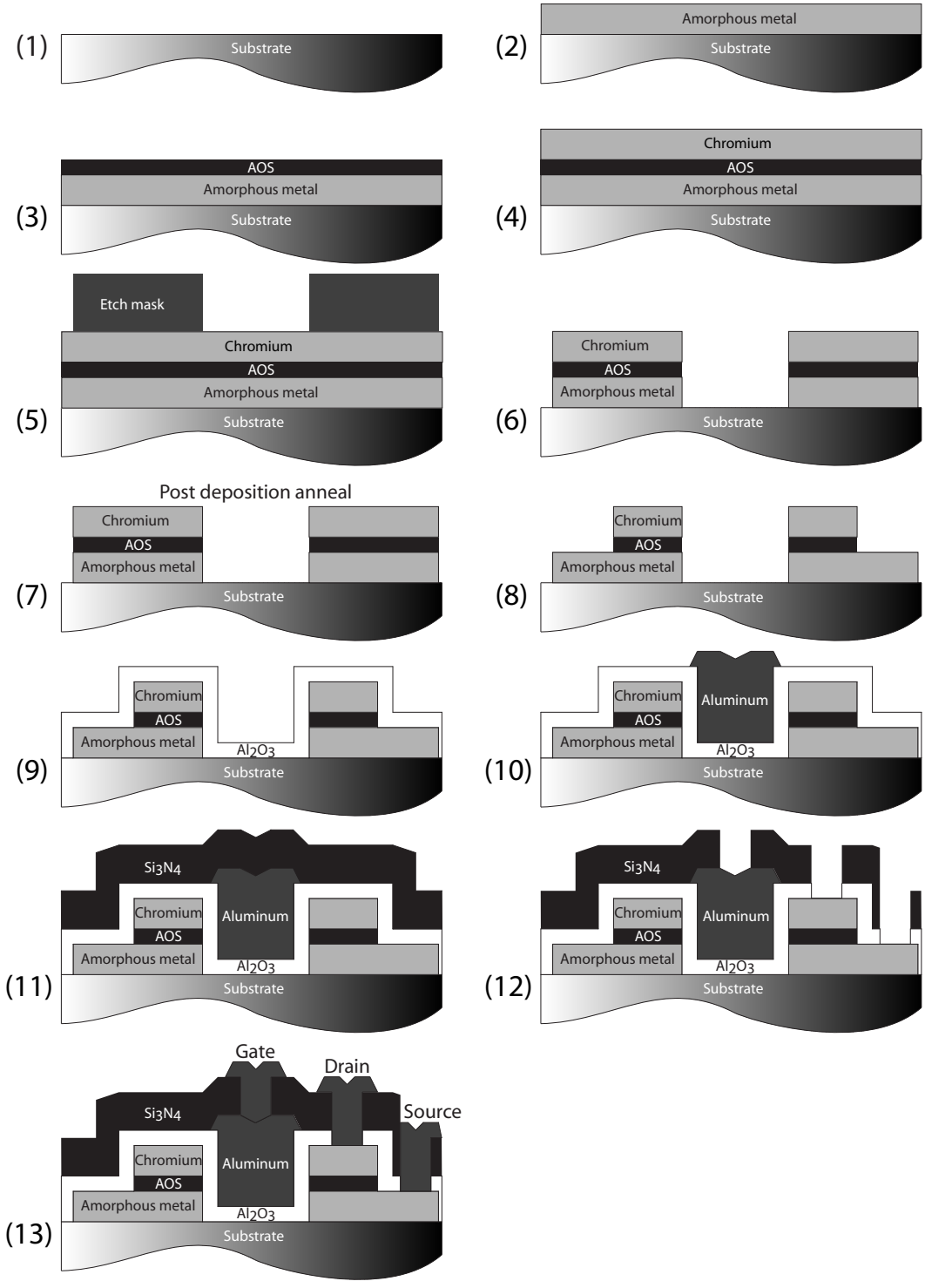

Figure 7.4: "Jelly doughnut" vertical transport TFT alternate processing steps.

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APPENDICES

Appendix A. Process Flow

Substrate Preparation

Substrate preparation has an interesting paradox where less is more, but only to a point. For example, it is observed for thermal silicon dioxide (TOX) on heavily doped p-type coupons used for channel material development that a thorough cleaning is necessary for a good semiconductor-gate insulator interface. However, the use of ultrasonic cleaners, multiple tweezers (to clean *under* the tweezers), and other cleaning agents such as Kontrad 70 have all resulted in poor TFT performance indicated by increased hysteresis, decreased mobility, and decreased subthreshold swing. For the such TOX samples a thorough rinsing in acetone, methanol (replaced by isopropanol alcohol), and deionized water (also known as AMD clean) followed by a hotplate dehydration is the best. Other substrates, such as the ITO coated 1737 glass from Delta Technologies requires an initial ultrasonic clean in Kontrad 70 before the AMD clean. Note that the Kontrad 70 solution is extremely difficult to remove when allowed to dry. Therefore, samples must be quickly and thoroughly rinsed with deionized water upon removal from the ultrasonic cleaner. The difficulty in removing the Kontrad 70 solution, and therefore the residue left behind, has been shown via atomic force microprobe (AFM) to roughen the surface of films and substrates. Therefore, the ultrasonic Kontrad 70 treatment should be avoided, unless the ITO coated 1737 glass substrates are particularly dirty.

Between all dry steps (i.e., post hotplate and pre deposition) the samples benefit from a quick dry clean with a nitrogen blow gun to remove any particles. *This step is assumed below and will not be specifically noted again.*

TOX on silicon samples

- Rinse with DiH_2O
- Blow dry with N_2

- AMD clean
- Blow dry with N_2
- Dehydrate on hotplate
  - 200 °C
  - 10 minutes

ITO coated glass

- Ultrasonic clean *Avoid this step unless absolutely necessary*
  - Kontrad 70 solution
  - 40 °C
  - 60 minutes
- Rinse with DiH_2O
- Blow dry with N_2
- AMD clean
- Blow dry with N_2
- Dehydrate on hotplate
  - 200 °C
  - 10 minutes

Generic Photolithography Recipes

Provided below are generic photolithography recipes for both etching and lift off purposes. They are labeled generic due to the profound impact that the environment (i.e., temperature and humidity) has on the process. This is a good "all around" recipe, but the user should be prepared to "tweak" as needed.

Photolithography - Etch

- HMDS surface prep
  - Dispense enough HMDS (MicroChem MCC Primer 80/20) to coat surface
  - Let sit idle for 20 seconds
  - Spin: 3K RPM for 10 seconds, then 4K RPM for 20 seconds
  - Dehydrate on hotplate
    - 115 °C
    - 3 minutes
- Let substrate cool
- Dispense photoresist (S1818 positive resist) *amount varies based upon substrate size*
- Spin: 3K RPM for 10 seconds, then 4K RPM for 20 seconds
- Photoresist bake on hotplate
  - 85 °C
  - 2 minutes
- Let substrate cool
- Expose: 11 seconds using MJB3 aligner
- Develope

  - 5:1 DiH_2O:351 Developer
  - ∼40 seconds *with agitation*
  - Rinse with DiH_2O
- Photoresist semi-hard bake on hotplate
  - 85 °C
  - 15 minutes
- Let substrate cool
- Progress to etch...

Photolithography - Lift Off

- HMDS surface prep
  - Dispense enough HMDS (MicroChem MCC Primer 80/20) to coat surface
  - Let sit idle for 20 seconds
  - Spin coat HMDS: 3K RPM for 10 seconds, then 4K RPM for 20 seconds
  - Dehydrate on hotplate
    - 115 °C
    - 3 minutes
- Let substrate cool
- Dispense photoresist (S1818 positive resist) *amount varies based upon substrate size*
- Spin coat photoresist: 3K RPM for 10 seconds, then 4K RPM for 20 seconds
- Bake photoresist on hotplate
  - 85 °C

  - 2 minutes

- Let substrate cool
- Expose photoresist: 11 seconds using MJB3 aligner
- Develope photoresist
  - 5:1 DiH_2O:351 Developer
  - $\sim$40 seconds *with agitation*
  - Rinse with DiH_2O
- Removal of excess water from photoresist on hotplate
  - 85 °C
  - 2 minutes
- Let substrate cool
- Progress to thin-film deposition...

Single Channel Staggard Bottom-Gate Circuit Process flow

This process flow is for a TTFT or transparent circuit using IGO as the channel material. Note that the source/drain contact and trace layer is defined by lift-off patterning. However, the use of a co-planar bottom gate structure would eliminate the need for lift-off of the source/drain layer.

- Substrate prep for ITO coated glass
- Photolithography for gate traces (ITO) *etch*
- Etch ITO
  - non-diluted HCl (12.1 Molar)
  - $\sim$2 minutes if *thin ITO* used ($\sim$150-200 nm, $R_S = 4 - 8\ \Omega$)
  - $\sim$5 minutes if *thick ITO* used ($\sim$15-30 nm, $R_S = 70 - 100\ \Omega$)
- AMD clean (remove photoresist)
- Dehydrate on hotplate
  - 115 °C
  - 3 minutes
- PECVD deposit gate insulator (SiO_2)
  - Pressure: 250 mTorr
  - RF Power: 250 Watts
  - SiH_4 (2% in helium balance) flow: 75 sccm (15% on 500 sccm MFC)
  - N_2O flow: 100 sccm (20% on 500 sccm MFC)
  - Time: $\sim$5 minutes for $\sim$100 nm layer
- RF Sputter deposit AOS channel (IGO, 1:1) using CPA
  - Pressure: 5 mTorr

  - RF Power: 75 Watts
  - 90:10 Ar:O_2 gas mix (Ar = 40 sccm, O_2 = 4.4 sccm)
  - Target-substrate distance = 4 inches
  - 10 min for a ∼50 nm thick layer
- Photolithography for IGO *etch*
- Etch IGO
  - 5:1 DiH_2O:HCl
  - ∼1 minute
- AMD clean (remove photoresist)
- Dehydrate on hotplate
  - 115 °C
  - 3 minutes
- Post deposition anneal IGO
  - 500 °C
  - 5 °C/min ramp rate
  - 1 hour in air
- Photolithography for gate insulator (SiO_2) Vias *etch*
- Etch SiO_2 Vias
  - Buffered HF solution
  - ∼5 minutes (*this is strongly dependent on the quality of the SiO_2 layer!*)
- AMD clean (remove photoresist)
- Dehydrate on hotplate

  - 115 °C
  - 3 minutes

- Photolithography for source/drain contacts and traces (ITO) with *lift off*
- RF Sputter deposit source/drain contacts and traces (ITO) using CPA
  - Pressure: 5 mTorr
  - RF Power: 75 Watts (normally 100 Watts, but lowered to avoid photoresist damage)
  - 100% Ar gas mix (Ar = 40 sccm)
  - Target-substrate distance = 4 inches
  - 12 minutes ∼100-120 nm thick layer ***DOUBLE CHECK THIS!!!***
- Lift off excess ITO
  - Soak in acetone for at least 30 minutes (1 hour preferred)
  - Rinse off loose material (ITO) with Acetone.
  - Ultrasonic for ∼15 seconds.

    If edge tearing is an issue, try reversing the order of the previous two steps. Avoid allowing the surface of the substrate dry between steps, or when the substrate is being transported (i.e., not submerged in acetone). Allowing the surface to dry will result in re-adhesion of the lifted ITO flakes and particles.
- AMD clean (remove left over photoresist and source/drain material)
- Dehydrate on hotplate
  - 115 °C
  - 3 minutes
- Test devices and circuits

Appendix B. VerilogA Code

```
// VerilogA for ahdlcustom, transparent_transistor, veriloga
//
//
// Transparent Transistor - Level 1
//
//
//
//
`include "constants.h"
`include "discipline.h"

    module tt_level1(vdrain, vgate, vsource);
    inout vdrain, vgate,vsource;
    electrical vdrain, vgate, vsource;
    parameter real W = 1u from (0:1);
    parameter real L = 1u from (0:1);

    /* variable for overlap capacitance (parasitics) */
    parameter real GSDoverlap = 2u from (0:1);

    /* note: CSDoverlap is only for layout,  */
    /* makes no numerical difference, so not */
    /* used here (aside from contact         */
    /* resistance, assumed negligible)       */

//
// visible variables
//
        real    vds, vgs, vd, vg, vs;
        real    id, id_polarity;
        real    qgs, qgd, Cgs, Cgd;
        real    c0, c1, c2, c3, c4, c5, c6;
        real    von, tox, Kox;
        real    Eo,Cins;

analog begin

@ ( initial_step or initial_step("static") ) begin

//
//Process Parameters
//
```

```
//************************************************************************
//** NOTE: Define Uave coefficients for Veff_defined >> Veff_simulated, **
//** i.e., define (manually add data points if needed) polynomial fit   **
//** "accurate" to Veff =~ 100 V for simulator use of Veff = 40 V       **
//************************************************************************

    //Eric Sundholm (6/4/2009) CURRENTLY USING
    //090604F2
    c0 = -0.1861;
    c1 = 1.5903;
    c2 = -0.0447;
    c3 = 0.0007;
    c4 = -6E-6;
    c5 = 3E-8;
    c6 = 5E-11;
    von = 1;
    tox = 0.1E-6;  /*dielectric thickness, 100nm */
    Kox = 3.9;

    // SECOND SET OF TFT VARIABLES HERE
    /*
    c0 = ;
    c1 = ;
    c2 = ;
    c3 = ;
    c4 = ;
    c5 = ;
    c6 = ;
    von = ;
    tox = ;
    Kox = ;
    */

// For calculations, do not edit
    Eo = 8.85E-12;   /* Farads/meter */
//
// Insulator Capacitance
//
    /* Farads/cm^2 (*10000 to change meters^2 -> cm^2) */
    /* cm^2 to properly cancel units with mobility     */
    Cins = (Kox*Eo)/(tox*10000);

    /* parasitic capacitors */
    Cgs = (Kox*Eo/tox)*W*(GSDoverlap+L/2);
    Cgd = (Kox*Eo/tox)*W*(GSDoverlap+L/2);
```

```
end

    vd = V(vdrain);
    vs = V(vsource);
    vg = V(vgate);

//
// swap definitions of drain and source depending on "polarity" of vds
//

    if (vd-vs >= 0) begin
        vds = vd-vs;
        vgs = vg-vs;
        id_polarity = 1;
    end

    else begin
        vds = vs-vd;
        vgs = vg-vd;
        id_polarity = -1;
    end

//
// channel component of drain current.
//

    //
    // cutoff
    //

        if (vgs <= von) begin
        id = 0;
            end

    //
    // linear region.
    //

        else if (vds < vgs - von) begin
            id = (W/L)*Cins*
            ( (c0/2)*(pow(vgs-von,2)-pow(vgs-von-vds,2))
            + (c1/3)*(pow(vgs-von,3)-pow(vgs-von-vds,3))
            + (c2/4)*(pow(vgs-von,4)-pow(vgs-von-vds,4))
```

```
            + (c3/5)*(pow(vgs-von,5)-pow(vgs-von-vds,5))
            + (c4/6)*(pow(vgs-von,6)-pow(vgs-von-vds,6))
            + (c5/7)*(pow(vgs-von,7)-pow(vgs-von-vds,7))
            + (c6/8)*(pow(vgs-von,8)-pow(vgs-von-vds,8)) );
            end

    //
    // saturation region
    //

        else begin
            id = (W/L)*Cins*
            ( (c0/2)*pow(vgs-von,2)
            + (c1/3)*pow(vgs-von,3)
            + (c2/4)*pow(vgs-von,4)
            + (c3/5)*pow(vgs-von,5)
            + (c4/6)*pow(vgs-von,6)
            + (c5/7)*pow(vgs-von,7)
            + (c6/8)*pow(vgs-von,8) );
            end

//
// paracitic capacitors
//

    qgs = Cgs * V(vgate,vsource);
    qgd = Cgd * V(vgate,vdrain);

//
// current calculation
//
    I(vdrain, vsource) <+  id_polarity*id + 1e-10*V(vdrain,vsource);
    // drain current + a small conductance to aid in DC convergence
    // results in I_off = 1e-10 A, or 1e-10 A being the noise floor

    I(vgate, vsource)  <+  ddt(qgs);
    I(vgate, vdrain)   <+  ddt(qgd);

end
endmodule
```

Appendix C. Dielectric Charge Trapping

When performing a $log(J)$-ξ test on a MIM capacitor fabricated with a PECVD SiO_2 dielectric, it is common to observe a negative curvature roll-off in the high current density region dominated by Fowler-Nordheim tunneling. Figure C.1 shows an example $log(J)$-ξ curve of an excellent quality 90 nm PECVD SiO_2 on a heavily-doped silicon substrate. Note that the $log(J)$-ξ leakage behavior for this curve is nearly identical to that of curve A, Fig. 6.9, which employs a SiO_2 thermally grown on the same heavily-doped silicon substrate, except that the negative curvature roll-off effects are more pronounced for the PECVD dielectric.

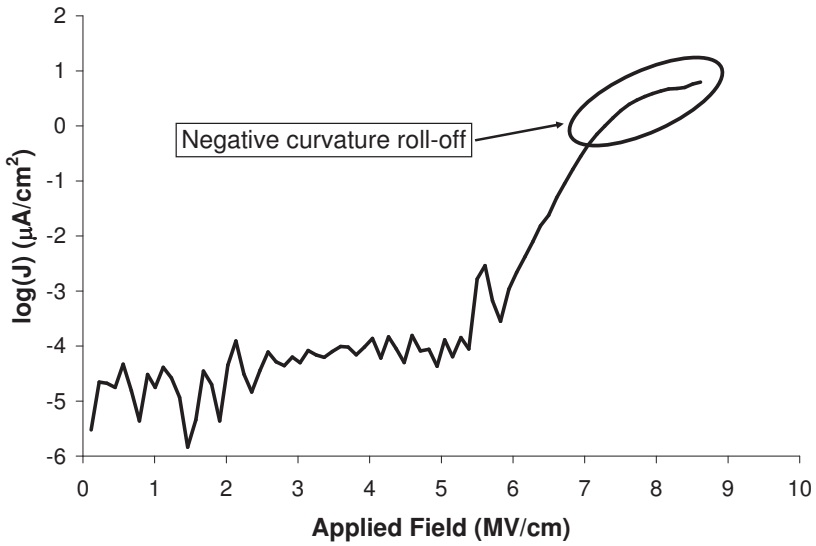

Figure C.1: $log(J)$-ξ characteristics of an excellent quality 90 nm thick PECVD SiO_2 on a heavily-doped silicon substrate highlighting a negative curvature roll-off at a high applied electric field.

As shown in Fig. C.2, replotted from curve B, Fig. 6.11, the negative curvature roll-off leads to a discrepancy between the measured (with roll-off) and simulated (without roll-off) $log(J)$-ξ leakage curves. Initial attempts to account for this discrep-

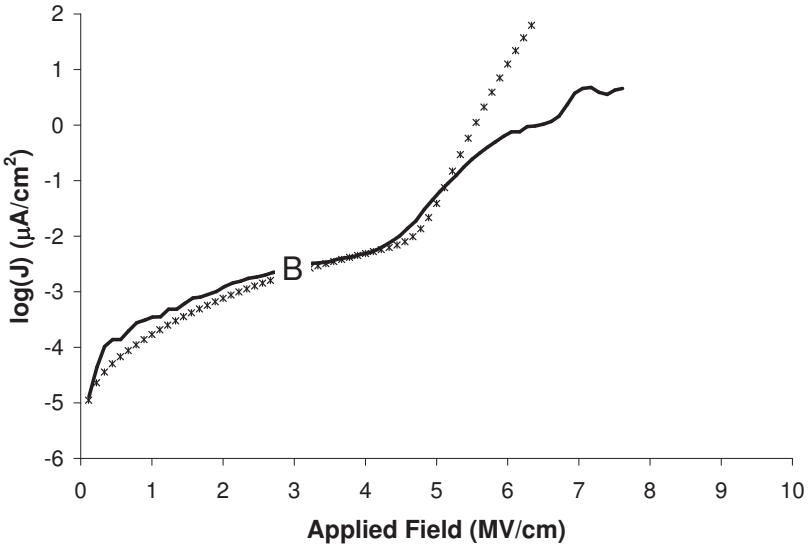

Figure C.2: Replotted $log(J)$-ξ leakage characteristics of curve B from Chapter 6.

ancy involved modifying the Fowler-Nordheim tunneling equation, Eq. 6.3, to include series resistance. This is accomplished by replacing ξ in the original Fowler-Nordheim equation with $(\xi - J_{FN} \cdot \rho_{SERIES})$ in the modified equation [53, 60, 61, 66], i.e.,

$$J_{FN} = \frac{q^3 \cdot (\xi - J_{FN} \cdot \rho_{SERIES})^2}{16 \cdot \pi \cdot \hbar \cdot \phi_B} exp \left[\frac{-4 \cdot \sqrt{2 \cdot m^*} \cdot \phi_B^{\frac{3}{2}}}{300 \cdot \hbar \cdot q \cdot (\xi - J_{FN} \cdot \rho_{SERIES})} \right], \quad \text{(C.1)}$$

where J_{FN} is the Fowler-Nordheim tunneling current density in A/cm^2, ξ is the applied electric field in V/cm, ρ_{SERIES} is the series resistivity in Ω-cm, q is the charge of an electron in coulombs, $\hbar$ is the reduced Planck's constant (i.e., $\frac{h}{2\pi}$) in joule-seconds, ϕ_B is the dielectric barrier height in joules, and m^* is the effective mass of an electron in SiO_2 in kg. The value of 300 in the denominator of the exponential in Eq. 6.3 is changed from a value of 3 in the original Fowler-Nordheim equation to accommodate the use of V/cm as the units for the applied electric field, as opposed to V/m.

Figure C.3 is the result of using Eq. C.1 in place of the original Fowler-Nordheim equation, in conjunction with Ohmic and SCLC conduction mechanisms, for simulation of the $log(J)$-ξ curve shown in Fig. C.1 and of the $log(J)$-ξ curve B shown in Fig. 6.11. As indicated in Fig. C.3, the correlation between measured and simulated $log(J)$-ξ curves is much improved with the inclusion of series resistance. However, the simulation requires for both curves shown in Fig. C.3 that $\rho_{SERIES} = 1 \times 10^{12}$ Ω-cm. No physical justification for a series resistivity of this magnitude could be found.

Further work to clarify the physical mechanism responsible for the negative curvature roll-off behavior witnessed in Fig. C.2 involved obtaining multiple (i.e., sequential) $log(J)$-ξ curves. Figure C.4 illustrates three such $log(J)$-ξ sweeps for a MIM capacitor fabricated with PECVD SiO_2 and exhibiting a pronounced negative curvature roll-off. Note that the basic $log(J)$-ξ shape changes dramatically in going from sweep 1 to sweep 2. However sweep 2 and 3 are very similar. The negative curvature evident in the high field portion of sweep 1 completely changes its inflection to positive curvature in transiting from sweep 1 to sweep 2. Negative curvature in a $log(J)$-ξ curve is evidence of negative charge (i.e., electron) trapping. The change to positive curvature suggests that traps have been filled. Thus, the trend shown in Fig. C.4 is evidence that the negative curvature roll-off phenomenon sometimes measured in the $log(J)$-ξ curves may be a consequence of electron trapping within the dielectric.

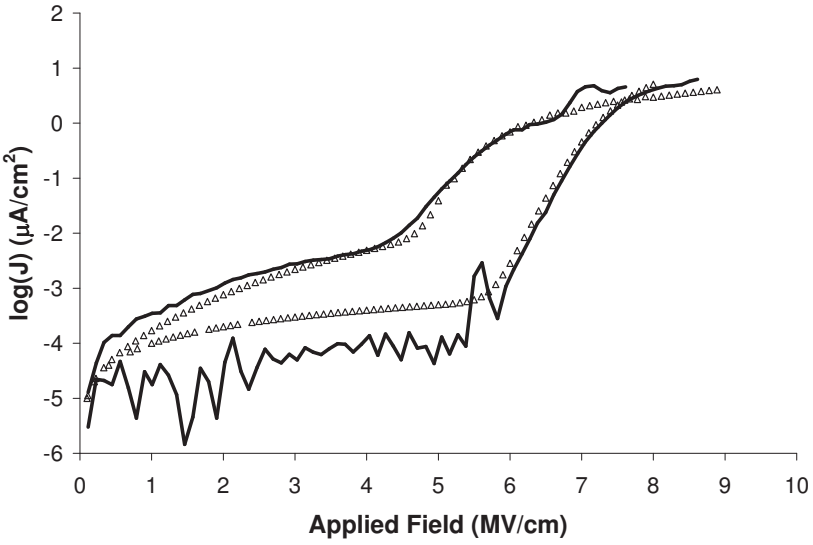

Figure C.3: Comparison of measured (solid lines) and simulated (triangles) $log(J)$-ξ curves from Fig. C.1 and from curve B of Fig. 6.11. The simulations performed employ Fowler-Nordheim tunneling with series resistance in an attempt to explain the negative curvature roll-off discrepancy evident in Fig. C.2.

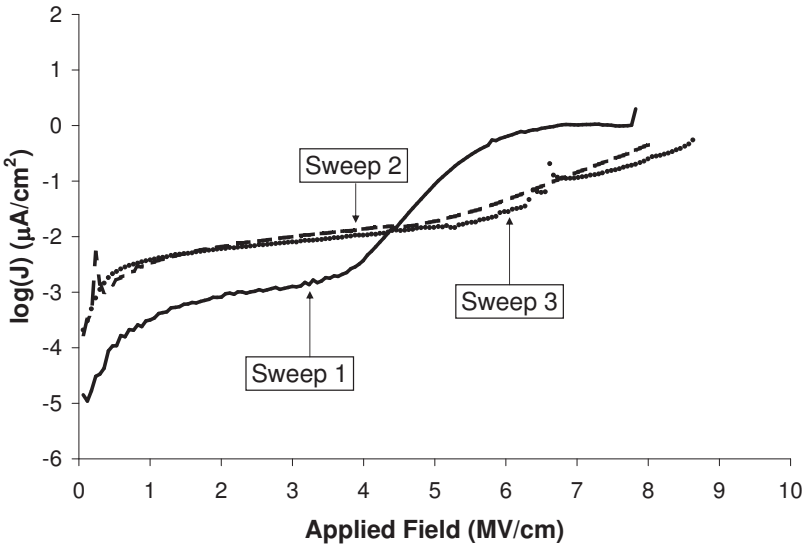

Figure C.4: Sequential $log(J)$-ξ sweeps on a MIM capacitor fabricated with PECVD SiO_2 exhibiting the negative curvature roll-off phenomenon.

Note that the onset of Fowler-Nordheim tunneling occurs at a higher applied electric field for sweeps 2 and 3 than for sweep 1. Also, the Fowler-Nordheim tunneling regime is not as steep for sweeps 2 and 3 compared to that of sweep 1. These differences between sweep 1 and sweeps 2 and 3 are attributed to electron trapping in the dielectric, as described in the following. Figure C.5 illustrates that a build up of trapped electrons (i.e., negative space charge) results in negative band bending in the insulator energy band diagram. This negative curvature in the energy bands acts to increase the dielectric barrier thickness, $t_{BARRIER}$, which in turn, suppresses Fowler-Nordheim tunneling. Thus, if a dielectric has a significant density of empty traps (e.g., the PECVD SiO_2 featured in Figs. C.1, C.2), then significant electron trapping results in negative curvature band bending, which then leads to a suppression of Fowler-Nordheim tunneling and to the negative curvature roll-off phenomenon seen in the $log(J)$-ξ curves.

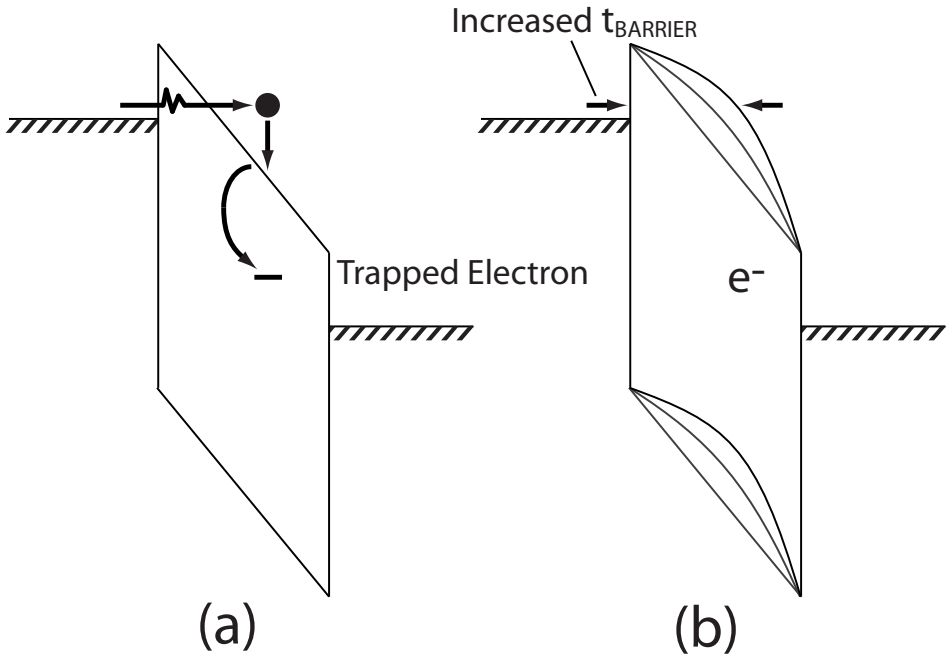

Figure C.5: Energy band diagrams illustrating electron trapping within the insulator for a metal-insulator-metal (MIM) capacitor. (a) Fowler-Nordheim tunneling and subsequent electron trapping, and (b) increased tunnel barrier thickness due to the presence of negative space charge created by electron trapping within the insulator.