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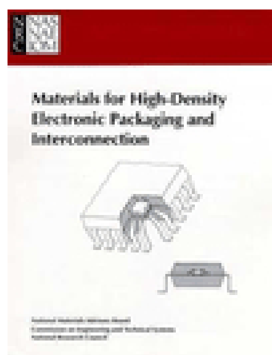

Materials for High-Density Electronic Packaging and Interconnection

Committee on Materials for High-Density Electronic Packaging, Commission on Engineering and Technical Systems, National Research Council

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Materials for High-Density Electronic Packaging and Interconnection

Report of the Committee on Materials for High-Density Electronic Packaging

National Materials Advisory Board
Commission on Engineering and Technical Systems
National Research Council

NMAB-449

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This report has been reviewed by a group other than the authors according to procedures approved by a Report Review Committee consisting of members of the National Academy of Sciences, the National Academy of Engineering, and the Institute of Medicine.

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Cover: Schematic cross section of a molded plastic leaded chip carrier (Courtesy of AT&T Bell Laboratories)

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Abstract

Electronic packaging and interconnections are the elements that today limit the ultimate performance of advanced electronic systems. Materials in use today and those becoming available are critically examined to ascertain what actions are needed for U.S. industry to compete favorably in the world market for advanced electronics. Materials and processes are discussed in terms of the final properties achievable and systems design compatibility. Weak points in the domestic industrial capability, including technical, industrial philosophy, and political, are identified. Recommendations are presented for actions that could help U.S. industry regain its former leadership position in advanced semiconductor systems production.

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Preface

What is packaging? The subject of this report is commonly referred to as electronic packaging, but the term "packaging" carries connotations that tend to trivialize the highly technical and critically important electronic context. Electronic packaging now goes well beyond physical protection and includes electric power distribution, signal transmission between integrated circuits, and, of growing importance, the removal of heat associated with the very high densities of circuit elements that are being achieved. Modern system performance is as much limited by these functions as by the operation of the integrated circuits. Thus, electronic packaging and interconnection are essential enabling technologies that underlie vital computer and other electronic applications. Success in integrating these enabling technologies into the nation's microelectronics efforts is directly related to how well the United States will succeed as a major competitive force.

The specific subject of this report is the materials employed in high-density electronic packaging and interconnection. Materials issues are closely coupled to other systems design factors, and all materials advances must be coordinated as the field progresses. A successful competitive position cannot be maintained without leading-edge materials engineering and science. Coordination of physical design, materials properties, and materials processing is essential. The competitive position of the United States in an area of the highest leverage is at stake.

This report focuses on first-and second-level packaging—i.e., the integrated circuit chip package and the printed circuit to which the chips are attached. The connectors, backplanes, cables, and other higher-level interconnect structures have been omitted because it was perceived that materials problems in these areas were less urgent. In addition, the higher interconnection levels are, at present, undergoing some degree of conversion from electrical to optical, and optical interconnections are outside the scope of this study. The committee believes that optical interconnection is a very important technology and will certainly spread to the board level and beyond in the course of time. Optical technology has many advantages and could depart radically from the geometries required of "wire"-based systems. An additional study of optical interconnection is strongly recommended [1].

The literature on electronic packaging has recently been unified through publication of an authoritative monograph[2]. This handbook gives a coherent, balanced discussion of all aspects of electronic packaging and interconnection, with materials considerations appropriately integrated into physical design. In addition, the ASM INTERNATIONAL has published a

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comprehensive document on packaging, its first that is directed specifically to electrical and electronic materials[3]. Concurrently with the preparation of the present report, a group has been working on a related project sponsored by the National Security Industrial Association (NSIA). Dr. Bruce E. Kurtz, chairman of the NSIA Electronics Packaging/Interconnection Task Force, has kindly provided the committee a draft of this material which was found to be highly valuable. The materials and processing interaction in packaging is effectively covered in a recent McGraw-Hill publication[4].

Anticipating that further advancements in IC technologies would be hampered by limitations of currently available materials and processes, the Department of Defense and National Aeronautics and Space Administration requested the National Materials Advisory Board to examine the situation. A committee was appointed that included representation from industry, university, and research institutions and provided a balance of experience and knowledge in chemistry, polymer science, ceramics, materials science, electronics, and physics. A biographical sketch for each committee member is found in Appendix G.

A major objective of this study was to assess the current state of the art in packaging and to anticipate the requirements for new materials and processes for packaging highly integrated semiconductor chips and future designs, particularly for military and space applications. The committee was asked to assess the existing capability for packaging electronic components and existing limitations, identify probable needs in new materials and processing techniques to accommodate new package designs, determine where superconductor breakthroughs may be properly employed, identify the electrical, thermal, and mechanical properties of materials needed for the newly designed chips and interconnects, recommend where R&D efforts should be directed toward developing the needed materials and systems for future electronic packages, and, to the extent possible, assess the U.S. position relative to that of world competition—i.e., Japan, Europe, and others. Although the report is directed primarily to the sponsoring agencies, it is presented in a broad-based manner for a wider readership, to help them understand the current situation and gain a perspective on what actions are needed to enhance the domestic capability to compete in a global market. A discussion of nontechnical issues was not in the scope of the committee's task, however, thoughts on such issues were included to explain why certain actions are advised to help improve the industry's competitive position.

[1] Photonics: Maintaining Competitiveness in the Information Era. Panel on Science and Technology Assessment. Washington, D.C.: National Academy Press, 1988.
[2] Microelectronics Packaging Handbook. Rao R. Tummala and E. J. Rymaszowski, editors. New York: Van Nostrand Reinhold, 1989.
[3] Electronic Materials Handbook, Vol. 1, Packaging, M. L. Minges, technical chairman. Materials Park, Ohio: ASM INTERNATIONAL, 1989.
[4] principles of Electronic Packaging, Design and Materials Science. D. P. Seraphim, C. Lasky, and Che-Yu Li, editors. New York: McGraw-Hill, 1989.

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Acknowledgments

The committee is grateful to a number of individuals who provided extensive background materials for committee use. Experts were invited to committee meetings to present current data on specific topics of concern. The following are thanked for their generous participation:

MEETING 1

R A. Boudelaise of Westinghouse Defense and Electronics Center discussed Phase I of MANTECH packaging needs.

J. L. Heaton of Sanders Microelectronics Center discussed MMIC packaging needs.

M B. Ketchen of IBM's, T. J. Watson Research Center discussed Josephson packaging technology.

P. V. McEnroe of Digital Equipment Corporation discussed wafer-scale integration.

M. C. Peckerar of the U.S. Naval Research Laboratory presented an overview of VHSIC packaging needs.

R. Smolley of TRW's, Electronics and Technology Division discussed VHSIC Phase II, advanced development of packaging needs.

R. J. Willis of Floating Point Systems, Inc., discussed packaging of massive passive parallel systems.

MEETING 2

L. E. Cross of Pennsylvania State University discussed inorganic packaging materials and interconnects.

D. C. Hofer of IBM's, Almaden Research Center discussed organic packaging materials from a customer's viewpoint.

R. Jensen of Honeywell Sensors and Signal Processing Laboratory discussed copper-polyimide thin film interconnection technology for IC packaging.

J. Kim of IBM's, T. J. Watson Research Center discussed IBM's thermal conduction module.

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J. A. Nelson of Unisys Corporation was unable to attend but submitted comments on packaging materials needs and challenges for large computers.

R. M. Rivett of Edison Welding Institute discussed microelectronics metals joining.

R. M. Rosenberg and J. F. Strange of DuPont discussed materials for packaging and interconnects from a vendor's viewpoint.

MEETING 3

J. E. Anderson of Ford Motor Company discussed materials for electronic packaging in automotive applications.

J. S. Browning of Sandia National Laboratory discussed radiation effects in microelectronics.

A. Christou of the U.S. Naval Research Laboratory discussed gallium arsenide interconnects.

A. Huang of AT&T Bell Laboratories discussed optical digital computers, the devices and architecture.

A. Husain of Honeywell Sensors and Signal Processing Laboratory discussed trends in optical interconnect technology.

W. B. Jones of Sandia National Laboratories discussed performance and metallurgy of aluminum metallization interconnects.

L. M. Levenson of General Electric Company presented the highlights of the Santa Barbara Engineering Foundation Conference of 1988.

The government liaison representatives are thanked for participating in committee discussions and providing valuable support materials and data for committee use. D. R. Franck (President of Empire Planning Group, Ltd.) is thanked for undertaking an assignment for the committee to provide data on systems technology projections through 1994. In addition, some specific industry data in Appendix B are taken from a report, *Chip Carriers and Other Integrated Circuit Packages: A Review and Update, 1988*, (copyright 1988), with the kind permission of James D. Welterlen, President of Welterlen, Inc. These tables illustrate the complexity of the chip encapsulation picture, but they cover only a fraction of the field covered in Welterlen's annual reports.

The committee is indebted to committee member J. C. Logue, whose years of packaging experience at IBM was invaluable in its deliberations by providing technical insight and details for the report. The chairman acknowledges with thanks the extra efforts of Mr. Logue for his assistance in coordinating various inputs to the report. The committee members are thanked for their dedication and for their patience during the lengthy task of

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preparing and revising the report to ensure its accuracy and currency. Particular thanks go to the members of the committee who served as chapter or section coordinators for assembling pertinent facts for various parts of the report and presenting the data in a timely, open-minded, and professional manner. Specifically, Paul Penfield and J. C. Logue coordinated Chapter 3, C. A. Neugebauer coordinated Chapter 4, and Jack Hilibrand contributed heavily to Chapter 7. Discussions in the report are based on data compiled through Spring, 1989.

Special thanks are owed to colleagues at AT&T Bell Laboratories in connection with Chapter 4. D. W. Johnson, L. T. Manzione, and J. M. Segelken contributed important sections and provided expert advice on packaging issues generally, and L. L. Blyler, Jr., and L. D. Loan consulted extensively on this material. M. John Drobny provided the professional renderings for the report figures. Special thanks go to Shiro Matsuoka for his invaluable assistance as technical advisor to the committee. Ms. Irene M. Fedun greatly assisted in coordinating and assembling the preliminary report draft, efforts which are appreciated by all concerned.

Finally, the committee gratefully acknowledges the untiring support of George Economos, senior program officer of the National Materials Advisory Board, and his secretary Ms. Aida Neel, in all stages of report preparation.

DAVID W. MCCALL CHAIRMAN

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Executive Summary

Electronic packaging has become an important element in electronic systems and may very well be a critical pacing feature in the future. Modern packaging technology embodies a host of materials science and technology issues and necessitates an integrated design approach that includes packaging considerations from the very outset. Integrated circuit performance can be limited or enhanced by packaging features, and the designer no longer has the latitude to ignore such considerations until the electronic portion of the design is complete. Packaging, with all its implied materials issues, is a basic design feature. The materials of packaging and interconnection that are intrinsic to the design effort are the subject of this report. The ability to incorporate these issues into microelectronics products will be a key factor in maintaining this nation's competitive position in the world market for advanced electronics.

Electronic systems needed in the next few years will require unprecedented packaging technology. The rapid advances in integrated circuit chip capabilities will continue to increase demand for enhanced interconnect capability as regards numbers of connections (pinouts), pinout configuration, heat removal, signal rise time, signal transit time, power lead inductance, power supply current, and environmental protection. The projected evolution of chip parameters is presented in the format suggested by scaling theory for three families of chips [bipolar, CMOS, and GaAs], and the concomitant implications for packaging and interconnection are discussed. Appendix A contains a list of many special terms used in this report. No attempt is made to explain all terms commonly used in the industry. For individual chips, there will be hundreds of pinouts, tens of watts, and subnanosecond rise times in the 1990s. Clearly, interconnect structures will require considerable enhancements to translate these chip capabilities to system performance. Heat dissipation in thousands of watts and power supply requirements of thousands of amperes are projected at the board level. Special physical design problems arise with very-high-frequency and very high-speed circuits. There is concern that the United States is relying too heavily on foreign sources of packaging and interconnection materials for high-density electronic circuitry.

The United States has lost significant market share in advanced chip technology, and the process continues. As domestic production is lost (e.g., in DRAMs), advanced packaging and interconnection strategies will be handicapped by reluctance of foreign chip makers to supply ICs in unpackaged or other non-standard forms. Printed wiring board (PWB) technology continues to evolve with the introduction of efficient surface-mount technology, finer

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patterns, greater numbers of signal layers, and improved board resins for greater dimensional control. Forty-layer boards have been achieved. PWBs will certainly be important for many years to come, but their limitations in very-high-density electronics will have to be addressed in terms of new design strategies in which materials innovations will play a key role.

Packaging is now approaching a turning point at which single-chip packages cannot be assembled directly onto conventional circuit boards without impairment of performance. A new level of packaging, the multichip module (MCM), is coming into prominence. MCMs consist of inorganic base layers, to provide power, ground and decoupling capacitances, and signal interconnect patterns fabricated of high-conductivity metals and low-dielectric-constant organic polymer dielectrics. The individual chips are assembled on top, either in unencapsulated form or in low-impedance single-chip packages. The signal interconnection density achievable is very high, owing to the fineness of the patterns. Two layers of MCMs can replace dozens of layers in conventional PWBs. Materials support for MCM designs must be strongly encouraged in the United States.

Materials issues emphasize both process and final property aspects of design, and material compatibility is a critical issue. Many different properties and compatibilities must be optimized simultaneously. Issues of importance include the following:

- coefficient of thermal expansion
- dielectric properties
- thermal conductivity
- electrical conductivity
- interfacial chemistry
- adhesion
- mechanical strength and toughness
- impact strength
- long-term stability
- purity (including absence of radioactivity)
- vapor permeability (especially water)
- corrosion
- metal migration
- process control and reproducibility
- process compatibility

The engineering-design-manufacturing process sequence is somewhat difficult to describe briefly while emphasizing materials factors. Discussing some specific packaging and interconnection materials (see Chapter 5) can give a flavor for the complex compromises that must be made. These systems include epoxies for encapsulation and PWBs, ceramic materials for packages and co-fired circuits, polyimides for dielectric layers, and more exotic materials, such as superconductors, synthetic diamond layers, and composites.

Beyond the domain of engineering, packaging and interconnection materials are strongly affected by business, organizational, and government policy issues. International competition presents implications in terms of economics and national security. These interacting business and government

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issues have much in common with many other high-technology areas, but packaging materials is a field in which the organizational problems are important, competition is fierce, and the financial consequences of losing out are massive. The United States has already lost consumer electronics and the entire computer market could follow. Packaging is one of the essential ingredients in the future U.S. position.

In certain respects, the United States is poorly positioned in regard to materials employed for packaging and interconnection. In the sequence of raw materials, intermediates, formulated materials, completed piece parts, and assembled modules and systems, materials and information move from one company to another in a highly incomplete and imperfect way. The sequence is fragmented, and the technology is migrating to other countries, leaving U.S. manufacturers dependent on foreign supply houses. Some form of domestic supply chain that accomplishes the advantages of a vertically integrated corporation is urgently needed.

A further problem exists in connection with government-funded research and development. The most substantial source of federal money is the Department of Defense, and many important initiatives have received timely funding from that agency. Unfortunately, electronic packaging of military systems has evolved along lines that differ significantly from computer, consumer, automotive, and other electronic subareas. There are some hopeful signs of rationalization, but much remains to be done.

In recent years, many consortia have been formed to address problems faced by the United States in regard to international competition in technological matters. Groups of companies and other organizations come together to address common issues in a coordinated way and to pool resources. A consortium specifically addressed to materials for electronic packaging and interconnection could be an effective approach to some of the problems faced. Coupling to system design and engineering and the involvement of first-class engineering talent are essential features. An alternative to an independent consortium on packaging might consist of an expanded emphasis on packaging and interconnection by existing consortia.

The United States has enormous intellectual resources in the university system, and it will be important to bring this potential to bear on the critical area of electronic packaging. Coordination of efforts of the various relevant university engineering and science departments will not be easy for this interdisciplinary field. Coupling of university programs to industrial design, development, and manufacturing projects in productive arrangements will require creative management. Similarly, involvement of national laboratories and other organizations also must be implemented. Issues of organizational culture complicate communication among the potential contributors. The National Science Foundation's program on engineering research centers is a recent approach to finding a useful format, but it is directed to support large centers. Smaller grants that encourage materials innovations and industrial collaboration are needed.

The United States has lost significant segments of the electronics market in recent years. The future position of the United States as a world

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power and the U.S. standard of living depend on a broadly-based response to foreign competition. Any response that does not include aggressive materials and packaging programs will fail to regain and sustain the U.S. position. Both domestic comfort and national security are at stake.

The committee's conclusions and recommendations regarding specific areas follow.

- National policies. Antitrust laws still wield considerable influence in U.S. business circles. The need for strict interpretation of the laws has been largely eliminated by the growth in overseas competition, which will prevent any U.S. combine from raising prices to the disadvantage of the public. Modernization of these laws should be undertaken with emphasis on the features that affect the competitivness of U.S. corporations in critical world markets.

The introduction of advanced packaging technology and materials in U.S. industry could be facilitated by selectively removing antitrust restrictions on "buying cooperatives." Specifically, if U.S. companies were permitted to aggregate demand for new products (e.g., packaging materials), U.S. producers would be stimulated to risk their capital and develop the needed manufacturing capability. The committee concludes that a major impediment to U.S. competitiveness in computer and other electronic systems is the unwillingness of domestic material suppliers to invest capital for research, development, and production in long-term ventures. By aggregating market demand (as is done in Japan), U.S. electronics manufacturers would provide a more attractive market that would stimulate production of advanced materials and build a self-sustaining market. This would help compensate for systemic advantages of similar actions enjoyed by foreign materials companies.

Foreign companies also enjoy low-interest loans that encourage greater patience in market development. Some form of selective capital encouragement should be considered as a part of a broadly-based U.S. strategic plan to revive, sustain, and create critically-important base technologies. This could be done at the state level as well as on the federal level. It is difficult to overstate the need for actions that will encourage the long-range research and development necessary to provide the technology for future industries. Low-interest money is needed. Tax credits for research and development are an alternative approach that should be considered.

In an era of emphasis on short-term financial results, it is important to provide incentives for long-term investment in technologies that will build wealth for the nation. Although it has not been discussed widely, the much-admired U.S. corporate research and development laboratories are increasingly under pressure to shorten their sights and turn over quick profits. The current frenzy for mergers, acquisitions, and other forms of corporate churning is destabilizing and destroying the climate for long-range technical development. Some form of legislation that would discourage these practices seems desirable. Legislative solutions by their nature are long term. Thus, it is all the more important that a national strategiic program be undertaken to find remedies for our present malaise. The problems do not show signs of self-cure.

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The committee discussed some changes in regard to patent procedures that could enhance U.S. competitiveness in the packaging materials area. Legislation would not be required for a system that gives priority on Patent Office and Patent Court dockets for submissions in the packaging area. (This already has been done for high-temperature superconductivity.) The ad hoc nature of this approach is a negative aspect. Legislation to allow the formation of patent pools and licensing arrangements by removing antitrust constraints for a period of 10 to 20 years has been proposed. As U.S. corporations become owned by and allied with foreign companies, legislative and procedural efforts to favor U.S. firms become awkward and difficult to administer.

- User consortium. The committee exhibited considerable enthusiasm for an industry-led consortium of packaging-materials users, with the objective to develop a stronger U.S. base of packaging-materials suppliers. This consortium would develop materials requirements and materials application technology, and would cultivate domestic sources of supply. The analogy with Sematech, the U.S.-based consortium aimed at integrated circuit process equipment, is strong, and the term "Sepatech" was coined for purposes of discussion among committee members. Table 1 illustrates the analogy.

Table 1 Analogy of U.S.-Based User Consortia

Parameter	Sematech	"Sepatech"
Intended to motivate	Equipment suppliers to integrated circuit manufacturers	Chemical suppliers, compounders, and other materials suppliers
Set up by:	Chip makers	System companies using packaging and inter-connection technology
Activity:	Prototype and build leading-edge parts, working with equipment suppliers to integrated circuit manufacturers	Perform materials and process evaluation, build some demonstration systems, and establish sources of supply
Vehicles for activity:	Memories (advanced DRAM and SRAM	Advanced work stations
Full-scale manufacturing by:	US Memories, Inc., employing the apparatus, materials, and processes developed	System houses employing materials and processes

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The consortium approach offers an increasingly acceptable way for manufacturers to pool their resources and aggregate their markets at a precompetitive stage. The approach places responsibility and control in the hands of the user industry and, therefore, ensures development along relevant paths. Financing must be substantially industrial ("earnest money"), but government investment can significantly encourage and facilitate establishment of the combine. Indeed, government funding at some level is probably essential and justified.

Consortia are controversial, and there is a lot to be learned in their organization, strategic objectives, and operation. Clearly, success depends on the participating organizations, which must provide quality people at all levels and viable long-term career paths for individuals. The committee is aware that consortia are subject to diverse forms of criticism, but the consortium approach is a positive mechanism to relieve the problems of U.S. industrial fragmentation. There are not many readily implementable alternative approaches.

- Military packaging. The packaging of integrated circuits for U.S. military systems must be hermetic, which has caused military electronics systems to lag considerably in terms of overall capabilities. The committee urges that alternative means be found to allow military hardware to move into the mainstream of electronic packaging, while still preserving reliability over long periods in difficult environments. Some study programs are under way in specific areas (e.g., silicone gel coatings), but a broadly-based action group should confront the issue and initiate studies that will lead to needed change. Although it is possible to obtain high levels of performance under hermetic constraints, the committee believes that pursuit of other options is a promising approach that should be encouraged.
- Industry-national laboratory-university coupling. Although systems manufacturers have been very active in work on packaging and interconnection materials and structures, relatively little activity in this area is evident in universities and the national laboratories. The committee feels that interconnection and packaging are regarded as insufficiently exciting by many members of the academic community. Some means is needed to stimulate university work in the area. The National Science Foundation's Engineering Research Center program would be well suited for establishing a close coupling of industrial scientists and engineers as an explicit part of the basic format. A program of smaller grants, similarly structured, could be highly useful. Also, coupling of national laboratory talent in the area should be pursued. Clearly, new and innovative means must be found to focus more of the considerable U.S. technical power on the issues electronic packaging.
- Specific materials for support. The following specific materials and process areas are recommended for support in connection with electronic packaging and interconnection. In any such list, there is the danger of important omissions, statement of the obvious, and possible emphasis on areas

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that lie close to the interests of the committee members. The following list had general support:

1. Present mainline materials should be pursued to bring U.S. capability up to a position of world leadership. Briefly, this includes copper, gold, and aluminum metallization with progress on high reliability in high current density; alumina and aluminum nitride, and other ceramic processing for preparation of advanced interconnect details; further development of epoxies for encapsulation, board resins, and adhesives; and development of polyimides and other high-temperature polymers for substrates, interlayer dielectrics, and other uses. Benzocyclobutanes are a very promising class of low dielectric constant polymers that are beginning to appear in electronic products.
2. Glass-ceramic substrate compositions that can be co-fired with copper are viewed as an area of the highest priority. Much work has been done, but the problem has not been solved.
3. Low-dielectric-constant materials and interlayers are becoming increasingly important because signal transit time limits circuit performance. Polymeric materials are available with electric permittivity as low as 2, but substantial development is needed to bring the many other properties and process variables into useful ranges. Ceramics seem less likely for low permittivity.
4. High-thermal-conductivity materials for packaging are needed. Composites offer advantages in this area. Thermoelectric cooling offers an alternative approach.
5. Materials for high-reliability encapsulation are extremely important. Hermetic structures are expensive and not entirely reliable. Silicone gels are currently under study, with promising initial results.
6. New solder compositions that are creep resistant would be valuable. Solder substitutes (e.g., anisotropically conducting polymers and ceramics) can be used for low-temperature assembly.
7. Composite materials can be employed to engineer combinations of properties not achievable with homogeneous substances.
8. Materials amenable to environmentally benign processing (e.g., dry processing, aqueous-based systems) will become increasingly important. Circuit-board cleaning is a major source of solvent loss to the atmosphere, which leads to ozone depletion and other ills.
9. High-temperature superconducting oxides are exciting candidates for interconnects. Chemical stability, electrical contacts, and other problems remain to be solved. (Bear in mind that copper, aluminum, and other metals also are considerably better conductors at liquid nitrogen temperature than at room temperature.)

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10. Synthetic diamond films offer great promise for mechanical protection, chemical isolation, and electrical insulation. The thermal conductivity is uniquely high.
11. The ability to design materials with thermal expansion tailored to the application is emerging and should be extremely important for interconnect structures.

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Chapter 1

Introduction

In the 40 years since the invention of the transistor, much attention has been given to silicon devices and integrated circuits (ICs). (See Appendix A for some terms and acronyms.) The impact of silicon electronics triggered the era of information processing and continues to produce amazing progress. The size of the circuit elements, the speed of their operation, the minimal power consumed, the cost per element, and the reliability of the circuits have improved dramatically. Today, silicon integrated circuits (chips), about the size of a fingernail, may contain a million transistors and cost a few dollars or tens of dollars (or hundreds in extreme cases), depending on the type and production level. There are good reasons to expect that some chips will contain a billion elements by the end of this century, and other characteristics will be improved as well. The recognition and praise lavished on silicon electronics over the past 4 decades is entirely justified, and the future remains promising.

And yet, integrated circuit chips are not useful until they have been woven into the fabric of interconnections and packaged. Packaging and interconnection (interconnects) provide structural support, mechanical and chemical protection, thermal management, power, ground, and signal transmission, including timing. The package must be durable and manufacturable and allow access for testing and repair. System performance in today's advanced systems is as likely to be limited by packaging and interconnection as by the chips themselves. In this report, high-density electronic packaging and interconnection will be described from the point of view of the materials of construction. The time frame of this report covers the present (1989) and the period in which present practice evolved and extends toward the end of the century. It is probable that reasonable predictions can be made extending for 5 or 10 years, but foreseeing system trends in the next century is highly speculative.

The many different sectors that encompass the field make it difficult to separate those to include or exclude. Consumer products, computer mainframes, supercomputers, telecommunications switching, personal computers, work stations, automotive components, and various military classes and other subareas all represent modern practice in the context of specific needs. Some consumer products use an aggressive packaging strategy. Very-high-frequency systems are often not high density. Advanced areas (e.g., computer mainframes) are inherently expensive and thus do not represent the leading

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edge of developments in other applications. Therefore, this report concerns itself with high-density packaging, in the sense of chips with large numbers of I/Os (inputs, outputs, or both) and the need for high-speed communication between chips.

Materials properties play a critical role in system performance and in manufacturing process effectiveness. The materials in use have evolved along with the physical design of the electronic systems, and today's structures represent engineering optimization of many factors. It is of little benefit to consider the properties of the materials outside the context of the application. Furthermore, the packaging and interconnection structures are composites containing many different materials in close proximity. Thus, interfacial properties and materials compatibility factors are often more important than bulk properties of the isolated materials. The dependence of the materials properties on the manufacturing process is also important.

Electronic packaging includes all structures that are designed to protect the integrated circuits, the attendant interconnections and the related circuitry from physical damage and any other impediment to achieving design performance. Interconnections include all means of communication (power, timing, data, results) from one integrated circuit to another or from one system of circuits to another. Interconnections on the chips themselves is not considered in this report, and interconnection by means other than electrical (e.g., photonic) are also excluded. Thus, the subject matter of this report concerns materials issues involved in electric circuits that run from the bonding pad of a chip through the chip package (if any) by means of a lead frame (or other fan-out to leads), through strip-line circuits on a substrate that may be connected by "vias" perpendicular to the plane of the substrate, and end at other integrated circuit bonding pads; it also includes other components or connectors that lead to other circuit boards, shelves, or frames. The physical nature of this packaging and interconnection hierarchy is indicated in Figures 1-1 through 1-7.

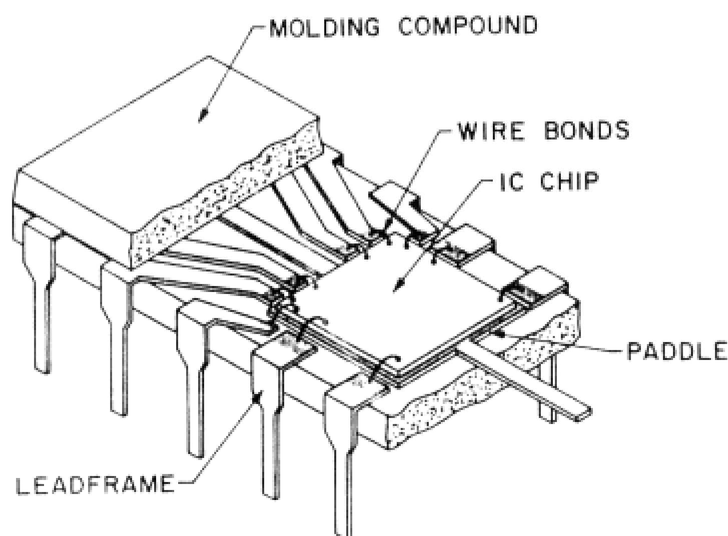

Figure 1-1
Cutaway view of a plastic DIP.

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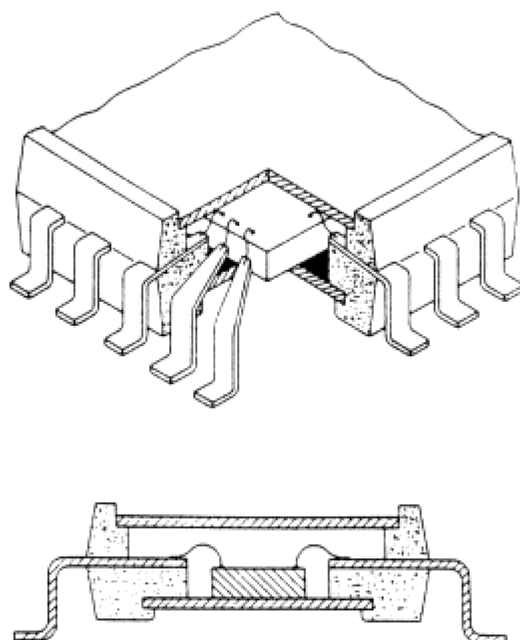

Figure 1-2
Schematic representation of a chip carrier. The chip is die bonded to the package. The signal, power, ground, and timing leads are wire-bonded to bonding pads on the chip. (A TAB inner lead frame could replace the wire bonds shown.) The exterior case may be premolded plastic (as shown) or ceramic.

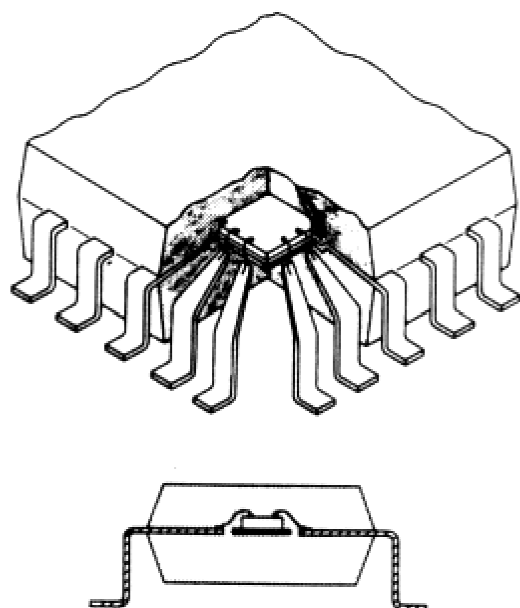

Figure 1-3
Molded plastic quad design or plastic leaded chip carrier (PLCC). The chip is diebonded to the paddle, which is connected to one or more ground leads. Signal, power, ground, and timing leads are connected by wire bonding pads. (A TAB inner lead frame can be used for this purpose.)

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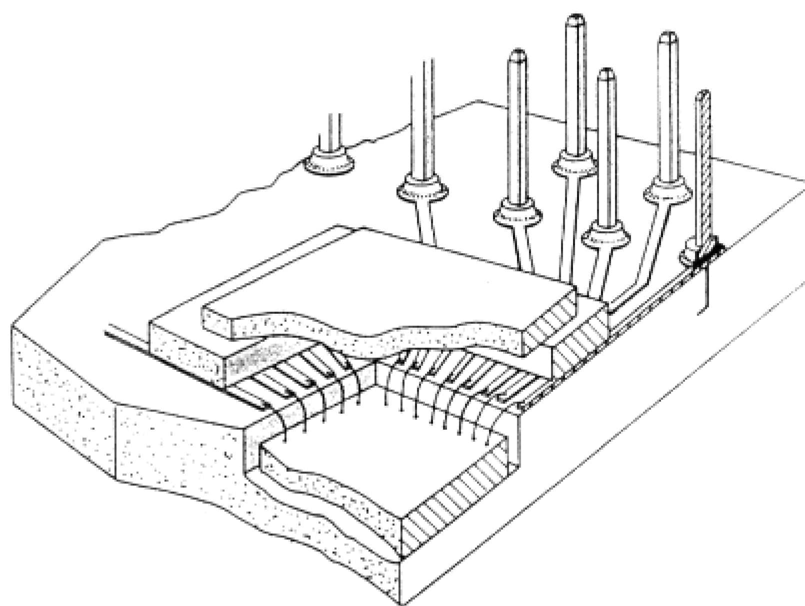

Figure 1-4
Cutaway of a PGA. The chip is die-bonded in the ceramic cavity and wire-bonded to the conductor fan-out, which is plated onto the ceramic. The outer end of each fanout finger is terminated onto a brazed pin, which is inserted into a through-hole on the PWB. This package can then be sealed hermetically with a lid (ceramic or metal). Similar packages with surface-mount leads are also employed. The device is shown inverted, and in use the active side of the chip would face the PWB (face down). The pins can be made to exit the ceramic on the opposite side (face up). The face-down option shown offers a favorable surface for heat-sink attachment.

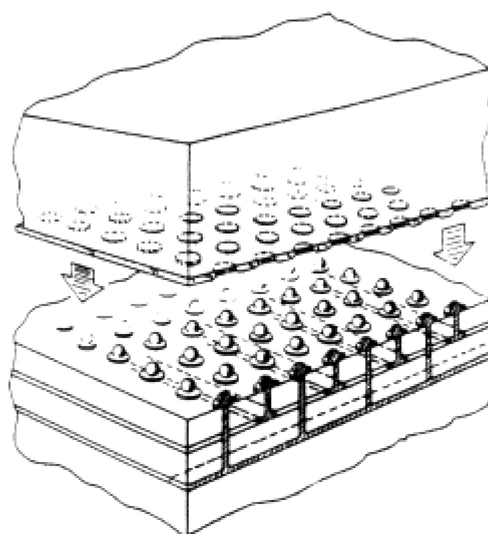

Figure 1-5
A field of solder bumps with device ready for mounting in C4 attachment (controlled collapse chip connection).

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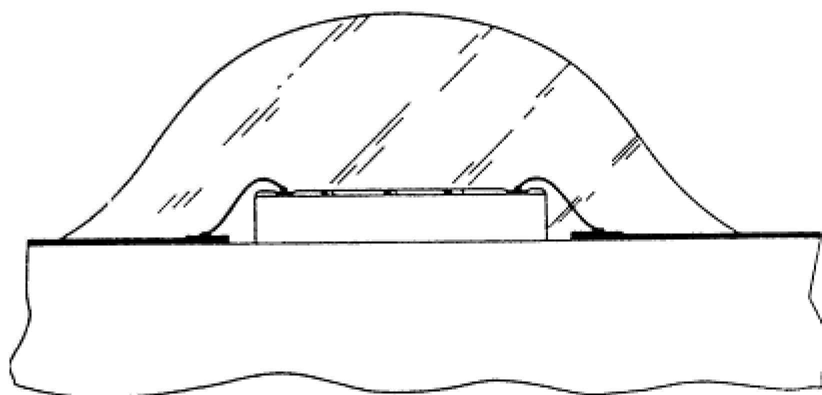

Figure 1-6
Direct chip attachment with protective polymer overcoat ("glob top").

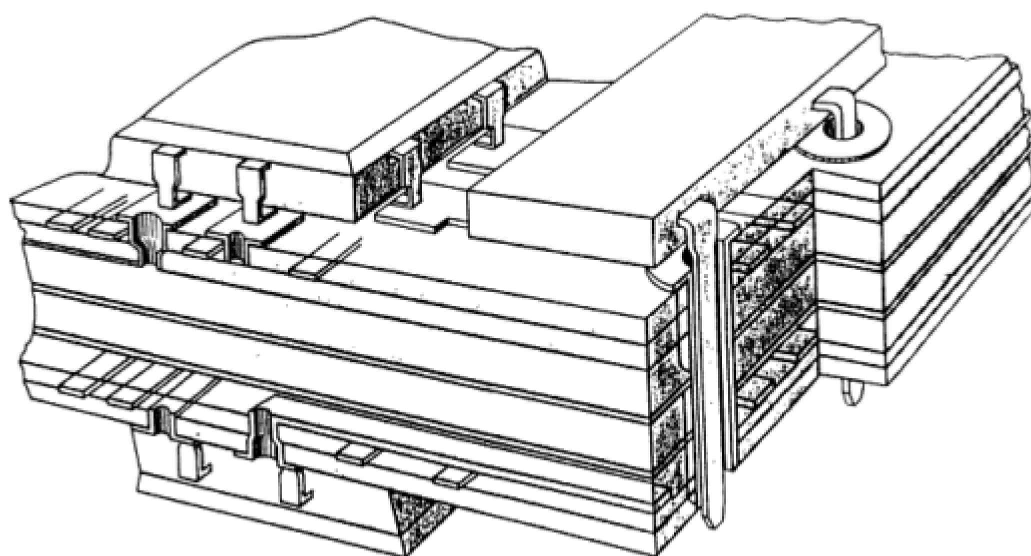

Figure 1-7
Printed wiring board circuit shown in cutaway to reveal inner connector layers and vias. A surface-mount device (left) and a through-hole device (right) are illustrated. Note that surface-mount devices can be mounted on both sides of the board (as shown) and do not consume valuable inner layer space with the through-hole.

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Integrated circuit chips are encapsulated in three types of packages: dual in-line packages (DIPs), chip carriers (CCs), and pin grid arrays (PGAs). Each option has many variants, and only the most elementary description is attempted herein. In terms of numbers of units manufactured, the DIP is most important. Chip carriers, however, are now being adopted widely and should rival DIPs in numbers within a few years. In monetary terms, DIP and CC packaging are comparable today, owing to the higher average cost per unit of the CC option. PGAs are very expensive and are employed only for chips with large numbers of external connections (I/Os).

The magnitude of the packaging market for 1987 is summarized in Table 1-1. The $2.0 billion packaging total is part of a total U.S. IC market of $9.3 billion. The 1987 market for printed circuit boards amounted to $5.1 billion, and edge connectors for boards amounted to $0.8 billion. Thus, the 1987 silicon cost of $7.3 billion was supported by more than $7.9 billion in packaging and interconnection. These numbers are imperfect, owing to the omission of captive production by equipment suppliers and other factors, but nonsilicon costs are comparable to and probably greater than silicon costs. The numbers also omit the hybrid market (U.S. 1987, about $4 billion), a substantial portion of which can be classified as interconnection and packaging. In view of the rate at which silicon costs are dropping, this spread in costs will increase unless packaging technology is given more emphasis.

Table 1-1 U.S. Packaging Market, 1987 Estimate

Type	Units (billion)	Average Cost ($/unit)	Total Cost (billion $)
DIP	7.4	0.13	0.93
CC	0.7	0.68	0.47
PGA	0.05	6.61	0.31
Other	0.7	0.34	0.25
Total (avg.)	8.9	0.22	1.96

The lead frames of DIPs are inserted in holes (vias) that extend through the printed circuit board. These holes are usually drilled on a 100-mil (0.1 in.) grid and each (copper plated) hole passes through each layer of a multilayer circuit. Chip dimensions are conventionally discussed in terms of micrometers (μm). Printed wiring interconnection structures are usually described in terms of mils (i.e., 0.001 in.). Advanced interconnection structures may involve both units; 1 mil is equal to 25.4 μm. The holes account for an appreciable fraction of the board area and thus limit the number of interconnections that the board can support. Chip carriers (CCs) are bonded only to the top surface (surface mount assembly, SMA) of a multilayer circuit, and no grid of holes are needed. With SMA, components can also be mounted on both sides of the board. Therefore, CCs with SMA are

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capable of a higher density of interconnection, which is an important driving force for CCs to displace DIPs. Pin grid arrays (PGAs) are also available in surface-mount form.

Chips are attached to the lead frame by "die-bonding" on the back side with solder or conducting adhesive, and the bonding pads are connected to the lead frame fingers by means of fine gold or aluminum wires. A "ball" bond is formed at the chip bonding pad and a "wedge" bond is formed at the inner lead frame finger. The process of wire bond formation is automated and very fast, although they are done serially, one at a time. The bonding pads on the chip are usually restricted to the perimeter. The spacing between bonding pads is, however, limited (about 6 mils) by the size of the wire-handling tool, which is an important design factor affecting chip die size for circuits with a large I/O count. An alternative to wire bonding is tape automated bonding (TAB), in which the lead frame is a thin copper layer supported by polyimide film and all the inner fingers are bonded to the chip pads in a single operation. By supporting the leads on film and eliminating the wire bonding tool, finer lead spacing (about 4 mils) and higher interconnection density are possible. This technology has been available for many years, but no large-scale displacement of wire bonding has occurred. Difficulties involved in preparing the pads or tape fingers ("bumping") and in the simultaneous bonding operation are significant.

Preformed packages (premolded plastic or ceramic) are sealed by affixing a lid. The chip resides in a cavity. If the package material is ceramic, the seal may be hermetic, a feature required for most military and other high-reliability circuits. All plastic materials are permeable to some degree, and thus hermeticity cannot be achieved today in plastic packages. Even so, plastic packages can be highly reliable. Plastic packages can be premolded, but they are more likely to be transfer-molded after the wire bonds have been formed. In this process, the chip, bonded to the lead frame, is placed in a mold tool and molten plastic is forced in to fill the cavity completely. Good adhesion between the plastic and the chip and the lead frame is achieved, which makes the structure durable. After the chip has been sealed in its package, it can be tested, transported, and mounted on a printed circuit board.

An alternative approach involves direct mounting of unpackaged chips on circuit boards. In the soldering process, the chips "float" (face down) on solder balls that form the conducting bridge to the circuit. This approach is sometimes called C4 bonding (for controlled* collapse* chip* connection*). The bonding pads are not restricted to the periphery of the chip, thereby offering considerable advantage. Other "bare chip" options exist, including the use of face-down, "beam-lead" or TAB lead frame arrangements, and also face-up wire-bonded configurations. Following assembly, these chips may be covered with a plastic coat ("glob top") for protection (see Figure 1-6). Chip-on-board (COB) interconnection is not amenable to the burn-in and testing required for military use, and hence this approach has been more popular in consumer-grade systems.

Printed circuit boards may have only one or two layers of circuitry, but high-density interconnection usually implies many layers, typically eight but

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possibly as many as 40. Patterns of metal are defined photolithography by means of a resist process on interlayer substrates, whereby "via" (i.e., through-sheet) connections are formed. The various layers are then "piled up" and processed to form the registered multilayer structure. For ceramic structures, the metals can be screen-printed in paste form, and the lamination is accomplished by "firing" at a high temperature (about 1600°C for alumina). Co-fired ceramics undergo large material shrinkage during processing, and thus present registration difficulties in multilayer structures. For epoxy-glass boards, copper patterns are etched (or plated) on partially-cured (B-staged) epoxy, and final bonding and curing are carried out under pressure at about 200°C. Vias are formed by electroless plating, after lamination for through-hole boards and before lamination for surface-mount boards. These processes are extremely demanding because the circuits are large in area and layer-to-layer registration must be maintained.

Figure 1-8 illustrates progress in chip and printed wiring board (PWB) miniaturization as measured by linear dimensions of conductor width or smallest circuit feature. Although there is much detail that is obscured by these lines, the progress is dramatic and real. Clearly, on-chip features have been reduced at a rate that consistently exceeds that for PWB patterns. Where chip features were an order of magnitude smaller in the 1960s than earlier designs, they are now nearly two orders of magnitude smaller than that. This, and other factors, will lead to an increasingly important intermediate level of interconnection. In fact, interconnect structures of intermediate size have existed right along in the form of thin-film hybrids. At this time, however, there is a great proliferation and diversity in the development of multichip modules (MCMs) that are at least a significant advance in hybrid technology and may be considered a new level of packaging. Multichip modules will probably become component-assembled on both hybrids and PWBs.

Multichip modules typically consist of a ceramic base section with power and ground planes. Interconnect circuitry is placed on top with fine metal traces, usually copper, separated by organic dielectric interlayers, usually polyimide. Because of the fineness of the signal traces, two layers on a MCM can replace many (>20) signal layers of a thick-film (screen-defined) structure.

In some MCMs, silicon wafers are employed as the substrate in place of ceramic. This form of MCM should not be confused with wafer-scale integration (WSI) technology, in which both chips and interconnections are fabricated on a single silicon wafer to form an independent system or subsystem. Yields are never 100 percent, and design redundancy is an inherent feature of WSI. This is a very demanding technology, and success has not been achieved, despite vigorous and well-conceived efforts. In the MCM approach, interconnect structures are built up on the silicon wafer, and tested chips are attached. The use of pretested chips greatly reduces yield loss. It seems evident that MCMs will play a central. role in high-density electronic packaging over the next decade.

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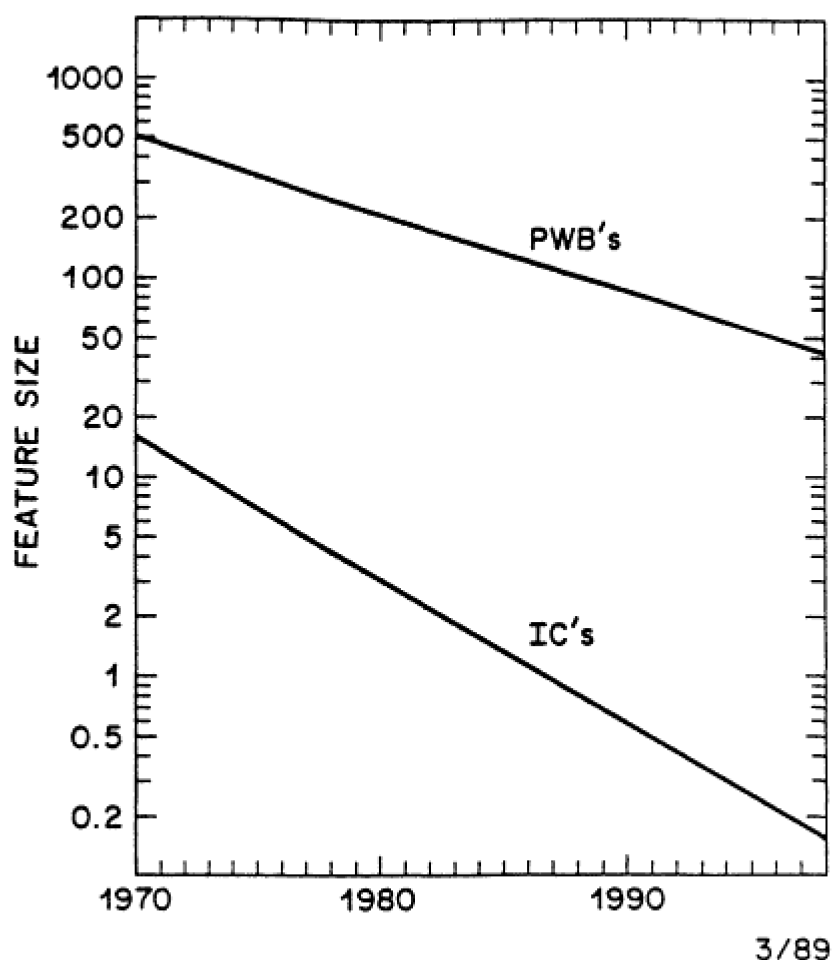

Figure 1-8
Progress in IC chip (in development) and PWB miniaturization (line widths expressed in µm). In Chapter 2 a more conservative extension of the IC line is developed.

Solder is employed for attaching chip packages to circuit board substrates. For DIP through-hole mounting, a solder wave is passed across the back side of the board (i.e., on the side with no components), which subjects the board to a brief thermal shock, although it is benign from the point of view of the components. For a surface-mount assembly, the entire structure must be brought to solder reflow temperature, which can place an unusual stress on the components. As the assembly is cooled following the soldering operation, thermal stress can arise if the thermal coefficients of expansion (TCEs) of the chip package and board substrate are not closely matched. This problem is accentuated as package size increases. When the TCEs are not well matched, the chip package must be provided with compliant leads that can adjust to the dimensional mismatches that develop with temperature changes. Conductive polymers, both isotropic and anisotropic, are being developed to replace solder, but widespread use in the next decade is unlikely.

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The materials of electronic systems can be summarized in terms of relatively few basic elements and compounds. The chips are silicon with aluminum metallization, and with silicon dioxide (silica), silicon nitride, or polyimide as the dielectric. A glass (P-glass) or silicon nitride is used for passivation. The chips are packaged in epoxy molding compounds filled with silica powder. Electrical connections are made with gold wires that go from chip bonding pads to lead frames constructed of copper or an alloy of iron and nickel. The packaged chips are attached by solder to printed circuit boards composed of epoxy-glass (or sometimes polyimide) substrates that support the copper interconnection patterns. In some cases, alumina substrates are employed with interconnections of refractory metals. Connections to other boards are made through connectors composed of molded plastic (e.g., diallyl phthalate, polyphenylene sulfide, etc.) with beryllium-copper contact fingers and cables with copper conductors insulated with extruded plastic.

This summary, while substantially accurate for the great majority of circuits, fails to reveal the enormous amount of materials engineering work that makes possible the manufacture and use of electronic systems. Each material has to be carefully tailored for specific purposes, and issues of material compatibility are of critical importance. The process sequence, often involving hundreds of steps, must be such that conditions later in the manufacturing sequence do not undermine structures formed earlier. This abbreviated description includes only the materials that remain in the final product. In fact, many other materials are necessary to the processes that give rise to the structures but are not an integral part of the final structure. Process control is increasingly critical. Thus, packaging materials present challenging demands. The package must provide timing information to all parts of all chips with manageable skew. Data must be delivered to and from chips with delays that are consistent with chip circuit switching times, and an increasing number of access points are required as chips evolve. Electrical power and ground must be supplied over leads having small impedance, which translates to extremely short paths. The heat generated by the chip circuitry must be transmitted to the environment effectively, lest the chip temperature rise disastrously.

In material terms, the electrical signal paths require high-conductivity metals (e.g., copper, aluminum, gold) and low-dielectric-constant insulation materials (e.g., polyimides, epoxies, hydrocarbons, and fluorinated polymers). The speed of light is a practical limiting factor in advanced circuits. For power delivery, high-conductivity metals are again necessary, but high capacitance that is physically close (i.e., low impedance) to the chip requires high-dielectric-constant capacitor materials, usually ceramic. Thermal conductivity favors metal, whereas other ceramic paths and polymers are thermal insulators. Thermal coefficient of expansion (TCE) is a critical factor in package design. Silicon has a low TCE compared with common metals and organic polymers. Thus, mechanical stresses are created when temperature changes occur as in manufacture, temperature-cycle testing, and use. The problem becomes more difficult as chip size increases. Thinner sections of the molded body are more susceptible to thermal-mechanically induced cracking failure. TCE of polymeric materials can be controlled by the addition of low-TCE fillers, as is conventional for molding compounds and printed wiring board

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resins. Many packaging and interconnection materials are composites designed to improve the TCE match.

As electronic equipment density increases, power dissipation becomes an ever greater problem. In general, heat is conducted away from the chips by the thermal conductivity of the materials employed. Metals and ceramics are relatively good thermal conductors, but polymeric materials as a class are poor conductors, a factor that will assume greater importance over the next few years. The tradeoff of dielectric constant and thermal conductivity will have to be met by compromises between materials and physical design. Application of fluid heat-exchange media will also increase, but the cost of this option is high, therefore, integration of this approach into physical design is essential. Thermoelectric cooling offers an alternative to thermal conductivty, a technology that has been applied to some commercial circuits.

This report begins with a discussion of system trends and needs (Chapter 2), followed by a description of approaches that have been employed for packaging and an indication of current trends (Chapter 3). Chapter 4 discusses materials issues, and Chapter 5 gives more specific information and perspective on plastic and ceramic encapsulants, ceramic substrates, and organic printed circuit structures. Chapter 6 presents an analysis of material sources, current trends, and the importance of the field in the context of international competitiveness. These discussions lay the groundwork for the recommendations for future actions in terms of specific technical development and research, and the organizational and political factors that distinguish the United States from other countries.

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Chapter 2

Microelectronic System Trends and Packaging Needs

Electronic systems needed in the next few years will require unprecedented packaging technology. In this chapter, the demands placed on the packages by anticipated chip technologies are discussed. In particular, the approach is to list requirements that, if met, will ensure that the inherent performance capabilities of the chips can be achieved and will not be degraded by the package. Some of these requirements deal with the interfacing of individual chips, whereas others deal with the interconnecting of groups of chips. In today's technology, these two functions are most often fulfilled by first-level packages, such as dual in-line packages, and by second-level packaging, such as printed-circuit boards, respectively.

Packaging requirements for the mid-1990s are of interest here. It is important to avoid any implicit assumption that the packages, appropriate at that time, can be categorized in the same way they are now. Indeed, there is already strong evidence that combining traditional packaging levels can lead to improved performance. For example, the IBM "thermal conduction" module eliminates one level of packaging by combining two levels into a single structure. In this chapter, those requirements that deal with interfacing individual chips are covered, as are those that deal with interconnecting several chips; the terms first-level and second-level packaging are not used. For interfacing to a single chip, the following additional requirements are important:

- die attachment
- chip pinout
- pinout configuration
- heat removal
- signal rise time
- power lead inductance
- power supply current
- interline coupling
- protection from the environment

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For connecting two or more chips, the following additional requirements are important:

- wiring configuration
- propagation delay
- signal rise time

Each of these requirements must be satisfied at acceptable cost and reliability, without adversely affecting the other requirements. It is assumed in this chapter that the signal-interconnection techniques do not employ multiplexing or optics, so there is exactly one electrical connection per signal (plus, perhaps, multiple ground and power pins).

It is possible to estimate many of these requirements rather accurately by extrapolating past characteristics of chips and systems, using ***scaling theory*** as a guide. The various types of chip scaling and the related theories are discussed in the next section. Scaling theory alone is not sufficient because different chips will be built using different architectural styles. An empirical relationship between pinout and circuit complexity, known as ***Rent's rule,*** can be used to characterize architectural style with sufficient accuracy for this discussion. Rent's rule and related items are also discussed in a later section.

Three principal system types have been identified, each of which appears to make different demands on packaging: low-end digital, high-end digital, and high-speed. Low-end digital systems typically use silicon MOS circuits packaged separately, with printed wiring boards (PWB) for chip interconnection. High-end digital systems typically use silicon bipolar technology, often with packages in modules that carry many chips. The advent of bipolar complementary (BiCMOS) technology will blur the distinction between the two digital system types in the future, but for the purposes of this study it is assumed that **BiCMOS** will have interconnection requirements similar to **CMOS and power requirements intermediate between CMOS and bipolar**. High-speed circuits typically use gallium arsenide (GaAs) chips. The assumptions about the chip technologies are presented in later sections in this chapter. The requirements listed above are qualified, where possible, for each of the system types.

SCALING THEORY

Scaling theory is important in understanding the driving forces that affect the trends of integrated circuit chips. The semiconductor industry learned, more than 20 years ago, that shrinking the photolithographic dimensions on the wafer and increasing the chip and wafer size increased the productivity of the semiconductor plant. The benefit to the user was lower cost per circuit, more functions per chip, and higher performance. The end result has been a quadrupling of the level of integration every 3 years. This section draws on scaling theory to permit a projection of the performance

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trends of bipolar and MOS integrated circuit chips and of generic module and board configurations. The intent is to understand the evolutionary trends and try to determine the material properties that may limit or even dead-end those trends.

Lithography

Lithography is of fundamental importance in semiconductor fabrication, and, therefore, a look at lithography is needed to get a feel for the future direction of the semiconductor industry. A key parameter is the minimum feature size that a given lithographic technology is capable of patterning on a chip at a given point in time. Minimum feature size has a first-order bearing on both circuit performance on a chip as well as the circuit density. To predict future packaging needs in the mid-1990s, it is important to have some feeling for what minimum feature size can be patterned in production in that time frame.

Bakoglu (1986) points out that between 1959 and 1983 the minimum feature size shrank at an average rate of 11 percent per year. Assuming that in 1988 the minimum feature size being patterned in production is about 1.0 μm, then by mid-1995, or seven years later, the minimum feature size will be about 0.5 μm. This assumes that the feature size will shrink about 10 percent per year. This is optimistic, since this dimension is near what is generally agreed to be the limit for optical lithography. It is an accepted fact that the rate of progress decreases as the limit of the technology is approached.

Optical lithography has been used since integrated circuits were first invented. The minimum feature size that optical lithography is capable of producing is limited by the wavelength of light used, and it therefore has a very fundamental limitation. Electron beam lithography can provide very small feature sizes with the use of proper photoresist material. However, it is highly doubtful that electron beam systems will ever be used in a production environment because of their slow throughput caused by their limited bandwidth. It is projected (Kern et al., 1988) that optical lithography sources are expected to be available for resolutions down to about 0.35 μm and will be extensively used into the 1990s.

The one technology that has the capability of providing a minimum feature size, smaller than 0.35 μm in volume production, is x-ray lithography. Whether an x-ray lithographic production system can be developed and installed by 1995 is dependent on many factors. Two major nontechnical factors are the need and the return on investment. Memory chips provide both a need, because of increased density requirements, and a better return on investment than logic chips, because of higher volume per part number, fewer part numbers, and increased yield. The increase in yield is a result of the fact that very small dirt particles are transparent to x-rays. If the very difficult technical problems associated with introducing x-ray lithography into a manufacturing operation can be overcome, then it is quite probable that it will be first used to fabricate memory chips, for these reasons.

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In view of the foregoing discussion, it will be assumed that during the mid-1990s the minimum feature size, practiced in production volumes, will be about 0.5 µm.

Scaling of Mosfets

As photolithographic techniques have improved, it has been possible to reduce the minimum feature sizes on chips. However, power supply voltages tend to remain standardized for economic reasons. As a result, it is not too meaningful to perform a scaling analysis while holding the electric field constant in the device being scaled. Baccarani and coworkers (1984) and Dennard (1986) have developed the general scaling relationship shown in Table 2-1. In this analysis, α is the factor by which the dimensions are reduced and ϵ/α is the factor by which the applied voltage and threshold voltage are multiplied. The depletion regions are scaled down, along with the other dimensions, by multiplying the doping concentration within the scaled device by the factor $\epsilon\alpha$.

Table 2-1 Generalized Scaling Relationships

Physical Parameters	Scaling Factors
Linear dimensions	$1/\alpha$
Electric field intensity	$\epsilon \cdot 1$
Voltage (potential)	$\epsilon \cdot 1/\alpha$
Impurity concentration	$\epsilon \cdot \alpha$
Wiring current density	$\epsilon^2 \cdot \alpha$
Gate delay	$1/\epsilon \cdot 1/\alpha$
Power/gate	$\epsilon^3 \cdot 1/\alpha^2$

Source: Based on Baccarani et al., 1984; Dennard, 1986

When the power supply voltage is held fixed, then $\alpha = k\epsilon$, where k is a proportionality constant, and the gate delay scaling factor becomes k/α^2. There are limits to how far generalized scaling can be extended, since, as ϵ increases, gate-to-insulator failure increases and hot-carrier mechanisms produce long-term degradation. In addition, the current density in devices and metallization increases, which can lead to electromigration-type failures. Another problem that is aggravated as device dimensions shrink is the effect of alpha particles.

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Therefore, within limits, as the device dimensions on a chip shrink, the delay per gate decreases, as does the power per gate. Devices have been made and tested (Dennard, 1986) that confirm the scaling analysis. The experimental results show that a loaded NMOS NOR circuit constructed with a 1.0 micrometer channel length and again with a 0.5 micrometer channel length exhibited gate delays of approximately 1.0 and 0.5 nsec respectively. The power per circuit decreased by about a factor of 4, to about 50 µw dissipation. In this experiment, the power supply voltage was scaled by about a factor of 2, from 2.5 to 1.2 volts, so as to keep the electric field in the device constant.

These scaled NMOS NOR circuits were patterned with a vector-scan electron beam exposure system having a capability of producing 0.5 µm features with a standard deviation of ±0.05 µm in both feature size and level-to-level overlay. Circuits with channel lengths as short as 70 nm have been fabricated with five levels of electron-beam lithography overlaid, with an accuracy of better than 30 nm (Kern et al., 1988; Sai-Halasz et al., 1987). In a ring oscillator, these silicon field effect transistors (FETs) have a delay per stage of 13 psec.

In addition to the technical problems associated with shrinking the dimensions of NMOS devices, this technology has a serious competitor in the form of CMOS. It is highly probable that CMOS will be the dominant technology by the mid-1990s, with bipolars and GaAs relegated to specific applications where their unique properties are superior to those of CMOS.

Scaling of CMOS

The CMOS technology has a very important and positive characteristic because its circuits dissipate power essentially only during switching. When these circuits are in a quiescent state, they consume very little power. This is an important feature, since power that is not consumed does not need to be removed. In addition, the copper required in the conductors supplying power to the back planes and modules is greatly reduced. The designer of a CMOS system must not, however, expect to operate very densely packaged chips at very high clock rates without due concern for heat dissipation. The nature of a CMOS gate is that its power dissipation increases in direct proportion to its clock rate, all other terms held constant. Noise generated by these gates increases at high clock rates to such an extent that they may not be sufficiently noise-tolerant in digital systems beyond clock rates of 75 to 100 MHz. It is doubtful that high-clock-rate problems can be corrected by either scaling or by operation at liquid nitrogen temperatures. (Appendix C gives projections on operating and structural parameters.)

CMOS had to overcome two major handicaps before it became a very acceptable technology: latch-up and a complex manufacturing process. Latch-up, caused by the current gain of parasitic lateral transistors, produces a high current path between the power supply and ground lines, a feature that destroyed early CMOS chips. This is no longer a problem. The CMOS manufacturing process approaches the complexity of the bipolar process. By slightly increasing the complexity of the CMOS process, bipolar transistors

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can be fabricated on the same chip as CMOS devices. Bipolar transistors have a much higher transconductance, or di/dv (change of output current to input voltage change), and as a result take up less area on a chip for a given drive capability.

Baccarani and associates (1984) applied general scaling theory to a 0.25 µm NMOS FET and calculated that a device with a fan-out of 3 would have a gate delay of about 200 psec, with a power dissipation of 50 µw at a power supply voltage of 1.0 volt. In relating their results to CMOS, they state, "Due to the lower hole mobility, and to the larger sheet resistance of p+ shallow junctions, however, quantitatively different results are obtained in this case, leading to somewhat modified design tradeoffs." They are saying that the design of the n-channel FET in the CMOS circuit must be optimized differently than the p-channel FET. The lower hole mobility will adversely affect performance of the CMOS circuit.

Boudon and associates (1988) describe a 20K two-way NAND equivalent CMOS gate array prototype with 0.5 µm channel length FETs. The 7.5-× 7.5-mm chip is designed for high performance, with 245 psec gate delay with a fan-out of 3. A 32-bit reduced-instruction set computer (RISC) processor, with a 16-× 16-bit multiplier implemented on the chip, has been measured at 17 nsec cycle time with a 3.4-volt power supply. This experimental result is 1.6 times faster than the same implementation with a CMOS 0.9 µm gate.

Cong and associates (1988) describe a low-power CMOS dual-modulus (divide by 128/129) prescalar integrated circuit. They point out that the prescalar has been traditionally implemented in GaAs or bipolar technologies. The best prescalar fabricated with 17.5 nm gate oxide, functions at 2.06 GHz with 25 mw power consumption. The channel length is 0.5 µm and operates on a supply voltage of 3.5 volts with ring oscillator (unloaded) delay of 110 psec.

When CMOS devices are designed for low-temperature operation, at liquid nitrogen temperatures of 77 K, the circuit speed is enhanced by a factor of two. The reasons include decreased leakage, increased carrier mobility, sharper subthreshold turn-off transition, lower interconnect line resistance, and improved reliability (Sai-Halasz et al., 1987). In addition, latch-up effects are greatly reduced at low temperatures because of lower bipolar gains. As device dimensions decrease, the benefits of operating at 77 K become more attractive.

Scaling of Bipolars

The bipolar transistor has had a long history of development. During the period when it was produced as a discrete device, two techniques were invented to improve its performance by keeping it out of saturation. They were the Schottky clamp-circuit, invented in 1953, and the emitter-coupled logic (ECL) circuit family, invented in 1956. Since the invention of the integrated circuit, many improvements have been made to the bipolar device structure. In parallel with these improvements have been improvements in photolithography that have reduced the size of the device, with an attendant increase in performance.

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A few of the important structural improvements made to bipolar planar devices are self-aligned base contact, deep-trench isolation, and a polysilicon emitter contact. Both the self-aligned structure and the trench isolation greatly reduce the device area and the associated parasitic capacitance, and hence significantly reduce the power-delay product and increase the density of bipolar circuits (Ning and Tang, 1986). Experimental evidence has overwhelmingly shown that polysilicon emitter contacts make it possible to vertically scale bipolar transistors and improve circuit performance without unacceptable degradation in current gain.

Ning and Tang (1986) state, "The trend in bipolar device technology is then to develop the version or versions of self-aligned structure, deep-trench isolation, and polysilicon emitter contact that are manufacturable and applicable to both high-speed as well as high-density applications The central idea is to reduce the horizontal and vertical dimensions in a coordinated manner so that all the key delay components are reduced approximately proportional in scaling."

The scaling rules for ECL circuits are shown in Table 2-2. The projected delay as a function of the switch current of the scaled circuit is shown in Figure 2-1. Reduction in gate delay can be expected as chip power is increased in projected future circuits.

Table 2-2 ECL Scaling Rules

Parameter	Rule*
Base width, W_b	$a^{0.8}$
Base doping level, N_b	W_b^{-2}
Collector current density, J_c	a^{-2}
Collector doping level, N_c	J_c
Circuit delay	a

* a = minimum feature dimension and emitter-stripe width
Source: After Ning and Tang, 1986

It can be seen from Figure 2-1 that the maximum benefit in performance, from scaling, is obtained when the current, and hence the power, is held fixed. Naturally, it is possible to reduce the current as the emitter width is reduced and accept a smaller improvement in performance. This approach has generally been resisted by the ECL enthusiasts, since they constantly strive for improved performance. As a result, ECL-based systems consume quite a bit

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of power (2 to 5 mw per circuit), which must be supplied and removed. A further complication is that the power supply voltage is in the range of 2 volts, which means that a system with a power requirement of 5000 w will require a current of 2500 A. This magnitude of current requires a copper conductor of very large cross section between the power supply and the circuit modules or board.

GALLUM ARSENIED TECHNOLOGY

An additional category of digital components, which has emerged from the laboratory and entered general use during the 1980s, is that of the extremely high-speed devices. Such devices, because of the lower level of integration at this time, typically exhibit a smaller number of signal pins than, for example, CMOS chips, but in a few years, they can be expected to have the same pinout needs as today's slower-speed silicon counterparts. Logic gate delays in these ultrafast chips of as little as 10 to 100 psec make it possible to design signal processors that are already achieving clock rates as great as 2 GHz. Furthermore, gallium arsenide (GaAs) digital integrated circuits have been demonstrated in the laboratory that perform useful functions at even higher clock rates, of up to 25 GHz. Present GaAs chips of 1000 gate complexity, capable of 6 GHz, are available in experimental quantities (in 1989), 10-GHz digital chips will be available by 1990 to 1991, and 20- to 25-GHz chips are expected to be readily available by 1995.

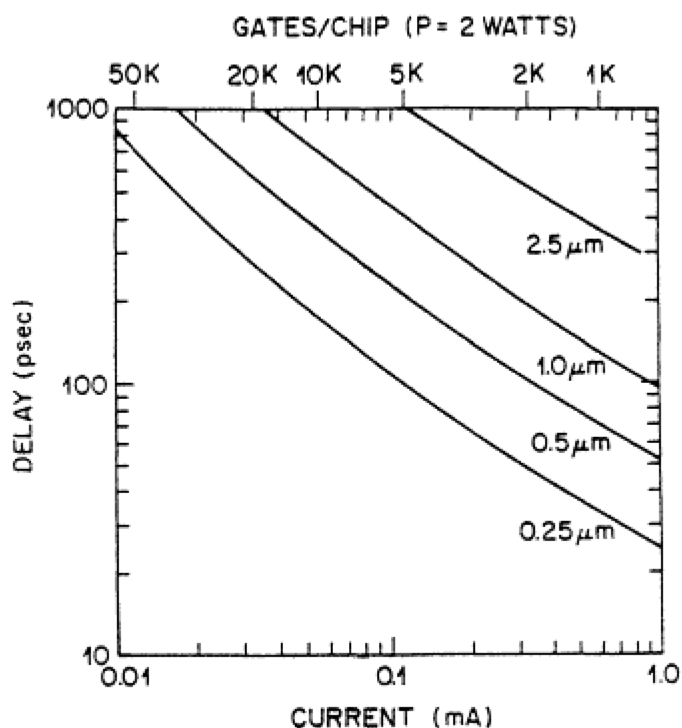

Figure 2-1
Gate delay for a 2 watt chip as a function of switch current. The curves refer to emitter stripe width. (After Ning and Tang, 1986)

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Very-high-frequency digital integrated circuits are employed in a wide range of equipment, including supercomputers, telecommunications transmission equipment, communications satellites, radar, video image processing, military electronic countermeasures, image processing, and air traffic control displays. Silicon ECL components have been used traditionally, and GaAs components are now being introduced. Clock rates have been increasing steadily and are now at about 0.5 GHz. The fast digital portions of these circuits may be small enough to fit onto a multichip module, which will be the heart of the system.

Very-high-speed electronics require attention to electromagnetic issues that are often unfamiliar to digital systems designers. Fast rise-time devices radiate electrical energy in that portion of the electromagnetic spectrum traditionally reserved for analog microwave communication channels and radar systems. Bandwidths must be preserved as the signals propagate through the packaging and interconnect structures, if the robustness and noise immunity of the processors are to be maintained. Despite these problems for interconnect designers, these enabling technologies will be pursued vigorously during the next decade, because the higher system clock rates can lead to signal processing rates that are one or two orders of magnitude greater than those currently available.

RENT'S RULE

About 1960, Edward Rent, working at IBM, observed a relationship between the complexity of logic circuit (expressed, for example, by the number of gates in it) and the number of signal wires (pins) connecting to it. [Rent himself never published an account that bears his name, but two early references describe the relationship (Logue, 1966; Landman and Russo, 1971)]. In its simplest form, it is

$$N_p = K_p N_g^{\nu}$$

where N_p is the number of pins, N_g is the number of gates, and K_p and ν are constants. The relationship has been applied to a variety of systems, including digital computer systems, integrated circuits, random logic, and even animal eyes and brains. Rent's rule is used here to predict the pinout of future integrated circuits and the interchip wiring complexity of highly parallel computer architectures of the future.

Two empirical constants, K_p and ν, appear in Rent's rule. Of these, ν is the more critical. In a two-dimensional world, such as inside an integrated circuit or on a printed-circuit board, the rule is qualitatively different, depending on whether w is above or below 0.5. If ν is greater than 0.5, then, as more and more complexity is added to a circuit, the circuit becomes harder and harder to wire. To appreciate this, consider a chip on which the perimeter is used for bonding pads, and suppose that all the space on the (one-dimensional) perimeter is used for these pads. If the size of the circuit quadruples (e.g., by making each dimension of the chip twice as

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large), the required number of pins more than doubles, yet the perimeter only doubles, and as a result not all the required pins will fit in the available space. A similar argument applies to wiring within the chip if the subcircuits on the chip themselves obey Rent's rule with the same exponent. Values of v below 0.5 do not pose such difficulties. Incidentally, in a three-dimensional setting, the critical exponent is 2/3 rather than 1/2, because this is the exponent governing the ratio of surface to volume.

Recent examinations of Rent's rule (Bakoglu, 1986; Ferry, 1985) have focused on the critical nature of the exponent, and it has been observed that different styles of system architecture or different types of systems seem to be characterized by different exponents. The values reported by Bakoglu (1986) are 0.63 for chip-and module-level design of high-speed computers (in agreement with Rent's original value), 0.5 for gate arrays, 0.45 for microprocessors, 0.25 for board-and system-level computers, and 0.12 for memories. The value reported by Ferry (1985) is 0.21 for a mix of logic, microprocessors, and memory. Bakoglu's value for microprocessors appears to be heavily biased by a single early example and two RISC chips; without them, the value is less than 0.2.

Rent's rule is empirical, and empirical observations invite fundamental explanations. It may be that an exponent of 2/3 can be explained by the surface-to-volume ratio of a design produced by evolution that is truly three-dimensional, such as animal brains. It is also obvious that memories should have a low exponent, since address coding permits the number of address pins to be a logarithmic function of the size of the memory. For the other types of systems, however, fundamental explanations seem less satisfactory.

However, one fundamental distinction does seem appropriate. Ferry (1985) attributes to McGroddy and Solomon (1982) the distinction between *highly partitioned* and *functionally partitioned* circuits. The former are defined as those for which chip or module boundaries do not tend to coincide with system or subsystem boundaries. Gate arrays, random TTL logic, and indeed designs where many components are required for a system, are like this. Functionally partitioned circuits, on the other hand, are defined as those in which the chip or module boundaries do coincide with system or subsystem boundaries. Microprocessors are like this. The definition of what is a subsystem is a human one, based on the partitioning of a total system for easier human understanding. Human understanding is more likely to occur when the subsystems do not have complex interactions but instead interface with minimal information interchange. It appears that the following values of constants appear to characterize different types of chips and systems:

- Memory chips, $K_p = 6$, $v = 0.12$
- Functionally partitioned chips, $K_p = 10$, $v = 0.2$
- Modules and boards, $K_p = 82$, $v = 0.25$
- Highly partitioned chips, $K_p = 2$, $v = 0.5$

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These values are generally consistent with the data presented by Ferry (1985), although they differ from the numbers given by Bakoglu (1986). It is likely that the data for gate arrays (highly partitioned) are based on the fact that, in most present packaging schemes, signal pins are located on the periphery of chips. As a result, a natural evolution from one gate array to the next, keeping design style and design tools similar, will necessarily scale the pinout as the square root of the number of gates. Thus, the pinout of highly partitioned chips may in fact be limited more by the interconnect technology available than by the inherent needs of the logic, and therefore, in designing packages for the future, perhaps higher exponents might be appropriate.

Other types of chips can be categorized according to whether they are highly partitioned or functionally partitioned. For example, systolic arrays and some signal-processing chips may be functionally partitioned, whereas the "glue logic" that seems to surround microprocessors in many systems is probably highly partitioned.

CHIP TECHNOLOGIES

The committee's assumptions about chip technology in use in systems in the mid-1990s are summarized in Table 2-3. These data were supplied by Donald R. Franck of the Empire Planning Group (personal communication to the committee, October 1988), except as follows: The linewidth estimates are justified earlier, and the inter-latch delays are an assumed logic depth (20 for MOS, 15 for bipolar, and 10 for GaAs) times the gate delay, plus an estimate of on-chip wiring delay. This estimate is the "Elmore time constant" of an aluminum wire 4 mm long with the linewidth, cited as 0.3 µm thick, over and under 0.5 µm thick oxide insulators; for GaAs, silicon nitride insulator above and insulating GaAs below (Elmore, 1947; Rubenstein et al., 1983). This wire has a resistance of 700 ohms and a capacitance of 0.4 pF, for an "Elmore time" of 140 psec (1 pF and 350 psec for GaAs). Even the relatively long length of 4 mm assumed here will require restraint on the part of circuit designers, since chip sizes are expected to be up to 3 cm on a side in 1994, and thus circuit designers will have to use careful placement of combinational logic blocks and perhaps buffers for long signal paths. The clock frequency calculated assumes that during half a clock cycle a signal must settle and the settling time should be at least 1.5 times the inter-latch delay. In other words, the clock period is three times the inter-latch delay. The power supply current is the power divided by the assumed supply voltage, and the power per gate is calculated from the chip power and gate count.

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Table 2-3 Mid-1990s Integrated Circuit Chip Technologies

Chip Interface	CMOS	Bipolar	GaAs
Linewidth (µm)	0.5	0.5	0.5
Gate count	400,000	20,000	100,000
Power and signal pinout	600	600	300
Pinout configuration	Two dimensions	Two dimensions	One dimension
Device gate delay (psec)	200	40	50
Inter-latch delay (nsec)	4.1	0.74	0.85
Clock frequency (MHz)	80	450	250
Power supply voltage (v)	3	1.3	2
Power (W)	20	40	20
Current (A)	6.7	33	10
Power per gate (µW)	50	2000	200

Source: Based on data from D. R. Franck (personal communication to the committee, October 1988) and some prepared by the committee.

The "pinout configuration" entry in Table 2-3 requires an explanation. Consider the problem of providing pins for integrated circuits, which are planar (two-dimensional). The "boundary" of a two-dimensional region is one-dimensional, in this case the perimeter of the chip. Modest pinout (say up to 300) can be satisfied by one row (or two) of pads at the perimeter of the chip, and, in fact, most chips fabricated today use perimeter bonding pads. Therefore, without revolutionary reductions in pad size, the larger pinout that will be needed in 1994 cannot be satisfied with perimeter pads, so the two-dimensional chip area must be used. Indeed, this technology is in some use even today. Thus, the demand for more pinout must be satisfied by "escaping" to a higher dimension.

If the full performance of the chips, as summarized in Table 2-3, is to be realized in a system, the packaging requirements listed in Table 2-4 are necessary. Any deviations from meeting these specifications will force compromises on chip and system designers and will, therefore, mean that system performance is limited more by the packaging than by the chips.

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Chip Interface Packaging

For interfaces to the chip not to inhibit the chip performance described earlier, the following packaging requirements apply (see Table 2-4). The package pinout must, of course, equal the chip pinout. The package pinout configuration cannot be accommodated using the perimeter of the package for the same reasons that this will not be possible for chips. The chip power cited is from D. R. Franck (personal communication to the committee, October 1988). The chip drivers and receivers, together with the package signal lead inductance, must be capable of responding in the inter-latch delay cited above—in other words, in about a third of the clock cycle. The power (and ground) lead inductance is calculated by requiring that the L di/dt voltage dropped across the pins not exceed 0.1 times the supply voltage, when as much as 50 percent of the current for MOS, 5 percent of the current for bipolar or 10 percent of the current for GaAs is switched in a time equal to the signal rise time. Clearly, this requirement cannot be met unless multiple pins are used for both ground and supply voltage. This requirement can, however, be relaxed if a multiphase clock or on-chip voltage regulation is used.

Table 2-4 Mid-1990s Chip Interface Technology

Chip Interface	Low-End Digital	High-end Digital	High-Speed
Chip pinout	600	600	300
Package pinout configuration	Two dimensions	Two dimensions	One dimension
Heat removal per chip (W)	20	40	20
Signal rise time (nsec)	4.1	0.74	0.85
Power lead inductance (nh)	0.4	0.07	0.17
DC power supply current (A)	6.7	33	10
Environmental protection	Essential	Essential	Essential

Chip Interconnection Packaging

If the signal propagation delay from chip to chip and the signal rise time for interchip communication at least match the inter-latch delay for the chips, then signals can be transmitted from one chip to another during a single clock cycle, and the packaging will not substantially degrade system performance. The requirements are given in Table 2-5.

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Table 2-5 Mid-1990s Chip Interconnection Technology

Chip Interconnection	Low-End Digital	High-End Digital	High-Speed
Wiring configuration	Two dimensions	Three dimensions	Two dimensions
Propagation delay (nsec)	4.1	0.74	0.85
Signal rise time (nsec)	4.1	0.74	0.85

The key requirement for interchip packaging is the ability to have a large number of interconnect wires between and among chips. This is necessary whenever an overall system is too complex to be put on a single chip. Generally, total systems have a relatively small number of signal pins, because systems with complex interfaces are difficult to understand and systems are, after all, defined by humans who must understand their input and output behavior. The need for complex interconnections arises when the limitations of chip technology force a system to be implemented on more than one chip.

Systems are conceived in all sizes, and, therefore, it is difficult to be quantitative in the general sense about the interconnect needs. For this reason, no estimates are given regarding pinout of modules that perform chip interconnection. Rent's rule for highly partitioned chips and modules is probably valid for systems, both high-end and low-end, that are sufficiently complex so that many chips are necessary.

The entry "wiring configuration" in Table 2-5 requires further discussion. Today, the most common interchip wiring is done on printed wiring boards (PWBs) in which a very small number of two-dimensional routing surfaces are used. This works well only for limited chip pinout and limited board pinout. It works best for chips with perimeter bonding, or whose first-level packaging provides perimeter connections, because of the difficulty of using essentially a two-dimensional scheme to connect to a two-dimensional pinout array, given the normal wire size, spacing needed to reduce crosstalk and adjacent-conductor shorts, and the pad or connector size.

Chip pinout for 1994 will require, for systems with several chips, a correspondingly high number of connections between chips. For example, consider a system that requires several 1994 chips, each with pinout of 600. The partition of functionality among the two chips might be "highly partitioned" in the sense used earlier, with a Rent's rule exponent of 0.5. In that case, two chips taken as a unit would, between them, need 850 wires to connect with the rest of the system. The remaining 350 pins from the two chips might go between these chips, implying the need for 175 signal paths between these adjacent chips. (This number might be increased slightly because some electrical nodes have multiple connections.)

The required interconnect density, although difficult to quantify in general because of the varied size of systems and the degree of partitioning

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necessary, is clearly beyond the capabilities of today's PWB technology and also will be difficult to satisfy with advanced multichip modules. It is believed that, for high-end systems with many chips, the wiring congestion can be overcome only by using a three-dimensional interconnect structure. By this is meant a structure in which the wiring density in the third dimension is comparable to that in the other two dimensions. This kind of structure actually is not as far-fetched as it sounds; the IBM thermal conduction module and today's best PWBs have horizontal and vertical pitches for horizontal wires, and horizontal pitches for vertical wires, that are within a factor of five. In the case of the thermal conduction modules, the horizontal spacing between wires in one plane is 5 mils, the distance between planes is 10 mils, or 20 mils if a ground plane lies between for shielding, and the pitch of vias is 25 mils.

In contradistinction to the moderate clock rate described throughout this report, packaging intended for the fastest clock rate devices (both silicon and GaAs) must assume that the interchip signal connections will be transmission line in nature. It is difficult to understate the impact on chip interconnect caused by the need for a transmission line environment on the substrate, which, as a rule of thumb, arises whenever the off-chip signals exhibit risetimes of 2 nsec or less. The risetimes of typical silicon ECL and GaAs components are all less than 1 nsec at present. It should be noted that the fastest risetimes are currently in the 200-psec range, with 100 psec achieved on a small subset of the very fastest GaAs devices intended for communications applications. Although even 30-psec risetimes have been demonstrated, these ultrashort risetimes will not be necessary until the mid-1990s, when clock rates exceeding 10 GHz are employed in communications and radar processors.

Driven by the operating parameters of high-clock-rate systems described above, all of the parameters of concern for silicon CMOS chips assume even greater importance for the fastest devices. The use of single-chip surface-mounted packages is already giving way to the method of placing bare chips nearly side by side on very dense metal-on-organic dielectric structures (e.g., copper-on-polyimide or the equivalent). The ability to fabricate very uniform transmission line structures on these dense "chip-on-board" substrates, with low DC and AC resistive losses in the lines, will be important.

To minimize the high-frequency crosstalk between densely-packed interconnect lines, very low values of dielectric constant (ϵ' about 2.0) will be required for the materials that separate the signal planes from their ground reference or shield planes. Such low ϵ' values not only increase wavefront propagation velocities, but also allow ground planes to have minimum separation from the signal planes for a given line impedance, thereby decreasing interline coupling effects. The interplane dielectrics must also not be lossy and must not become lossy at higher frequencies because of adsorbed or chemically-bound water. For interconnection between the chips and the substrates, the frequency limits of wire bonding must be better assessed, and current TAB technology must be extended (e.g., with "flip-TAB" or modified "flip-chip" techniques) to provide improved high-frequency transmission line behavior and shorter total lengths of the TAB structures. Finally, the

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ability to provide integral high-frequency local power plane decoupling adjacent to the active chips must be provided in a more cost-effective manner than is done now.

The flip-chip technique provides an excellent ultra-high-frequency connection between chip and substrate. The technique permits the chip to be removed a limited number of times. However, the ability to provide signal integrity, with demountability between the MCM and the back panel, becomes increasingly more difficult as signal risetimes approach 100 psec. When innovative approaches (e.g., fuzz buttons and elastomeric materials) are considered for solving connector problems of high-performance electronic systems, materials issues must be considered. (See Appendix D for two innovative approaches.)

SOME PACKAGE DESIGN CONSIDERATIONS

The single-chip and multichip modules are described in this section to point out the techniques used to handle the interconnects and the problems encountered in each type.

Single-Chip Modules

Single-chip modules (SCMs) can be divided into two categories: the first is the surface-mount module, and the second is the pin-through-hole module. The surface-mount package, of necessity, requires that the leads come out around the perimeter of the package. This, therefore, requires that the lead pitch becomes finer because the number of leads supplying signals and power to the package increases as more circuits are placed on the chip. To support 400 to 700 signal and power connections to a surface-mount package in a surface-mount configuration in the 1994 time frame would require about a 12-mil lead pitch. The leads would have to be staggered, since the card or board to which they are soldered or otherwise connected must have more than one plane of connections for signal and power. It is doubtful that vias that make connections from the surface to internal planes can be placed on 12-mil centers. The problem is solved by staggering the length of the leads exiting from the surface-mount module. Handling 400 to 700 very fine leads that have a pitch of 12-mils is a difficult problem in production, as is the problem of removing 15 to 20 W of heat from the chip in this package.

The pin-through-hole single-chip module has the pins in an area array. The pins are inserted into holes in the card or board or the next level of package. It is conceivable that the single-chip module need not have pins, but it could have contacts that mate with contacts on the next level of package. In any case, it is necessary to have vias under the module that permit connection to the internal wiring planes in the next level of package. If pins do not need to be inserted in holes, then these holes can be smaller in diameter than holes that must contain pins. In any case, there is wiring congestion under the module. If, as is usually the case, there is a limit to the number of lines that can pass between two vias, then more wiring planes

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are needed in the next package level to overcome the wiring congestion under the module.

Multichip Modules

The advantage that a multichip module (MCM) provides is greater density at both the module level and at the system level, because with the greater density comes improved performance from the shorter transmission paths. This improved performance is attained in present MCMs even though the dielectric constant of the ceramic is approximately nine. Since the velocity of propagation is proportional to $\epsilon^{-0.5}$, the velocity of signals propagated on lines within the ceramic is one-third of the velocity of light. Future MCMs will require insulating materials whose dielectric constants are as close to 1 as possible. Naturally, the insulating materials used must be patternable; that is, it must be possible to make via holes in the material that can be filled with a conductor to provide a connection path from one level of conductor to the next. The insulator must permit a conductor to be attached to it by some means, such as evaporation, sputtering, or vapor deposition. The process of laying down the insulator and patterning should be a dry process, because dry processes cause fewer ecological problems and provide high resolution in a patterning process.

The chips, mounted on the MCM, must be attached in such a way as to provide electrical connection to the 600 signal and power supply connections that must be made to each chip. Since each chip may dissipate as much as 50 W of power, large thermal stresses can be set up in the connections made to the chip. When the system containing these MCMs is cycled on and off, these cycled stresses in the connections between the chip and the module can and do fail from fatigue. This requires that the thermal expansion coefficient of the substrate material of the MCM match that of the silicon chip. The problem is complicated by the fact that the substrate material dissipates much less I^2R power than does the chip, which results in a short-term transient thermal mismatch between the chips and the MCM substrate. The use of Peltier-junction cooling close to the chip is worthy of consideration here. In addition, it should be noted that the thermal mismatch problem is not peculiar to MCMs, but is equally important with SCMs.

The mismatch in thermal expansion coefficient between the MCM substrate material and the chip material is aggravated when the distance between the extreme farthest connections to the chip increases. Since there are 600 such connections, there will be an array of connections with about 25 connections on a side. If the chips are 1 cm on a side, then the array of connections must exist within the chip footprint, or within about 0.8 cm, which places connections on 0.32-mm (12.6-mil) centers. If the via holes in the insulating material, which contain the metal that connects to the wiring plane below are 5 mils in diameter, then the distance between the via walls is 7.6 mils with no tolerance. If there is an allowed tolerance or a guard band of 1 mil around each via, only 5.6 mils are left in which to place lines that conduct signals within the wiring plane. Clearly, something must be done to decrease the wiring congestion immediately under the chip. Today, this is done by the

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addition of more wiring planes to redistribute the congestion to lower wiring levels (Blodgett, 1983).

As more ECL circuits are crowded onto each chip, and since the system designers are reluctant for performance reasons to reduce the power needed per circuit, the power required and that must be dissipated per chip goes up. For reliability reasons, the maximum junction temperature on the chip must be limited to about 85 or 90°C. Assuming that the ECL circuits need 2 mW and that there are 20,000 circuits per chip, the power required per chip is 40 W. If the MCM contains 100 chips, the total power required by the MCM is 4000 W. If the power supply voltage is assumed to be about 2 volts, then the current required by the module is 2000 A.

The MCM of 1994 with 2,000,000 circuits will require about 5000 signal and power pins. The idea of separating the pins that supply signals from those that supply power by connecting bus bars to the MCM for the power and a smaller number and size of pins for the signals is not workable, because there must be ground returns for the signal pins. There is no requirement in 1989 for a ground pin for each signal pin; the ratio of signal to ground pins today is about 4 to 1. In the 1994 time frame, this ratio will probably decrease because of the steeper risetime of the signals expected at that time. The idea of separating the signal pins from the power pins is not a good one because at least the same number of signal pins is needed in each case. Certainly, smaller pins can be used if they carry only signal currents and not power-supply currents. It must be noted that a significant portion of the circuit current flows from other sources and in other directions, however, the current and pin problems are major issues to be dealt with.

Removing 40 W of power from a chip is a very challenging problem, as is removing 4000 W from the MCM. Since MCMs are quite expensive, they must be repairable. It must be possible to remove and replace chips on the MCM and to reroute signal paths, not only because of failure modes but because of the need for engineering changes. By 1994, engineering changes might possibly be made by external electrical signals.

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Chapter 3

Packaging Strategies and Associated Materials and Process Requirements

The increase in system performance that modern VLSI processing technology can provide usually is not realized because electronic packaging and assembly techniques practiced today negate much of the potential performance gain. The situation arises because the lengths of chip-to-chip interconnections on various packaging levels have not shrunk at nearly the same rate as on-chip interconnections, and the package-associated total wiring off-chip often exceeds the length of on-chip wiring by many times.

To minimize deleterious package effects, it is necessary to first reduce the average chip-to-chip interconnection length, i.e., chips have to be placed much closer to each other. It is also necessary to use materials with minimum dielectric constant for insulators in the interconnection network. Furthermore, circuit noise must be minimized, and there must be sufficient wirability at the various packaging levels to interconnect all the I/Os within a relatively few layers.

This chapter reviews current packaging approaches, with emphasis on the limitations that make them insufficient, and projected future packaging strategies, with focus on the packaging materials and processes that are required to make them a reality. Comparisons of packing density, performance, and cost are made for various approaches.

PRESENT PACKAGING APPROACHES

The two main approaches currently used in the United States to achieve high-density electronic packaging are the printed wiring board (PWB) approach and the thick-film multichip module (MCM) approach using ceramic and polyimide dielectrics. In the PWB approach, single-chip modules (SCMs), the first packaging level, are assembled on a printed wiring board, the second packaging level, as individual packages by either through-hole or surface mounting using soft solder joints. In the thick-film MCM approach, on the other hand, multichip modules contain multiple bare chips jointly packaged in a ceramic package that is constructed by multilayering thick film conductor layers and ceramic dielectric layers. It is these MCMs (level 1.5) that are then in turn mounted on the PWB (second level). A third technique employed by NEC (Japan) since 1983 uses successive thin-film wiring layers.

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Single-Chip Modules on Printed Wiring Boards

In the PWB approach, a printed wiring board is used with multiple x and y conductor planes appropriately spaced between ground and power planes. The conductor run width is typically 5 to 10 mils, and the thickness is of the order of 1 mil. The epoxy-glass dielectric layers are typically 5 mils thick. Plated through-holes (PTHs) connect the various conductor planes and are arranged on a regular grid with a hole-to-hole spacing of 100 mils. Chip dimensions are conventionally discussed in terms of micrometers (μm). Printed wiring interconnection structures are usually described in terms of mils, i.e., 0.001 in. Advanced interconnection structures may involve both units. One mil is equal to 25.4 μm.

Geometric Limitations: To increase the packaging density, the systems designer attempts to place the semiconductor packages as close together as possible. The interconnection vehicle, the printed wiring board, is normally offered with a 100-mil PTH grid and a wirability in the neighborhood of 40 lines per inch per layer. Many interconnect layers are possible, but 2- to 8-layer boards are most common.

Since each package pin must normally be connected to one PTH, the packaging density is limited approximately by the PTH density (i.e., 100 pins per square inch). Thus, a 100-pin package occupies at least 1 square inch, even if the package outline per se is much smaller. Pin grid arrays (PGAs) are the most efficient, since the pin spacing on the package exactly corresponds to the PTH grid on the board. Of course, not all PTHs on the board may be occupied by package pins, since a rim of about 250 mils must be kept open around each package to facilitate package mounting, removal, access to test pads, engineering change capability, decoupling capacitors, etc. Surface-mounted, peripherally-leaded packages can be just as density-efficient if the package leads can be wired to the PTHs underneath the package. This normally is possible unless the package pin count is too great or the lead pitch is too coarse. The reason is that, to be able to route underneath the package to reach the appropriate PTH, most of the conductor runs must squeeze between two PTHs on the distribution layer of the board. If a surface-mounted package has more than 256 pins, then, because of the maximum permitted wiring density of 40 lines per inch, the innermost PTHs underneath the package can no longer be reached, and at least some package pins must be routed to PTHs outside the package outline.

This is true for square package outlines. If rectangular outlines are used for surface-mounted packages, a packaging density equivalent to that for PGAs can be achieved, provided that no more than 64 pins are placed on the short edge and the pin spacing is not larger than 25 mils. Since the PTH grid is the ultimate factor that limits the packaging density in any case, a pin pitch less than 25 mils for square-mounted packages is unnecessary, because this will not lead to increased density on a 100-mil PTH grid board. Thus, even "chip-on-board" packaging techniques do not lead to a higher packaging density.

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Board assembly of surface-mounted packages with lead pitches as fine as 25 mils already presents many problems, such as lead control, solder control, placement accuracy, and inspectability. These factors may force the use of coarser lead pitch (e.g., 50 mils), if the number of PTHs contained in the area underneath the package exceeds the number of package leads. Even when optimum outlines are used, only about 50 to 75 percent of the available PTH grid can be occupied by package pins.

Clearly, higher packaging density can be achieved with a PTH spacing of less than 100 mils, but a finer grid is not easily achieved because of the required hole-drilling position accuracy, which is particularly critical in multilayer boards. Furthermore, PWB technology is a well-entrenched manufacturing technology in which considerable investment has already been made. It is likely that there would be resistance to the introduction of new techniques that require drastic manufacturing changes. The introduction of more blind vias also can lead to somewhat higher density.

Pin Limitations at the Interface to the Next Packaging Level: The systems designer normally is constrained to present a relatively small interface to the outside world. Thus, a state-of-the-art printed circuit board today is typically limited to a 200-to 400-pin interface to the next packaging level, depending on board size and edge-connector technology.

Since even 2 or 3 VLSI chips together can exceed this number of I/Os, a significant number of chips can be interconnected on the PWB only if the pin-to-gate ratio can be drastically reduced, normally well below that predicted by Rent's rule. For example, for an array processor design using a mix of 100 VLSI logic and memory chips for a total of 4.36 million gates, the designer is presented with 8600 signal I/O and power and ground pins on the chip level. These must be reduced to a few hundred by a proper interconnect design. Perhaps 200 of these can be brought out through the board edge connectors to the backplane. The remaining pins must be interconnected on the board.

This pin reduction is achieved by interconnecting the appropriate mix of logic, memory, and glue chips, i.e., counters, latches, shift registers, and multiplexers. Although this is usually done at the expense of the number of available data paths, some performance loss is recouped because of shorter interconnections and fewer required PWBs, backplanes, and cables.

Rent's rule can be broken at any level of integration. The microprocessor chip is an example of the breaking of Rent's rule in its original form for gate arrays on the chip level. The multichip-module approach to packaging, on the other hand, allows a delay in breaking of Rent's rule until a much higher level of integration is achieved. This is always an advantage because it preserves many parallel data paths, even at very high levels of integration, and thus offers higher systems performance and greater architectural flexibility.

Materials Limitations: Considerable differences exist in the thermal coefficient of expansion (TCE) between the PWB and the common first-level packages. Thus, the TCE of an FR-4 PWB is 17 ppm in the XY direction and 60 in the Z direction. Both of these are higher than the TCEs encountered in

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most packages, particularly the ceramic packages that are normally used to house high-pin-count VLSI chips. These differences cause large plastic strain excursions between board and packages and can lead to metallurgical fatigue in the solder joints and the copper in the plated through-holes. There is also the tendency of the PWB to warp during assembly because of the use of low-T_g polymers.

Thick-Film Multichip Modules Using Ceramic Dielectrics

An alternative approach to the density problem is to insert another packaging level between the single-chip module (level 1) and the printed wiring board (level 2), namely the multichip module (MCM), often called level 1.5. The added level is not limited by the PTH grid and thus is capable of a much finer interconnection grid and much higher wirability than the printed wiring board, and it can also provide most of the interconnections between chips. This greatly reduces the interconnection effort required at the PWB level. Chips can be placed much closer together, and, in fact, there is normally no room for first-level packages at all; bare chips directly bonded to the MCM substrate must be utilized.

In the multichip module, bare chips are interconnected on a substrate with substantially finer conductor lines, smaller dielectric thicknesses, and denser via grid than on a board. In addition, the substrate is not subject to conventional PWB design rules and assembly restrictions. Multichip-module technologies can be grouped roughly into thick-film multichip modules using ceramic dielectrics and thin-film modules using polymeric dielectrics. The thick-film approach has been used extensively in the past, whereas the thin-film approach is just emerging. (The thin-film wiring approach has been employed extensively by NEC.)

The thick-film approach is in turn divided into two groups, the multilayer hybrid and the co-fired ceramic and conductor block. In the first, the thick-film multilayer hybrid, both the metallic conductor layers and the dielectric layers are applied by silk screening. The appropriate metal or dielectric ink is applied to a sintered ceramic substrate by use of a squeegee through thick-film screen masks that define the location of the conductor runs and vias. After screening, these layers are fired at temperatures from 650 to 950°C. The metallic thick-film inks normally contain noble metal (Pt, Au, Ag, Pd) particles and glass frit particles suspended in an organic binder. The glass frit anchors the metal particles firmly to the substrate during the firing process in an oxidizing atmosphere. Non-noble metal (Cu, Ni) inks are sometimes used instead of noble ones. These employ fluxes, such as CdO, to ensure adhesion to the substrate, but must be fired in a nonoxidizing atmosphere to avoid tarnishing the metal. Generally, control of the firing process is poor. Dielectric inks contain glass and ceramic particles that fuse together to give continuous, nearly pinhole-free films. Many layers can be printed and fired in this way; however, yield considerations generally limit this approach to about 12 layers or fewer.

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While the thick-film multilayer approach has been used to interconnect VLSI chips, either as bare chips or packages in ceramic chip carriers, it can achieve only modest packaging density. Some of the reasons are:

- insufficient wirability;
- poor registration accuracy;
- poor electrical conductivity of the conductor runs;
- high-dielectric-constant insulators;
- insufficient substrate flatness.

The thick-film multilayer approach has found its most significant application in linear circuits where thick-film resistor functional-trimming requirements make this approach cost-efficient.

The second thick-film, multichip approach currently in use employs a co-fired ceramic multilayer substrate that contains multiple conductor and dielectric levels fused into a three-dimensional block. Because of its mechanical stability, this approach has seen extensive application in high-density digital packaging, principally for central processors in computers. A packing density of 25 percent of a "solid block" is possible, although many tens of layers are required to achieve this. However, still greater densities are becoming more difficult because of the following:

- The refractory metal ink conductor line must be fairly wide (10 mils) to ensure sufficient electrical conductivity.
- As many as 50 layers have been manufactured, but the process is increasingly costly as layers are added.
- After firing and the resulting shrinkage, the location of any particular feature on the fused substrate is known only with limited accuracy.
- Flatness control is difficult.
- The process is feasible only in high-volume production that requires large investments.

FUTURE PACKAGING STRATEGIES

A successful packaging strategy will have to embody the following features:

- much higher functional density,
- managing very high pin counts,

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- distributed power supplies to allow high-voltage power delivery,
- many simultaneously switching I/Os,
- heroic cooling approaches at higher power densities and less space allotted for the cooling fluid,
- some approach for high-density Z-direction wiring,
- more serial data transmission by optical, microwave, or other links for data communication over longer distances,
- optical clock signal distribution to control skew, and
- reasonable costs.

The fundamental building block is the replaceable high-density module, mounted on a second-level board. Packaging approaches will differ from each other principally in the choice of the multichip module alternatives. The two most important alternatives are the thin-film multichip module and wafer-scale integration.

Thin-Film Multichip Modules Using Polymeric Dielectrics

The new packaging approaches now emerging, intended to increase the packing density to well above 25 percent, all attempt to employ processes analogous to those used in the processing of the VLSI chips themselves. In particular, the interconnecting conductor pattern is deposited by thin-film deposition techniques that are amenable to photolithographic definition and etching to achieve much higher wirability than was possible for the thick-film approach. Thus, the thin-film conductor width and the spacing between them is typically 1 mil or less, and the via grid is on a 10-mil pitch; this is an order of magnitude finer than ordinary wiring boards. The resulting increased wirability makes it possible to interconnect even the most densely packed structures with only 2 (at most 4) interconnecting conductor layers, in addition to power and ground planes. Dielectric layers between these closely-spaced conductor runs must also be about 1 mil or less.

To achieve this uniformly over a large substrate area and achieve planarization at the same time, thin (1-mil) polymeric dielectric layers are spun or sprayed on between the conductor layers. Polymeric films have the added advantage of a lower dielectric constant (2 to 4) that allows faster signal propagation. Silicon is often the substrate of choice (inspire of its brittleness, low current-handling capability, and difficulty in making many connections), because of the TCE match it provides, its superb thermal conductivity, and its compatibility with silicon chip processing equipment already in place. Not only does this reduce investment requirements, but the reliability is also expected to improve with the application to packaging of the processes that have proved their integrity on the chip level. Packing densities as high as 90 percent are projected. Table 3-1 summarizes some

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recently reported high-performance, bare-chip interconnect technologies. A specific example is shown in Figure 3-1, and additional MCM approaches are illustrated in Appendix F.

Table 3-1 Emerging High-Performance Multichip Module Interconnect Technologies

User	Substrate	Conductor W.T.P.*	Insulator	Chip Attach**	Module I/O**	Advantages	Disadvantages
Mosaic[1]	Silicon	Aluminum 11,2,22	Silicon dioxide	WB	WB	Vendor/Si chip Technology/ TCE match	High capacitance High resistance lines
IBM[2]	Alumina	Copper 8,6,25	Polyimide	SB	PGA	Low attach inductance/ substrate for PWR/GND	Heat removal
Honeywell[3]	Alumina	Copper 50,5,125	Polyimide	WB/TB	WB	Substrate for PWR/GMD	
AT&T[4]	Silicon	Copper 10,5,20	Polyimide	SB	PGA	Low attach inductance/ TCE match	Heat removal
Raychem[5]	Silicon	Aluminum 40,5,100	Polyimide	WB	WB	Vendor/TCE match	
GE[6]	Alumina	Copper 25,5,75	Polyimide	Overlay	WB	No masks/fast prototype/low attach inductance	Must remove overlay to replace chips
Livermore[7]	Silicon	Various	Various	Beveled chip edge	Various	Handle high pin count/TCE match	Beveling step limited line routing
MCC[8]	Alumina Silicon	Copper 15,6,50	Polyimide	TB	TB	Programmable interconnect	
HP[9]	Ceramic	Copper	Polyimide	No detailed data available			
Augat[10] (Rogers)	Copper Steel	Copper 100,25,250	Polyimide	No detailed data available			
NTT[11]	Ceramic	Copper 25,6,50	Polyimide	No detailed data available			
NTK[12]	Ceramic	Multiple 25,5,65	Polyimide	No detailed data available			
Mitsubishi[13]	Ceramic	Copper 50,5,100	Polyimide	No detailed data available			

References listed separately at end of table

* W = width; T = thickness; P = pitch; conductor dimensions are in micrometers. [Numbers are conservative reported values, not minimums.]

** WB = Wire Bond; TB = TAB Bond; SB = Solder Bump; PGA = Pin Grid Array.

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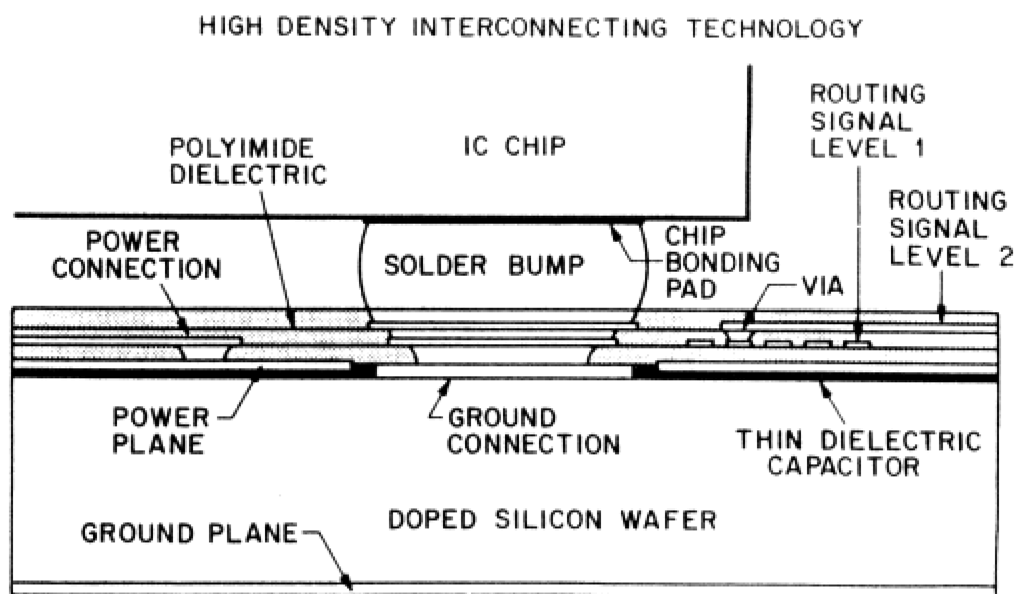

Figure 3-1
Cross-sectional view of AT&T AVP module.

For the highest frequency systems, MCMs represent a breakthrough in packaging. It is probable that this generic technology will come to dominate the packaging of components for the clockrate environment of higher than 100 MHz, with all present and intermediate future forms of circuit-board technology falling into disuse. Although there is already intense international activity in this area, further materials research, development, and application are strongly recommended.

The interconnect issues, which all of these high-density approaches using bare chips must face, are listed in below. In many cases, line-density demands conflict with requirements on crosstalk, yield, ease of fabrication, ease of repair and circuit changes, and cooling difficulty. The systems designer must understand the trade-offs involved in committing a circuit design to a module layout and in working closely with the circuit designer to understand systems requirements such as chip placement and I/O layout to the next level of packaging.

- Testability of bare chips to operational speeds.
- Use of CAD for chip placement and optimum interconnect layout.
- Low inductance power leads (ΔI noise).
- Yield in interconnect fabrication (opens, shorts, vias).
- Transmission line impedance control.

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- Line resistance (DC and AC line losses, including dielectric loss and skin-effect losses in conductors).
- Line capacitance to ground.
- Decoupling capacitors.
- Testability of interconnects.
- Testability of circuits to locate defective chips.
- Ease of change of interconnect routing.
- Repairability of interconnects.
- Reliability of interconnects under thermal and mechanical strain.
- Chip removal and replacement.
- Heat removal.
- Hermeticity, if required.
- Integrity of return current path.

Wafer-Scale Integration

Wafer-scale integration (WSI) implies an integrated circuit that, compared to state-of-the-art VLSI, has a quantum jump (not just incremental) in having more functions integrated on the same monolithic piece of silicon, much larger than a VLSI chip and normally of full wafer size. The attractiveness of WSI is in its promise of greatly reduced cost, high performance, higher level of integration, greatly increased reliability, and significant application potential. Among the advantages WSI promises are:

- lower cost per function because of a much higher level of integration and because of high yields made possible by fault tolerance
- higher performance because it leads to the highest possible packaging density of functions in a system and thus minimum interconnection lengths and signal delay. (This assumes that redundancy requirements will not negate the gains.)
- highest reliability because practically all interconnections in a system are by aluminum-metallization on silicon, which is inherently more reliable than other interconnection techniques, such as wire bonds or solder connections. (An additional dramatic increase in reliability can also be expected with the advent of self-reconfigurability, which makes possible failure tolerance, and transparency to systems operation.)

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- dramatically higher functional density in both an evolving IC technology development environment, such as GaAs, and in a mature IC technology environment, such as silicon.
- significant application potential both for regular structures, such as memory, and for irregular structures, such as random logic.

WSI cannot simply be looked on as a superchip that has larger dimensions than chips conventionally encountered in VLSI. The upper dimensions of a VLSI chip are normally determined by such factors as yield and defect density, allowable interconnection lengths (RC delay), or the dimension of available packages. For WSI, on the other hand, the most important characteristic is the requirement of massive testability and reconfigurability, referred to as fault tolerance. In other words, WSI greatly exceeds the ability to get a totally perfect circuit; that would be merely a large VLSI chip. Instead, WSI crosses into the arena of fault tolerance, with the attendant need for redundancy, constructability, and reconstructability.

The committee exhibited considerable divergence of opinion in the preparation of this discussion in regard to WSI. Negative aspects perceived by some members include the following:

- The need for circuit redundancy in a planar configuration seriously impacts performance and packing density.
- Open metallization lines on a chip reduce yield. Redundancy requires increasing the number of wiring levels.
- Present management of semiconductor facilities, which strives to maximize the number of good circuits per wafer, is not optimally suited to WSI production.

The majority of the committee concludes that WSI is unlikely to become an important interconnection strategy in the foreseeable future.

PACKAGING MATERIALS REQUIREMENTS

The required packaging improvements on all packaging levels are summarized in Tables 3-2 through 3-5 in the light of the VLSI chip technologies expected to be available in the future, as well as the future systems requirements. The latter include performance, electrical noise control, packaging density, reliability, and manufacturability.

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Table 3-2 Materials Requirements for Level 0 (On-Chip or Wafer Scale Integration)

	System Drivers				
VLSI Chip Drivers	Performance	Electrical Noise Control	Packaging Density	Reliability	Manufacturability
Large chips or wafers	Lower-temp. operation	Cross wafer communication, distributed	More functions per cm^2	TEC compatibility to substrate, keep small and matched	Fault and failure to lerance
100-psec rise and settling times	Lower ϵ dielectric, low ρ conductors	Ground planes on wafers, impedance control	-	-	Shielded connector
1000 I/Os	Multilayer signal lines	-	Superconducting connections	-	Damage control in repair; fault isolation, on-chip repair and rewiring, easy chip and wafer replacement
256 simultaneously switching I/Os	-	High ϵ decaps on wafers, distributed power supplies on wafer	-	-	-
High power density	-	-	No heat spreading on wafer	Bulletproof passivation for direct immersion cooling	Low-resistance joints
1.5-V power supplies	Low IR in power leads	Tight control of L, C, R	Distributed power supplies on wafer, high efficiency, power by light	-	-
3-D construction	-	-	-	Zero insertion force connectors	Vibration g-force immunity
Other	-	EMI sensitivity	-	-	-

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Table 3-3 Materials Requirements for Level I or 1.5 (Single-Chip or Multichip Modules)

	System Drivers				
VLSI Chip Drivers	Performance	Electrical Noise Control	Packaging Density	Reliability	Manufacturability
Large die size	-	-	High H, low R	TCE compatibility of die and substrate, fatigue	Void control and inspectability of die attach
100-psec rise and settling times	High λ conductors, low ϵ dielectrics, optical fibers	Distributed power supplies	-	Demountable 3-D construction (tight spacing)	-
1000 I/Os	1 mil pitch, 1:1 aspect ratio	Staked vias	Staked vias	TCE compatibility	Damage control in repair; solder control, outer lead bonding materials for TAB, engineering change pad periphery, planarizability
256 simultaneously switching I/Os	-	High ϵ decaps closely located near chip	High ϵ decaps	-	-
High power density	Low IR drops in signal and power lines	-	No heat spreading possible	If liquid cooling: corrosion, charge transport	-
1.5-V power	Low forward drops in power supply	Tight R, L, C control	High-efficiency power supplies, power by light	-	Low-resistance joining materials and processes
3-D construction	Shielded vertical conductors	-	-	Corrosivity of high materials, radiation hardness; hierarchy of sealing materials, adhesion, and purity control of plastics, outgassing, higher T_g s, nonhermetic enclosure	Materials to resist vibration, g-forces
Other	-	EMI, EMP radiation, upset radiation	-	-	-

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Table 3-4 Materials Requirements for Level 2 (Modules on Printed Wiring Boards)

	System Drivers				
VLSI Chip Drivers	Performance	Electrical Noise Control	Packaging Density	Reliability	Manufacturability
Large die size	Flatness requirement	-	High H, Low R	TCE compatibility of package to board, fatigue, barrel cracking	-
100-psec rise and setting times	Low ϵ boards, <13 mil hole sizes, thinner boards, optical fibers	Impedance control	Distribution power supplies	-	Demountable 3-D construction
1000 I/Os	Internal vias. Multilayer, i mil pitch, mounting of pin-grids.	-	Blind vias	-	Solder control, damage control in repair, engineering change pad periphery, 10-mil lead pitch, lead fragility and control, lead solderability
256 simultaneously switching I/Os	-	High ϵ decaps closely located near chip	High ϵ decaps	-	-
High power	Low IR drops	-	Heat spreading in 1st level package only, thermal vias, heat flow through board a long board. High efficiency power supplies, power by light	If liquid cooling: - corrosion, - board stability, - charge transport	-
1.5-V power supply	Low IR drops in power supplies	-	-	-	-
3-D construction	Tight board-to-board spacings	-	-	-	-
Other	-	EMI, EMF radiation upset	-	Corrosivity of Cu board coatings, deterioration in sliding contact surface	

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Table 3-5 Materials Requirements for Level 3 and Higher (Backplanes, Cables, Connectors)

	System Drivers				
VLSI Chip Drivers	Performance	Electrical Noise Control	Packaging Density	Reliability	Manufacturability
Large die size	-	-	-	TCE board to connectors, fatigue	-
100-psec rise and settling time	Optical fibers	Impedance control	-	-	-
1000 I/Os	-	-	Blind vias	Reliable demountable contacts	Tighter connector pitch, 3-D constructions, demountability
256 simultaneously switching I/Os	-	-	-	-	-
High power density	-	-	Lateral thermal conductivity, high-efficiency heat exchangers, plumbing, radiators	If liquid cooling: -corrosion, -compatibility, -charge transport.	-
1.5-V power supply	-	-	-	-	-
3-D construction	-	-	-	-	-
Other	-	-	-	Corrosion of Cu, protective coating, deterioration of demountable contacts	-

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SUMMARY OF FUTURE PACKAGING MATERIALS AND PROCESSES NEEDS

Future packaging needs are summarized below and include the following:

- Fusible link materials with reversibility;
- Materials for fuses and antifuses;
- Multilevel interconnection processes on silicon ;
- Thin and thick film magnetic materials for compact power supplies;
- Low-resistance contacts;
- Compatible power-device and digital-device processing;
- Minority-carrier quality GaAs on silicon substrates;
- Inner lead capability down to a 2-mil pitch;
- High-yield, high-reliability metallurgical microjoining techniques;
- "Bullet-proof" chip coatings of "hermetic" quality;
- Corrosion resistance of chip and package materials toward liquid coolants (e.g., water, fluorocarbons, liquid nitrogen);
- Very-low-resistance, maybe even superconductive, interconnections;
- High-and low-dielectric-constant materials in close proximity on the same substrate;
- Planarization processes;
- Solid vias;
- High-thermal-conductivity substrates;
- Metal-ceramic-polymer composites;
- Thermal expansion-matching materials and processes;
- Fatigue-free solders and die-attach materials;
- Solder flow and thickness control;
- Surface chemistry in relation to solder wetting;
- Lead corrosion, short-and long-term;

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- Inspectable joint materials;
- Fine lead control;
- Quantum jump in connector reliability;
- Connectors with lead pitches down to 10 mils;
- "Smart" connectors and mixed optical and electrical connectors;
- Packages with windows transparent in certain wavelength ranges;
- Method of coupling to incoming light beams;
- Shield conductors in Z-direction;
- Laser processes for multilayer fabrication;
- Benign repair processes; and
- Low-loss dielectrics at high frequencies (greater than 1 GHz).

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Chapter 4

Materials Issues

Materials science is an enabling technology that does not command interest for its own sake. Rather, materials issues play a key collaborative role in all matters of hardware design, fabrication, and performance. Thus, it is most effective to consider materials choices in the context of the physical design of specific packages and interconnection structures. In this chapter, relevant materials issues are discussed, emphasizing properties that are prime considerations in connection with the issues. It should be kept in mind that hardware is composed of combinations of materials, and the properties of the resulting complex are dominant in terms of performance. Materials compatibility is a critical issue, and interfaces count as much as bulk properties.

Process compatibility is also a major issue. Each of the materials that enters a piece of hardware must be robust in subsequent fabrication steps. This involves exposure to process chemicals and process environments that may not be apparent in the design itself. The effects can be less than obvious. For example, cure state of a polymer or the grain structure of a conductor can be significantly affected by process conditions that are not intended to modify previously-formed structures.

Stability in service is likewise an essential matter. Avoidance of corrosion, physical cracking, and other degradation or failure mechanisms is an important area of physical design in which materials properties play a central role. The issue of hermetic packaging is a materials-intensive one, and significant changes in practice and attitudes in this area can be expected over the coming years. Operating environment is a design factor best considered on a system level, but materials susceptibility to outside influence is often given too little emphasis.

Design trends associated with increasing density of electronic circuitry include the following items: Power dissipation per unit area or volume is increasing. This effect is a consequence of miniaturization of the chips and the packaging and interconnection strategies that pack more devices onto interconnect structures. As more circuitry is placed on each chip, it is inevitable that packages must evolve with an increasing number of I/Os. Certainly, several hundred I/Os from single chips appears certain. As circuit elements become faster and faster, the speed of the package and its interconnect transmission comes to be a critical limiting factor. Today, the time required to move information from one chip to another is longer than the switching time of circuit elements on chips, a limitation that is growing in importance.

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DISSIPATION OF HIGH THERMAL LOADS

The increasing density of electronic packaging is accompanied by increasingly high thermal loads that must be dissipated. Heat dissipation is one of the most serious problems that limits the further miniaturization of electronic packages. High thermal conductivity in electrically insulating substrates is most relevant to solving the heat dissipation problem. Ceramics, dominantly alumina, are currently employed as substrates in high-thermal-load structures. Organic polymer dielectrics, as alternatives, soften and degrade at high temperatures. On the other hand, ceramics have higher dielectric constants than polymers, which has an adverse effect on propagation speeds. Moreover, ceramics are more difficult to form or shape than polymers, requiring processing at very high temperatures. One approach to combining the most attractive features of ceramics and polymers is to use ceramic particles or fibers as fillers in a polymer matrix to form a composite. In general, however, there is an empirical inverse relationship between thermal conductivity and dielectric constant of substrate materials, as shown in Figure 4-1; some typical values are given in Appendix E. This suggests that a physical design that separates heat flow paths from signal propagation media will provide the most effective strategy in regard to dielectric materials. Metals are better thermal conductors and can play an important role in thermal management.

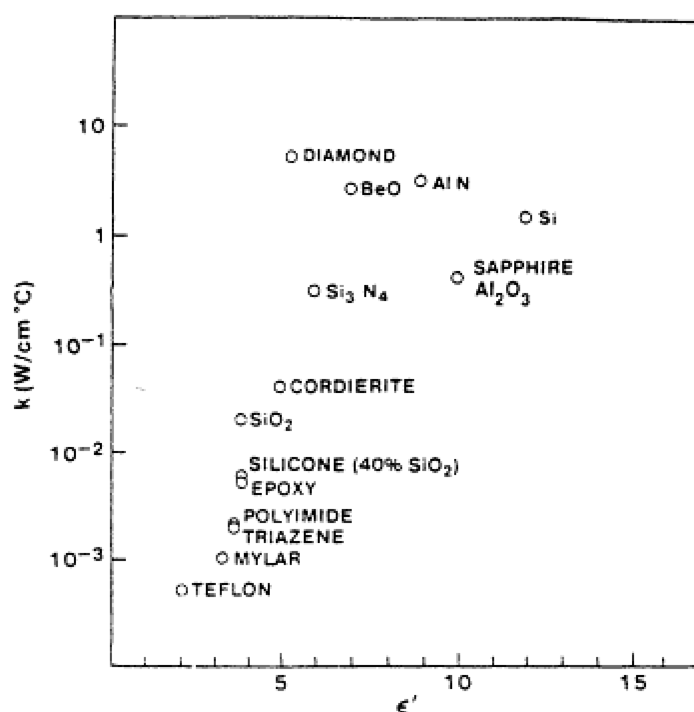

Figure 4-1.
Thermal conductivity-dielectric constant relationship of dielectric layer and encapsulation materials.

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The problem of thermal management, as it relates to the packaging of electronic devices, has been reviewed by Mahalingam (1985). Generally, it is assumed that the junction temperature of integrated circuits must be kept below about 90°C (this can vary from 60°C to 120°C depending on the application), and package, design, and heat transfer options are considered on this basis. Ability to remove heat depends critically on the type of package considered and on the commitment of the device to external cooling.

For molded plastic packages (DIPs, Quads), thermal conductivity (as opposed to electrical conductivity) has been the principal driving force for the shift from alloy-42 lead frames to copper alloy lead frames. Heat flows out of these packages mainly along the metal lead frame, and copper is an order of magnitude more conductive than alloy-42. This improvement can also be achieved by introduction of a heat spreader, a metal plate such as aluminum, molded into the package. Packages of this type can handle up to about 2 watts with no external cooling and 3 watts in forced air. The very low thermal conductivity of the plastic makes attachment of a finned heat sink relatively unattractive. The silica filler used in epoxy encapsulants is also a poor thermal conductor (see the relevant section in Chapter 5).

Chip carriers and pin grid arrays have the chip in a cavity, and thus the thermal path through the die bond and encapsulation material is very important. Ceramic materials are chosen because of their superior thermal conductivty in comparison with plastics. The "cavity down" configuration is chosen to vent the heat away from the PWB. Roughly speaking, 3 watts can be handled without forced air and up to 6 watts with forced air if no heat sink is attached. With a heat sink and forced air, 6 to 12 watts can be accommodated with an alumina carrier. With beryllia packages, the power level can be increased by about a factor of two, i.e., to 20 to 25 watts. The quality of the die bond is important in these packages because the presence of any voids will cause a large thermal impedance in the main heat flow path.

Very high power (greater than 1000 w) can be handled with structures mounted on a silicon substrate in which microchannels have been machined. Liquid is pumped through the channels as the heat-transfer medium. Kilowatt power levels may well be encountered in large, high-speed microprocessors. Values of specific thermal conductance of junction-to-ambient can be as low as 0.07 $W/cm^2/K$ for quite moderate junction temperature rises. The use of conventional liquid cooling is already established in mainframe computers. With intelligent engineering, such as is employed in table-top refrigerators, closed-circuit liquid cooling that uses microscopic heat exchangers should be an attractive approach to thermal management for high-performance desk-top work stations.

Polymeric circuit substrates are predominantly epoxies with glass reinforcement. Although the glass is introduced primarily to control thermal expansion, thermal conductivity also is improved. Continuous fibers work better than short fibers in all respects. Replacement of the glass with high-thermal-conductivity fibers (e.g., aluminum nitride) has been suggested but is very expensive. Research in this area could yield interesting composites. Metals are good thermal conductors compared to alumina, and their thermal conductivity can be enhanced further by incorporating continuous carbon fibers

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to form a metal-matrix composite. Because of the electrical conductivity of the metals, however, their use in substrates usually requires coating them with an electrical insulator, such as a ceramic or polymer film. For high-speed systems, the metal forms an essential reference plane. Coated metal substrates are valuable for applications that do not require operations that penetrate or degrade the dielectric (e.g., laser trimming).

Heat sinks are essential aids in the dissipation of heat, although those currently used are bulky and not very effective. Materials with superior thermal conductivities are needed (e.g., carbon fibers in composites). Improved thermal contact is also needed between the sink and the part to be cooled, and thermally-conductive adhesives (metal-filled epoxies), greases, and other media have been used. It is important to keep the bond layer thin and avoid delamination. New designs emphasizing efficient heat transfer, small volume, and low weight are needed. Hermetic chip packages consist of ceramic bodies with external leads sealed through the ceramic. The chip is mounted in the ceramic body cavity and electrically connected, usually by wire bonds, then a metal lid completes the seal. To improve thermal conductivity, there is a need to find a metal more conductive than the currently used kovar. Metal-matrix composites (e.g., carbon, silicon carbide, or aluminum nitride in aluminum) are promising candidates for further development. Elkonite, an alloy of tungsten and copper (80:20) that has high thermal conductivity and TCE matching silicon and GaAs, is used in high-frequency digital packages.

DIELECTRIC PROPERTIES

Substrates support both active and passive devices and also the interconnecting conductors that make up the substantial subsystems or the entire system. Discrete components integrated into the substrate also may be involved. Signal transmission from one chip pad to a pad on another chip is governed by the dielectric properties of the substrate or interlayer and the electrical conductivty of the metal strip. If the total resistance is low, signals will be propagated with the speed of light, with a delay that is proportional to $n = \epsilon^{1/2}$. Line termination is important to control reflections. If the resistance is large (greater than several ohms), transmission is slower and the effect of the dielectric constant exponent is even greater. Thus, the dielectric properties of the substrate play a crucial role in determining circuit speed. Detailed analysis of the transmission characteristics is highly specific to the geometry of the circuit.

Dielectrics chosen for substrates generally have low dissipation factors, and only the real part of the dielectric constant is important. Surface conduction and electrochemical reactions can constitute a circuit failure mechanism, particularly in high-humidity environments, and, as circuit lines are miniaturized, this problem becomes more important. Dielectric breakdown normally is not a problem in interconnections.

In printed circuit boards, hybrid circuits, and multichip modules, strip lines of various description occur. For example, in a multilayer board, a metal trace may have the substrate dielectric on one side and air on the other

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side, or a buried trace may have a dielectric on both sides. Adjacent power, ground, and signal lines have complex implications for impedance and crosstalk. In general, an intuitive average dielectric constant can be invoked to approximate the strip line characteristics.

Substrates fall into two classes, inorganic and organic, with ceramics (mainly alumina) dominant in the former and polymers (mainly epoxies) dominant in the latter. Alumina has a dielectric constant of about 9, and epoxy-based composites have dielectric constants in the range from 3 to 5. Thus, the speed of signal propagation on polymer boards is considerably faster than on ceramic. Although both classes have materials that offer lower-dielectric-constant substrate materials, polymers are more promising in this characteristic. Multichip modules are designed to make use of the best of both.

Beryllia (BeO) has been mentioned as an alternative to alumina ($A1_2O_3$), but mainly in the context of its thermal conductivity rather than its dielectric constant ($\epsilon' = 6.7$). Beryllia is toxic and requires special precautions during processing. It must be fired at high temperatures, a requirement that is inconsistent with co-firing with copper. Aluminum nitride (AlN) is another alternative to alumina, but it offers no advantage in dielectric constant ($\epsilon' = 8.9$). Glass-ceramic compositions based on cordierite have ϵ' between 5 and 6 and have the possibility of copper co-firing compatibility. This promising area is now receiving development emphasis. Foamed ceramics offer even lower ϵ', although they suffer in terms of mechanical strength and thermal conductivity. Even so, foamed ceramics deserve exploration.

New epoxy resins based on more highly functionalized materials now are being introduced for high-performance circuits when their dielectric constant is not the driving property. In view of the sophisticated (supercomputer) systems recently introduced based on epoxy boards, it must be concluded that epoxy resins in multilayer boards will remain dominant for the foreseeable future. Very advanced structures have been demonstrated (i.e., fine lines and many layers), and the processes employed are familiar. Other polymers with lower dielectric constant are available but are less well accepted. Many polyimides of varying chemical composition have been studied. In general, the polyimides have dielectric constants in the range of 3 to 4, but this varies considerably with humidity. High frequency dielectric loss is a negative factor in dielectrics that absorb water. Fluorinated resins have lower dielectric constants, as low as 2 for polytetrafluoroethylene. Cyanate (ϵ' about 2.8) and benzocyclobutane (BCB) resins (ϵ' about 2.7) lie in between those mentioned. An interesting cyanate resin-polytetrafluoroethylene fiber composite has been made available in sample quantities (ϵ' about 2.6), but the price is prohibitive at this time for general use. The search for low-dielectric-constant materials continues among a variety of candidates, but a great deal of development work is needed. Materials with high dielectric constants at high frequencies are necessary for power-supply decoupling. Their incorporation in substrates would be a worthwhile direction for the future.

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INTERCONNECT VOIDING

The reliability of interconnections on integrated circuits on chips is degraded often by the process of electromigration. In this phenomenon, small circuit traces develop cracks or voids when carrying high currents for substantial periods. Although this phenomenon is not completely understood, empirical studies have led to design rules for selection of alloys that minimize the problem. As interconnection traces on multichip modules are further miniaturized, electromigration may again cause problems.

A separate, but closely related, problem involves conductor voiding, which is driven by mechanical stresses in the metal. This phenomenon is less well characterized than electromigration and could become a design problem at module-conductor dimensions; it is most likely to occur in low-melting, ductile materials, e.g., PbIn. The committee could identify no example of voiding problems of this nature in interconnect structures, as yet.

THERMAL FATIGUE

Interconnect structures are complex assemblies of various materials separated by interfaces. Adhesion varies widely in going from one layer to another, and the coefficient of thermal expansion differs from one material to the next. As a consequence of these differences, stresses are generated as the temperature is changed, and the stress will be proportional to the physical size of the interface and to the temperature difference from some state of low stress. Thus, a silicon chip with an attached metal alloy lead frame which is transfer-molded in a silica-filled epoxy, will develop stresses as the assembly is cooled from the molding temperature to room temperature. In some cases, the stresses can be sustained by the material system, but in other cases the stresses cause the package to warp, twist, or deform. Finally, the package may fail completely by the cracking of the chip or the encapsulant or by delamination of the interfaces. Temperature cycling, employed in device testing, exercises the structure repeatedly and increases the probability of mechanical failure. Compliant layers can decrease thermal stress. Also, TCE matching can be approached through use of composite materials.

Designers must, therefore, have extensive knowledge of materials properties and the nature of interfaces to ensure stable and reliable interconnection structures and packages. The analysis of actual structures is exceedingly complex, even in relatively simple systems, and much design lore and structural approximation are employed. Intuition is often faulty in this area; for example, thermal fatigue of soldered joints is complicated by solder creep.

INTERFACIAL PROCESSES

Adhesion and bonding are required at virtually all interfaces within an interconnect structure. Stresses in the structures are mitigated when they are distributed over well-adhered surfaces, but delamination results from

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stress concentrations that can cause fracture, which allows subsequent rapid moisture ingress. An understanding of the fundamentals of adhesion among the common packaging materials is clearly incomplete. Although adhesion is well controlled and optimized in most present designs, there are still many cases where adhesive failures occur.

As new materials are introduced, each new interface will need detailed study for adhesive reliability. Although computer design aids and greater understanding of adhesion will improve design effectiveness, it is doubtful whether new materials or processes can be introduced without an extensive testing program. As an example, epoxies bond well to many different surfaces, but moisture ingress, poor design, or surface changes can weaken its adhesive strength. Hydrocarbon and fluorocarbon polymers, on the other hand, are inherently difficult to bond. Polyimides have been adapted to meet interconnect requirements, and new adhesive forms are available. Interdiffusion processes are of less concern for interconnects than they are for chips, but other long-term phenomena, such as physical aging and migration of additives to the interface, are still of concern. Lower-temperature processing will be of some help, but the higher operating temperatures of high-power devices will exacerbate these phenomena.

HIGH-TEMPERATURE STABILITY AND CHEMICAL REACTIONS

Interconnection and packaging materials are tested at temperatures ranging from-40° to +150°C; temperatures experienced in use are usually well within this test range. However, fabrication process temperatures can reach 350°C. Ceramics are exceptionally stable in this context. Most metals do not pose problems, but solder creep is a special issue. This may be addressed by the development of creep-resistant composite solders or solderless connections involving directionally conductive composites. Nevertheless, it seems safe to predict that solder will remain the dominant electrical joining material for the foreseeable future. Epoxies also are well behaved if formulated and cured correctly, but epoxies deteriorate in time. Other polymeric materials may deteriorate with time as a result of oxidation, hydrolysis, and photochemical effects, although this is not usually a major issue in packaging. Polyimides are a special problem when produced as solvent-cast dielectric layers. The polymer is soluble only in the polyamic acid form and must be thermally cured to the polyimide after casting. It is important that the copper be protected from the polyamic acid during curing (e.g., with the use of chromium).

TRACE RADIONUCLIDES IN PACKAGING MATERIALS

The importance of radiation-induced upsets (charged with particles entering and affecting the crystal structure) in microelectronic devices has become increasingly important as memory size has diminished. Some commercially-available dynamic RAMs function with about 10 million charge carriers per bit, or about 1 picocoulomb of charge. An alpha-particle (He) incident in this region of a memory may create a sufficient number of local carriers to disrupt bit storage at that level. This effect was first observed about a decade ago and has been the subject of several investigations. It has

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been found that very low levels of uranium and thorium can create such upsets, and it is recognized that essentially all materials contain these elements at part-per-billion levels. The problem can be particularly significant with some materials; e.g., alumina typically contains uranium at levels of about 100 ppb and requires the shielding of the active chip surface. Fortunately, alpha particles have a very short propagation range in dense matter. Silica filler used in plastic-molded packages is also an obvious source of alpha emission close to the chip surface. Suppliers have solved this problem by developing a low radionuclide silica, now synthetically produced. Cosmic rays also can give rise to the same problem, but, in this case, there is no way to shield the memory circuit. Thus, it is necessary to resort to circuitry solutions involving error-correction techniques.

ELECTROMAGNETIC INTERFERENCE

Along with the increasing sensitivity and abundance of electronics is the increasing severity of electronic pollution. The shield for electromagnetic interference (EMI) is necessary for connectors, cables, chassis, cases, etc. Metals, particularly aluminum, are most widely used for EMI shielding. They can be in the form of sheets, coatings, etc.; however, metals are not easy to shape compared to polymers and are relatively heavy. Moreover, coatings can be scratched and hence can degrade their shielding effectiveness. Polymer-matrix composites containing electrically-conductive fillers (e.g., graphite) are moldable and can be comparable or even better than metals in their EMI shielding effectiveness, particularly at high frequencies. More work is needed in the development of such polymer-matrix composites.

High-temperature superconductors are potentially valuable for EMI shielding, although the need to cool to below the critical temperature (T_c) limits their usefulness. Nevertheless, superconductors may have unusual shielding capabilities and deserve attention.

ENCAPSULANTS AND HERMETICITY

Hermetic packages are intended to provide complete protection for the integrated circuit chip from all external influences. In practice, this usually implies the exclusion of all forms of water from the active silicon chip and its lead frame. In fact, chips are passivated by a thin glass layer (usually Si_3N_4), but an external, robust package is required for high-reliability applications. Suitably prepared ceramics and metals are impermeable to gases and can produce effective hermetic packages. Typically, the chip is bonded inside a ceramic body cavity, and a lid (metal or ceramic) is attached with a glass or metal seal. Ceramic-to-metal seals that can withstand thermal cycling are needed. All polymers are permeable to gases and thus are unsuitable for hermetic packaging components.

Hermetic packages are expensive and involve lead impedances that make substitution options a matter of considerable interest. There is further concern that many so-called hermetic packages are in fact leaky. One

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alternative is the use of silicone coatings that passivate the active silicon surface. These materials are permeable to water vapor, but they preclude the formation of liquid water on the inner surface and thus eliminate corrosion reactions. At present, these material coatings have not been accepted as substitutes for hermetic packages, but extensive test programs are being actively pursued to provide data that could justify substitution. There are strong and highly divergent opinions on this issue that are unlikely to be completely resolved across the board in the near future. (See the section on "Military Packaging" later in this chapter.)

MATERIALS-RELATED RELIABILITY ISSUES

Packaging and interconnection reliability issues are usually related to materials chemistry failure mechanisms. As circuit density increases, many of these mechanisms will be exacerbated. The focus in this type of failure mechanism is on combinations of materials—e.g., corrosion by galvanic couples, stress concentrations from thermal expansion mismatches, and loss of interfacial adhesion. Environmental factors in service usually center on water penetration, particularly when salts are present. Exposure to solvents, wide temperature excursions, mechanical shock or deformation, and particulate contamination also are significant. Assembly processes (e.g., solder reflow for surface-mount devices) can subject packages and interconnections to more severe conditions than those encountered in product use.

Corrosion is a persistent threat that is minimized by eliminating ionic impurities from the materials. Epoxy molding compounds were once a major source of chloride contamination, but resin suppliers have significantly reduced the problem. Soldering operations involving fluxing can cause impurity entrapment that often leads to long-term corrosion and eventual circuit failure. The presence of ionic impurities with clustered water is particularly serious, since they form an electrochemical cell that rapidly accelerates corrosion. Conditions conducive to water clustering, such as voids or delaminated interfaces, must be prevented. This once again indicates the importance of interfacial adhesion in promoting device reliability.

Corrosion is a widely occurring phenomenon that affects most metals. Specifically, the copper commonly employed in lead frames, printed circuit boards, connectors, wire, and cable is subject to corrosion. In general, liquid water must be avoided. This is more difficult than it may seem because of the common presence of salts, and it will begin to condense at about 70 percent RH when salt contaminants are present. Thus, it is necessary to clean all parts carefully and prevent subsequent contamination. Gold may be used for very high-reliability circuits. Silver is employed in some cases, but sulfiding and migration are problems. There is no very effective method to test for corrosive agents, and accelerated thermal aging does not suffice. Interfaces with imperfect adhesion often become the sites for concentration of corrosive action (e.g., on the glass reinforcement in epoxy multilayer boards).

Metal connections in some cases can interdiffuse and form brittle intermetallic compounds (e.g., aluminum and gold), and this continues to be an

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important problem in packaging and interconnection (Harman and Wilson, 1989). It is extremely important to form good bonds in component manufacture and assembly, and a great deal of engineering knowledge has been amassed in this area. As wire bonding becomes inadequate for high I/O chips, this area will be a central issue for an alternative technology. TAB is an alternative candidate that has been available for many years, but there still are significant remaining questions in regard to effective chip bonding. Even now, the future of TAB is uncertain. Wire bonding, nevertheless, could continue to be important for several years.

MILITARY PACKAGING

The military environment is one that puts great emphasis on packaging technology. There is a requirement for operation and survival in extreme conditions of high and low temperatures, high humidity, temperature cycling, etc., all of which are identified in military specifications to which military electronic packaging must be qualified (e.g., MIL STD 38510 group D tests on individual device packages). More generally, there are requirements for conformance to package outlines and packaging materials within the framework of denser packaging (more gates per cubic inch) and lighter packaging (more gates per pound).

As a result of extensive tests of transistors in a variety of package types evaluated for survival in high-moisture ambients dating back to the 1950s, most military systems include a requirement for hermetic packaging. Every package incorporates a cavity around the active chip, and that cavity is tested for leaks to the outside environment. Ceramic and metal packages meet that requirement and have been used in military systems, to the exclusion of plastic packages, for the past 30 years.

Because of the desire for maximum packaging density, there is a tendency to use flat packs rather than dual-in-line packaging. Similarly, in recent years, when the push for closer lead spacing and higher lead counts has put pressure on military packaging, leaded and leadless chip carriers, surface-mounted to high-density printed circuit boards and to ceramic modules, have become dominant in military systems. Such packages permit lead counts up to 400 and lead spacings down to 20 mils. Indeed, such high-density modules have been standardized under the Standard Electronic Module (SEM) title in sizes from 2 by 5 in. to 5 in. by 5 in. Multiple ceramic modules are then mounted on larger printed circuit boards as required. The modules are partitioned to permit module pin counts only slightly higher than individual device pin counts.

Military system designers are increasingly concerned with the penalty paid by adhering to requirements for hermeticity, and activities are under way (specifically by the Air Force Wright R&D Center, Attn: S.E. Wagner) to provide assurance that polymer-based systems can be used without any significant reliability impact as they are being used in commercial and industrial systems (Wong 1988). Such systems involve barriers to contaminants on the chips and strong bonding of the polymer to the chip surface, so that motion by mobile ions in surface moisture layers is impossible. The

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acceptance of such systems will result in substantially higher density, since the sealing structure uses a great deal of surface area. Simultaneously shifting to chip-type lithographic techniques will permit multilevel interconnect layers under or over multiple chips on a single substrate, so that the chips can be placed almost butting each other. The replacement of wire bonds by techniques that apply many bonds simultaneously (e.g., tape automated bonding, flip chips, or other techniques) will permit significant improvements in module reliability, since the wire bonds are still a relatively fragile interconnection methodology.

One of the areas of greatest importance in the packaging hierarchy is the power supply. Military systems generate and distribute power at 20 to 50 volts. Locally, there are power converters that convert the power to the 5-volt level that is most usually required by chip circuitry. Recently, the faster switching parts and the tendency for many gates and drivers to switch simultaneously has resulted in a desire to do power conditioning at the second package level and to use decoupling capacitors to further stabilize the supply voltage at the chip terminals. Small, lightweight, high-frequency switching supplies are responsive to this requirement, and they are appearing in new military systems. The ability to cool such distributed power converters is an important aspect of modern military system packaging structure design.

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Chapter 5

Some Specific Materials

In this chapter, several specific materials or classes are described. These examples will give a flavor of the complex compromises that must be made in optimizing material and process choices. Even so, the presentation is simplified, and it should be emphasized that materials engineering for packaging and interconnection follows requirements set by system design considerations. Thus, at any given time, system needs may put pressure on a specific property. Cost, in general, is a critical issue, although it is not susceptible to treatment in a report of this type. Cost is both volume-and process-dependent, further complicating the material design choice.

THE EVOLUTION OF EPOXY MATERIALS IN PLASTIC PACKAGING

Various epoxies have been developed in recent years, and today they play an important role in electronic packaging. The following sections cover some of the special features and how they can be modified to meet specific needs.

Epoxy Versus Silicone Materials

The earliest materials used for plastic packaging of microelectronic devices were silicones because of their high-temperature performance and high purity. The common bisphenol-A (BPA) epoxies were introduced that have lower glass transition temperatures (T_g). Novolac epoxies are generally preferred over BPA materials because of their higher functionality and attendant improvements in heat resistance. However, epoxies can have high ionic impurity levels because their reaction chemistry uses an excess of halogen-containing epichlorohydrin. Hybrid encapsulant materials consisting of epoxies and silicones captured a large segment of the molding compound market in the mid-1970s because they combined some of the high-temperature performance and the high purity of the silicones with the mechanical properties and the solvent resistance of the epoxies. Molding compounds since then have moved steadily toward all-epoxy systems, as the high-temperature novolac materials were improved and the ionic impurity levels were driven below 100 ppm. Figure 5-1 charts the property and process evolution.

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	1970 — 1980 — 1990
DRAM	16K, 64K, 256K, 1M, 4M
LOGIC (# GATES)(CMOS)	0.1K, 1K, 10K, 100K
	FLAME RETARDED; LOW IONIZABLE CHLORINE; LOW STRESS; LOW α- EMISSION
	ANHYDRIDE CURE; AMINE CURE NOVOLAC; STRESS MODIFICATION; SYNTHETIC SiO_2 FILLER
THERMAL STRESS (MPa)	12, 8, 5, (< 2)
THERMAL EXPANSION ($\times 10^{-6}$/°K)	25, 22, 19, 17, (< 14)
IONIZABLE CHLORINE (ppm)	1000, 100, (< 100)
U/Th CONTENT (ppb)	100, 10, (< 1)
FLAME RETARDANCY	UL-94 HB, UL-94 V—O
CURE TIME (SECONDS)	140, 120, 90, 60
MELT VISCOSITY (POISE) (MIN.)	2000, 800, 500, 300
MOISTURE SENSITIVITY (REL.)	1, 5, 10, 30
TEMPERATURE CYCLING (REL.)	1, 10, 100, 500

Figure 5-1.
Property improvement history of epoxy encapsulating compounds, 1970-1990.

Low-Stress Materials

A major advance in epoxy molding compounds was the development of the low-stress materials in the early 1980s. Package cracking, passivation-layer cracking, and circuit-pattern deformation can all result from the disparities in the coefficients of thermal expansion among chip, plastic package, and metal leadframe. This problem was exacerbated as the surface area of memory devices with 64K and 256K DRAMs became a significant fraction of the package itself. The plastic edge thickness became thin, and cracking began to occur. To alleviate this problem, the low-stress molding compounds combined several approaches. Fillers with different size and shape distributions were used to increase the filler loading to over 72 percent by weight, thereby reducing the coefficient of thermal expansion by as much as 25 percent (21×10^{-6} to 16×10^{-6} in./in.°C). The second advance was the addition of elastomeric modifiers in a dispersed domain morphology, which improves toughness. Research on the size, size distribution, and interfacial region was a major contributor to the improved performance of these materials. It is at this point that the Japanese suppliers surpassed the domestic suppliers in molding compound performance.

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Low-Alpha Materials

Alpha particles emitted from the silica fillers can cause soft errors in memory devices. The development of molding compounds that were low-alpha-particle emitters was a major advancement. Although these materials were available from the late 1970s, the silica was from the few mines that had low natural uranium and thorium contamination. Supplies were scarce, and prices were much higher than conventional materials ($25/lb compared to $3.50/lb). The use of synthetic silica in the early 1980s reduced the price of low-alpha materials to $10/lb by 1986. These materials quickly captured the market for memory devices, effectively eliminating silicone rubber in applications where it was used for alpha-particle protection.

Processing Improvements

Processing improvements also were required to keep pace with the increasing demands of higher-pin-count packages. The 40-pin DIP of the early 1980s was the first design to experience significant flow-induced stress problems. The long cantilever of the leads and the close proximity of the wire bonds made the package much more susceptible to lead movement, paddle shift, and wire sweep; the forces are proportional to the product of the material viscosity and its velocity. Japanese suppliers led the way in developing materials that had significantly lower viscosities than the previous generation of materials. The introduction of fine-pitch packages and thin leadframes has continued to push the need for very-low-viscosity molding compounds. The viscosity at the molding temperature has been reduced from 1500 poise in 1980 to 300 poise (at 100 sec^{-1}) in 1988, while both the filler loading and crack resistance of the material have been increased. It is also significant that the cure time for epoxy molding compounds has been reduced from 3 to 4 minutes in the mid-1970s to 60 to 90 seconds in the late 1980s, thereby contributing an important productivity increase.

Market Shares of the Major Molding Compound Suppliers

Japanese firms now hold 70 percent of the world market share in epoxy molding compounds for IC packaging. Less than a decade ago, U.S. companies had the majority of the market. This substantial U.S. market share advantage waned with the introduction of newer low-stress epoxy novolac materials. High purity, low viscosity, and low shrinkage stress were the major technology areas where the domestic suppliers fell behind.

FUTURE TRENDS IN PLASTIC PACKAGING MATERIALS

Advancements are needed to meet the challenge of future high-density packaging requirements. Some of these are discussed in the following sections.

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Surface-Mount Technology

Surface-mount attachment of IC packages will grow very rapidly over the next five years. The use of vapor phase and IR reflow solder methods for surface-mount devices exposes the entire molded body to high temperatures that can cause cracking through two different mechanisms. The first is by the thermal shrinkage forces already discussed. Continued reduction in the coefficient of thermal expansion, reduction of the glassy modulus, and additional improvements in adhesion will be needed to prevent thermal-shrinkage stress cracking of the molded body.

The second crack mechanism is through rapid vaporization of moisture within the molded body, which causes volume expansion above the glass transition temperature (T_g) of the plastic package. To alleviate this serious problem, there are four possible material improvements that could be made: a) lower the moisture uptake of the molding compound, b) increase the T_g to near the solder reflow temperature, c) increase the mechanical modulus above T_g to minimize high-temperature deformation, and d) improve adhesion to the bottom surface of the paddle, where delamination occurs.

Very High Pin Count Packages

Pin counts for microprocessors and logic gate arrays will continue to rise rapidly over the next several years. This will cause package dimensions to grow significantly despite the anticipated reductions in lead spacing. This trend will continue to put pressure on the processability of epoxy molding compounds. Larger packages with thin lead frames and very narrow spacings between the leads and wire bonds are much more susceptible to flow-induced stresses. Continued decreases in molding compound viscosity will be needed to package the 196-and 244-pin packages that will appear in the next few years, since current materials and processes may not be able to realize high production yields on these designs. New process technology, such as the multiplunger transfer molding and smaller conventional molds, may be required to provide the long cavity fill times needed to reduce the flow-induced stresses, if further viscosity reductions cannot be achieved. Pin and pad grid arrays (PGAs) could show substantial volume growth if the lower productivity of molded high-pin-count packages increases their costs close to that of the PGAs; the PGAs generally are easier to assemble onto printed wiring boards than fine-pitch chip carriers that are restricted to edge leads.

Heat Dissipation

Power dissipation requirements of IC devices have been steadily rising. Although the shift from ECL to CMOS technology has at present substantially reduced the problem, it is only a postponement. Power increases rapidly because power dissipation scales linearly with feature size at constant voltage, but on-chip circuit density increases as the square of the feature-size reduction ratio. Continued growth in device integration and miniaturization will push the power per chip to over 5 W in the near future, a level that cannot be easily dissipated in a conventional plastic package

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design. Thermal management will become much more important than it is at present, and the epoxy molding compound will have to play a major role in this management if the costs of plastic packages are to remain low. High-conductivity fillers are available, such as alumina, silicon nitride, silicon carbide, and magnesium oxide (see Appendix E). These alternative materials are all very abrasive. Developments in tool design may enable manufacturers to use these more abrasive materials, or surface treatments for the fillers could be developed to reduce their abrasiveness. The dielectric properties of these alternative fillers are not as good as silica (see Appendix E). In the absence of these technical developments, active thermal-management components will have to be added to the packaging. Devices such as molded-in heat spreaders or added-on cooling fins could significantly affect package manufacture and assembly, however, with attendant increases in cost.

Figure 5-1 recounts the improvements in thermoset molding compounds since the 1970s, and the expected needs over the next few years.

Plastic Alternatives to Epoxy Encapsulation

Plastic encapsulation of integrated circuit chips is, as noted above, dominated by novolac-based epoxies that are heavily filled with silica powder. These compounds are thermosetting (i.e., the resulting polymer is highly cross-linked) and the transfer molding cycle times for processing are long compared with injection-molding cycle times. On the other hand, transfer molds typically have hundreds of cavities producing hundreds of parts per cycle. The viscosity of a thermosetting epoxy evolves in a complicated manner, and thermoplastic compounds could well prove easier to process. However, procedures for processing epoxies are widely practiced, and the technology is entrenched. Reuse of scrap, as an economy, is another reason for considering thermoplastic encapsulants.

Liquid crystalline polymers form another class of material that is under consideration as a replacement for epoxy encapsulants. These materials are usually aromatic polyesters that contain naphthalene groups in the main chain. They form anisotropic liquids and solutions, and molded parts retain the anisotropic properties, an aspect that may be turned to advantage in a well-designed process because excellent mechanical properties can be achieved. This area is worthy of further research and engineering support to investigate the potential of liquid crystalline polymers in electronic packaging.

Polyphenylene sulfide is a thermoplastic material that has been available for several years as an alternative to epoxies. No widespread use has been reported, but development continues. This material can produce corrosive acid by-products and must be compounded carefully to avoid problems that could arise. As with epoxies, polyphenylene sulfide is filled with an inorganic powder, usually silica, to reduce the TCE.

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ORGANIC PRINTED CIRCUIT BOARD MATERIALS

Printed circuit substrates for electronic systems are usually organic, although circuits in the high-performance area tend to have more ceramic-based representation. It is obvious from Figure 1-8, discussed in Chapter 1, that chip technology in terms of density has advanced much faster than circuit board technology, conductor width and other features on ICs were 10 times smaller than those on circuit boards in 1965, and today they are about 100 times smaller. This linear gain is even more important in terms of circuit area. Progress in interconnection has not been as great. The large mismatch in dimensions that has now developed, less than 1 µm on the chip to more than 100 µm circuit boards, will over the next few years almost certainly lead to more extensive use of circuits of intermediate density.

The dominant material for circuit boards for more than two decades is a glass-fabric-reinforced epoxy resin labeled FR-4. This material is fire-retardant, stable, and amenable to high-volume processing. Inner layers in MLBs are available as B-stage material that can be processed to generate circuit traces and vias, then "layered up" and pressure-cured into the final, coordinated multilayer structure. This system has served the industry well and is likely to continue in widespread use for circuits that do not contain features smaller than about 100 µm (4 mils).

Advanced circuits appear to be moving to an improved version of FR-4 in which the bisphenol-A epoxy is replaced by a more highly crosslinked resin (novolac), a resin related to the molding compound employed for chip encapsulation. The glass reinforcement may also be modified or replaced to meet circuit demands. Thus, with only minor modification, it can be predicted that FR-4 will provide excellent circuits with features of about 20 µm in size. This development should provide MLBs of considerable sophistication for the remainder of this century. The availability of this improved FR-4 will blur the boundaries between very-high-performance circuit boards and multichip modules.

Other organic materials have coexisted with FR-4. FR-2 is a paper-reinforced phenolic resin, an inexpensive substrate material for single-and double-sided circuits. This substrate is popular in Japan. Molded printed circuits have been manufactured mainly from polyether sulfone and polyether imide. Several forms of flexible circuitry exist, including polyimide film, polyester film, and glass-mat-zeinforced polyester. Japanese consumer products employ polyimide film circuits. The glass-mat polyester also was used in telecommunications equipment. These materials (FR-2, flexible substrates, and some other examples) were (or are) niche products that are not part of the high-density substrate evolution history.

Beyond the improved FR-4, there are a number of alternative substrate and dielectric polymers available to meet specific needs. Polyimides provide excellent high-temperature performances, and a great deal of engineering has been conducted on this class of materials. Bismaleimide-triazene polymers (BT resins) exhibit good high-temperature properties and are compatible with epoxies. Polytetrafluoroethylene and certain highly crosslinked hydrocarbons offer a low dielectric constant as well as high-temperature performance. As

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the need arises for employing these more advanced materials, sources with the requisite expertise are available in the United States as well as in Japan. It remains to be seen which country will take the lead in producing materials and processes in this area.

PROCESSING TECHNOLOGY FOR CERAMIC PACKAGES, BOARDS, AND SUBSTRATES

The earliest packages for electronic circuitry were metal packages, and the interconnection between devices was generally done with wires. The earliest use of ceramics came in the form of bases for electron tubes with glass-sealed electrical feed-throughs. With the demand for miniaturization, some circuit designs began to use ceramic substrates. These provided a strong board upon which various wiring patterns could be placed. During the 1950s, the technology was developed for interconnecting various discrete devices using metal lines on these substrates. Furthermore, the technology for placing some resistors on these substrates in the form of thick films was also introduced.

One of the first applications of the ceramic package came with the need to house a simple quartz oscillator. This also was done in the late 1950s. While the substrate technology had led to miniaturization of resistors and capacitors, the individual transistor devices were still packaged in metal cans with the typical 3 lead wires protruding from the bottom of the can. This design was inconsistent with a low profile, so the model of the package used for the quartz oscillator acted as the driver for the first ceramic transistor package.

With the use of a ceramic substrate technology for interconnections, it quickly became obvious that, with increased complexity of circuitry, it was necessary to have a means of permitting one conductor path to cross another. A number of schemes were developed to do this, using complex insulated crossovers and small bridges, but the real technology for handling this problem came in two forms. These two forms, the ceramic multilayer tape process and the screen-printing process, constitute the basis for much of today's processing technology for ceramic packaging. Discussed in the following sections are some of the earliest technologies for making ceramic parts as well as the two major current processing technologies mentioned above.

Dry Pressing

The earliest process for making ceramic parts for electronic circuitry was that of dry pressing, and this included the substrates used for interconnection. In this technology, the powder is usually prepared by mixing the raw materials as a slurry in a ball mill. The material is dried and then calcined for phase formation and intial chemical reaction. The calcined mixture is again ball-milled to grind it into very fine particles, and this ground powder is then dried to prepare it for pressing. In the pressing operation, the powder is typically poured into a cavity of a metal die, and then the die plunger presses the powder into the desired shape. This

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technology can be cumbersome and relatively expensive, does not lend itself to having any buried conductor paths, and gives a part with a limited surface smoothness.

The Ceramic Tape Process

The ceramic tape-casting process (sometimes known as the doctor-blade process) was adapted from a process typically used in fabricating sheets of polymers or organics. In the ceramic adaptation, the powder is mixed with a liquid solvent containing various organic additives, which act as binders, dispersants, and plasticizers, to give a slurry with a viscosity roughly that of heavy cream. This slurry is poured into a reservoir and then spread into a thin sheet by having the slurry pass under the gate, known as the doctor blade, as either the reservoir is moved over a smooth sheet, or a smooth sheet is moved under the reservoir. After casting, the slurry is allowed to dry by volatilization of the solvent. The dried ceramic still contains sufficient organic binders so that the tape can be stripped from the carrier, and it exhibits sufficient flexibility and strength to be handled, cut, or punched. At this stage, the tape is referred to as a "green" tape, meaning an unsintered ceramic tape. The thickness is generally in the range of 0.5 to 1 mm.

This "green" tape can be used to fabricate substrates by punching the substrate shape from the rolled green tape, heating the piece to temperatures of about 200 to 300°C to pyrolyze or volatilize the organic binders, and finally heating to a sufficiently high temperature to sinter the ceramic particles into a dense, hard sheet. Because the particles are well dispersed in the original slurry and because the surface of the tape is very smooth, the sintered ceramic offers a high-quality, dense, pore-free, strong surface on which to place electronic interconnect devices.

By about 1960, the concept of making a multilayer substrate or ceramic package was introduced. In this technology, some or all of the metal interconnect lines are buried within the final ceramic. This is accomplished by printing the metal lines on each of several sheets of the unsintered ceramic prior to fabricating the package. The metal paste is formed by mixing the metal particles with organic binders and then patterning the metal lines by forcing the paste through a screen covered by an emulsion into which the appropriate pattern had been photolithographically etched. These layers of interconnect traces, or conduction paths, can be connected from one layer to the next using through-holes known as "vias." These vias consist of holes punched in the green tape into which the metal ink is forced in the screen-printing operation, thereby providing a conduction path from a point in one layer a to similar point in the layer above or below it. After all the layers are printed, they are then stacked together, with the appropriate registration, and laminated under slight heat and pressure into a solid unsintered block of ceramic and metal. This laminated piece can then be heated to remove the organics and finally to sinter it into a dense, hard ceramic. Furthermore, by appropriately shaping some of the layers, a cavity can be formed in the package into which ultimately the active device, such as a silicon chip, can be placed.

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Screen Printing

Screen printing mentioned above, provides an alternative mechanism for producing a three-dimensional interconnect technology on a ceramic base. This technology was developed in the late 1950s, at about the same time as the multilayer ceramic tape technology, and provides some of the same functions. In a typical application, a ceramic substrate is used onto which various layers are screen-printed. The first of these layers might be an insulating layer that is screen-printed, generally over a broad area. After printing, the layer is typically dried and fired at some temperature lower than that at which the original substrate was fired. If an insulating layer thicker than that typically obtained by a single screen-printing layer is necessary, a subsequent layer may also be screen-printed on, dried, and fired again. A metallization layer may then be screen-printed through a screen with an appropriate pattern. This, too, is dried and fired. The next insulating layer can then be applied, typically allowing openings for vias between the metallization in the first layer and the second layer. These various print, dry, and fire operations can continue to make a multilayer interconnect board. In contrast to the multilayer green tape technology, this method does not easily allow for a cavity into which an active device can be sealed and protected in an hermetic environment.

OTHER CERAMIC MATERIALS

This section describes some other ceramic packaging materials and makes projections about those materials that could play a prominent role in the future.

Glass and Porcelain

The earliest use of electronic ceramics was as insulators for carrying telegraph lines, telephone lines, and power distribution lines. Ceramics and glasses also were used in the fabrication of electron tubes, both as a tube housing in the case of glass, and, in some tubes, as the base material with glass-to-metal feed-throughs for the electrical conductors. The earliest attempts at making ceramic substrates and ceramic packages employed the materials available at the time, which were typically glasses and porcelains. Porcelain is generally made of naturally-occurring materials, such as clays and talcs. These substrates suffered from low strength, poor thermal conductivity, and poor surface finish. Early in the use of ceramics for substrates and packages, aluminum oxide (alumina) became the major material of choice, and it continues so today. Typical compositions are made up of about 92 to 94 percent aluminum oxide, the balance being materials such as magnesium oxide (magnesia) or silicon dioxide (silica).

The earliest metallization used was a molybdenum-manganese composition that had been known to fire onto aluminum oxide with a very adherent bond. This, too, was quickly replaced by either pure molybdenum or pure tungsten as the metallization of choice in co-fired aluminum oxide ceramic packages. These metallizations continue to be the choice today. Both of these materials

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can be made to sinter at about the same temperature as the aluminum oxide (about 1600°c) and provide reasonable electrical conductivity. However, both of these metal systems oxidize easily and require that the aluminum oxide be sintered in a hydrogen or hydrogen-water vapor atmosphere.

These alumina-based compositions provide a strong material with fairly high thermal conductivity. With tape processing, they can easily provide high-reliability hermetic packages for active semiconductor devices.

Low-Fire Materials

Low-firing ceramic materials are generally those that fire at temperatures below 1000°C, in contrast to the 1600°C necessary for firing aluminum oxide. Although a few single-phase ceramic materials do sinter at temperatures below 1000°C, this not the general case. Consequently, typical low-fire materials are made from glass-ceramic composites that fall into two categories. The first is known as glass-ceramics or devitrifying glasses. A glass is first formed by melting of the constituent materials, and then the cooled glass is crushed and ground into a fine powder, known as a frit. The frit is formed into the desired shape using any of the fabrication technologies discussed earlier. The article is sintered into a dense, glassy material, which is then annealed at some lower temperature where the glass crystallizes (devitrifies) into a two-phase crystalline-glass composite.

The second technology is known as glass-bonded ceramics. In this case, the desired crystalline phase is mixed as a powder with a frit of the desired glass phase. These again are fabricated into shapes by the various forming techniques already described and subsequently heated to sinter them into a dense material where the glass acts as a low-temperature sintering aid that bonds the ceramic particles together. The glass-bonded ceramic methodology is by far the most widely used. Aluminum oxide is again the typical crystalline material of choice. Its earliest use was in the screen-printed multilayer process described earlier. Here, the mixture of aluminum oxide and fritted-glass is screen-printed onto a substrate and fired at temperatures typically between 800 and 1000°C to make a dense ceramic layer.

As the complexity of thick-film interconnect substrates increased, the number of print-dry-fire operations exceeded 40. To simplify the process and yet use the firing equipment already in place, some producers have recently switched to a low-firing ceramic tape technology. Naturally, the tape generated to fill this void is again a glass-bonded ceramic composite. Here, the aluminum oxide powder and fritted-glass mixture is tape cast as described earlier. These tape-cast layers can also be screen-printed with the various interlayer metallization patterns and vias for three-dimensional interconnect applications.

This low-fire tape process offers at least two advantages. First, it permits use of the low-cost firing equipment available for thick-film printed circuitry. Second, it allows the use of metal conductors other than tungsten or molybdenum. Typical metals are silver, silver-palladium, or gold alloys, all of which have lower resistivity than molybdenum or tungsten and thus

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contribute to faster circuit-speed designs. A current challenge in this technology is the possible use of copper metal as a low-cost, low-resistivity interconnect material. Implementation of this ideal is hampered by the difficulty of preventing oxidation of the copper in typical firing atmospheres. The usual glass phases, in the glass-bonded ceramic compositions, are lead silicate-based glasses. If these compositions are fired in the reducing or neutral atmosphere conditions necessary for maintaining copper in the metallic state, the lead will partially or fully reduce, leaving a. lossy (low-resistivity) dielectric material. Thus, the full implementation of copper metallizations awaits a technology that can successfully implement glass-bonding agents that are not easily reduced in such atmospheres. Laboratory successes have been reported, and prototype materials are now available.

Low-Dielectric-Constant Materials

Aluminum oxide-based ceramics and most glass-bonded ceramic materials have dielectric constants in the range of seven to nine. The need for high-speed circuitry demands materials with still lower dielectric constants. Organic materials are available with dielectric constants as low as 2, but these materials are incompatible with the high-reliability hermetic ceramic packages. For inorganic materials, the lowest known dielectric constant is that of silica glass at 3.9. However, the thermal expansion characteristics and sintering characteristics of this material are incompatible with typical processing conditions. Consequently, glass-bonded ceramic compositions are being developed that strive to provide lower dielectric constants than those available in aluminum oxide-based materials. The typical crystalline phase in these materials is cordierite, a magnesium-alumino-silicate material. Also necessary are glass-bonding agents of relatively low dielectric constants, which typically avoid the use of lead oxide. Such materials, with dielectric constants in the range of 5 to 6, are now available in prototype form.

Inorganic materials with even lower dielectric constants probably await the implementation of a controlled-void technology. In this technology, the requirement is to process materials so that a large fraction of pores can be included, thus lowering the dielectric constant of the matrix phase. Incorporating hollow glass spheres or possibly applying sol gel glass technology are means of introducing controlled porosity. Closed pores are necessary to avoid any loss of hermeticity or possible inclusion of impurities that might lead to poor dielectric properties. If this technology could be successfully employed using silica glass, dielectric constants below 2 might be feasible. However, this technology will always be fraught with poor mechanical properties, since the pores are flaws that concentrate stresses and reduce the effective strength.

High-Thermal-Conductivity Materials

The design of integrated circuits and hybrid integrated circuits demands that the heat generated be dissipated through the package. Organic packaging materials or plastic packages typically have quite poor thermal dissipation

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properties, and for this singular reason ceramic packages are often used. Of the traditional ceramic packaging materials, aluminum oxide is a reasonably good thermal conductor. Of lesser conductivity are the glass-bonded ceramics, a deficiency that limits the use of some of the low-k materials.

Traditionally, when very high thermal conductivity has been needed, the material of choice has been beryllium oxide. This material has a thermal conductivity roughly equivalent to that of aluminum metal and about 10 times higher than aluminum oxide. In many respects, berylluium oxide is a convenient replacement for aluminum oxide; the processing conditions, metallization systems, and sintering temperatures are similar. However, beryllium oxide suffers from a major disadvantage—its toxicity. The care needed in processing even the powder has driven the price to about $50 per pound. Similarly, the caution exercised in processing this powder into ceramic packages adds additional cost to these packages, thereby leading to very expensive devices. Further limiting its use are the concerns of users in handling these packages.

Two new materials with high thermal conductivity have become available within the past five years: silicon carbide and aluminum nitride. Silicon carbide was first developed in a high-thermal-conductivity form by Hitachi. This was achieved by adding small amounts of beryllium oxide (less than 1 weight percent) to pure silicon carbide and sintering by hot pressing at very high temperatures, generally in excess of 1900°C. In contrast to less pure forms of silicon carbide, which are electrically conductive, this high-purity, beryllium oxide-doped form of silicon carbide is a good electrical insulator and has a thermal conductivity approximately equal to that of beryllium oxide. The shortcomings of this material are the high processing temperatures, the small beryllium oxide content which leads to some real or imagined health hazards, a high dielectric constant (on the order of 20 or more), and the lack of an applicable technology for making multilayer metallized packages. Thus, use of this material has been limited to some special substrate applications, particularly for laser mounts.

The second material, aluminum nitride, now offers greater promise than silicon carbide. If processed properly, this material has been shown to have a thermal conductivity even higher than that of beryllium oxide. Furthermore, the dielectric constant of aluminum nitride is approximately that of aluminum oxide. As with many covalently bonded ceramic materials, aluminum nitride also has the disadvantage of being very difficult to sinter, requiring temperatures in excess of 1900°C. Processing must also be done in the absence of oxygen because most of the oxides formed from these tend to degrade sharply the thermal conductivity of this material. However, some oxide dopants have been shown to be advantageous in aiding sintering without severe degradation of thermal conductivity; examples of dopant oxides are magnesium oxide or yttrium oxide. Another potential shortcoming of aluminum nitride is the difficulty in bonding it to metal. (Aluminum nitride has been traditionally used as a crucible material for melting metals because of its tendency to not bond to metals.) However, for multilayer ceramic substrate applications, bonding to metals is crucial. Nevertheless, the current state of the technology is better than that for silicon carbide since some laboratories have demonstrated processes for satisfactorily bonding metals to aluminum

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nitride. Generally, additives to the metals or additives to the ceramic are necessary to initiate this adhesion.

The material of highest known thermal conductivity is diamond, a material used in special cases as substrates and being considered for future more extensive use as substrates. Sumitomo Electric in Japan markets single crystalline diamond substrates for use in very demanding applications. These single crystalline substrates are, of course, very expensive, and means of potentially reducing the cost of such substrates are being explored. One possible fabrication technology is to sinter lower-cost diamond powders into dense polycrystalline diamond substrates; however, the state of this technology is still uncertain. The incorporation of electrical defects in the diamond structure, or having graphitic layers or other impurities present, has led to low electrical resistivity, which makes these sintered substrates unsuitable for electronic applications. A promising means of fabricating diamond for electronic applications lies in some of the CVD methods that have been explored in the mid-to late 1980s. This technology is still limited to relatively thin layers, generally less than 20 µm thick, and they also show irreproducible quality in their electrical insulating characteristics. Figure 5-2 (also Appendix E), cited earlier, reviews typical thermal conductivity and dielectric constant relationships of some important substrate materials.

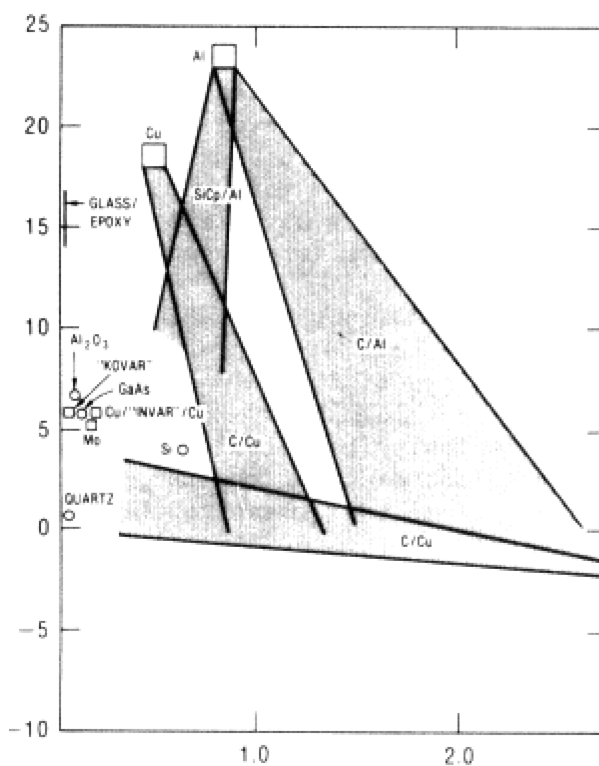

Figure 5-2.
Coefficient of thermal expansion and thermal conductivity ranges available with composite materials.

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POLYIMIDES IN HIGH-DENSITY PACKAGING

Polyimides have a number of characteristics that make them important for high-density electronic packaging. Some of these features are discussed in the following, and some insight on their more extensive use in electronics is provided.

Trends in High-Density Packaging

Until recently, computer systems with high-density packaging have used one of three approaches to chip interconnection: (a) conventional epoxy boards and multichip ceramic modules single chip carriers, (b) conventional epoxy boards and multichip ceramic modules with single chip carriers, or (c) conventional epoxy boards with chips directly attached to multichip ceramic modules. None of these systems had the capability of wiring all chips together with a single packaging level. The increasing size of central processing units (i.e., the number of devices in a CUP) and the importance of eliminating interconnection delays have led to exploration of approaches that have the potential for eliminating significant fractions of interchip signal delays.

The published literature contains numerous descriptions of efforts to reduce the gap between wiring density (and concomitant signal delay) on the chip and in the package. Two of these are (a) the silicon chip carrier, in which the interconnection between logic chips is accomplished by multilevel thin-film polyimide insulated copper or aluminum wiring on a silicon wafer, and (b) the hybrid ceramic module with levels of polyimide board, which is analogous to the traditional epoxy board, but has a lower thermal expansion coefficient and higher thermal stability for attachment of chips with a TAB-like carrier. However, only recently have these approaches to high-density packaging appeared in announced computer products.

The distinction between CMOS, bipolar, BiCMOS, and GaAs logic technologies does influence the optimum approach to high-density, high-performance packaging. CMOS and BiCMOS chips tend to have a greater number of logic devices per chip compared to bipolar and GaAs. This leads both to greater interconnection complexity for bipolar and GaAs logic and to an increased emphasis on the performance of the interconnection (packaging) technologies for these chip families. Despite this distinction, the technical literature abounds with reports of thin-film polymer-copper or aluminum interconnection for all the chip technologies. Consequently, it is possible to conclude that efficient chip interconnection has become important to all chip logic technologies.

Polyimide Processing

The processes used to fabricate polyimide-based packaging technologies vary widely. In the extreme of "chip-like" processing, conventional chip processes of photolithography, RIE processing, and spin coating are employed. In another extreme, conventional board processes are employed where the

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prepreg is fabricated, electroplating is used to form metal lines, and lamination, drilling, and electroplating are used to interconnect the levels. Combinations of these basic approaches make use of mixes of both extremes. One example is the use of "chip-like" processing but using "metallization" with electroplating of copper. No distinct trends in use of these processes are observable today, probably because the use of polyimides in high-density packaging has yet to reach maturity.

Polyimides and Properties for High-Density Interconnection

The polyimides currently used in the foregoing technologies are numerous, but all have a common characteristic. They are used when epoxies lack adequate properties for the application. This generally occurs when improved thermal properties (e.g., high direct solder-attach temperature) are required, improved mechanical properties are needed (polyimides generally are much less brittle and have greater tensile strength), or a lower dielectric constant is required. The thermal properties of polyimides are an improvement over epoxies in two ways: First, the thermal stability is considerably greater, and second, the glass transition temperature, or the temperature at which the polymer softens, is most often greater than 280°C. The dielectric constant of polyimides is usually between 3.4 and 2.9, as compared to epoxies, which are greater than 4.0.

Today, many polyimides are available for high-density packaging applications. The properties of these materials range widely in a number of categories: glass transition temperatures between 250 and 400°C are available; mechanical properties ranging from brittle to very tough may be achieved; thermal stability at 250 to 400°C is possible; dielectric constants from 2.65 to 3.4 are typical; adhesion to the ceramic, polyimide, SiO_zn, or metal interfaces varies widely, but generally requires an adhesion-promotion agent; the stress in a polyimide film varies widely among commercially-available materials (amorphous polyimides generally have a film stress of about 5 to 7 Ksi, whereas ordered polyimides may have film stress as low as 1 Ksi); and planarization also varies widely between polyimides but is generally dependent on the percent of solids in the formulation.

The thermally-induced stress in polyimide packaging structures is usually dominated by the high TCE of these materials. Recently, a breakthrough has occurred with the availability of low-TCE polyimides. These materials may have linear expansion coefficients of 6×10^{-6} /°C compared to 35×10^{-6}/°C for conventional polyimides. In addition, these materials may be tailored for TCE matching. This new family of materials will likely be used widely in high-performance thin-film interconnections. While these materials offer a significant advance in the reduction of stress in interconnection structures, further improvements in self-adhesion of these materials are desirable.

Although the packaging process engineer has this wide variety of properties to choose from, it is generally true that the best properties in each category are not available in a single material. Consequently, selection

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of a polyimide for a packaging application may be a complex process in which compromises must be made.

Photosensitive Polyimides

The processing of polyimide films for high-density packaging is often complicated by the necessary patterning of the films. This patterning is generally accomplished for board-like structures by drilling, by oxygen reactive ion etching (RIE) for fine-line features, or by etching with a strong base or hydrazine. Each of the last two methods requires separate masking steps that add to the complexity of processing. Considerable simplification of serial-process fabrication of polyimide-based packaging technologies can be realized with photosensitive polyimides. These materials have been commercially available for some years from a number of chemical companies in the United States, Europe, and Japan. Japanese chemical companies, in particular, have been most aggressive in making photosensitive polyimides commercially available. Again, as in the case of conventional polyimides, choosing a photosensitive polyimide for a packaging application is a complex process in which the optimum combination of properties is not available and compromises must be made. One example is the fact that most photosensitive polyimides shrink about 50 percent in processing from the lithographic imaging to final cure. This shrinkage leads to limitations in feature size resolution, which currently is in the range of 25 µm for thicknesses greater than the 8 µm thickness used in packaging technologies.

General Availability of Technical Information on Polyimides

Packaging engineers who seek to use polyimide materials are often confronted with the need for detailed information on their chemical, physical, and process characteristics. Chemical companies have traditionally supplied customers only sketchy information on these materials. University research on the chemistry, physics, and process characteristics has not been a popular endeavor, as this has been considered an "old" field of research. Large companies that intend to use polyimides in new technologies have conducted their own R&D but have not published this information widely. Consequently, detailed scientific understanding of polyimides, which forms the basis for a well-engineered packaging technology, has not been available to the whole industry. The technical vitality of the U.S. high-density packaging industry would be well seized if both chemical companies and universities placed greater emphasis on providing this information.

Benzocyclobutane (BCB) is a polymer recently introduced that has great promise as an interlayer dielectric and other applications. The dielectric constant is about 2.7 and the loss is very low, as expected for hydrocarbons. Polymerization does not release volatiles and high glass transition temperatures, greater than 350° C, are achieved. This material exhibits very low moisture absorption and is chemically extremely stable. Although there is much less industrial experience with BCBs, some commercial applications are already appearing and BCBs could become the polymer dielectric of choice in a

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wide range of circuits. A photoimageable BCB has not appeared yet, but it can be plasma etched through a lithographic mask.

Polymers in Future High-Density Interconnection Technologies

The trend toward thin-film interconnections in high-density packaging appears to be set and will continue for the foreseeable future. With the evolution to higher-performance requirements, incremental improvements in the properties of polyimides or polymers used as insulators will be sought by the industry. Required improvements will be needed by the industry, and will probably occur in two categories: (a) photosensitive polyimides with greater lithographic image resolution and (b) polymer insulators with lower dielectric constants. It would be useful if easily processible materials with dielectric constants as low as 2 were available. These requirements present a significant challenge to the chemical industry because they are not currently available.

TAPE AUTOMATED BONDING

Tape automated bonding (TAB) uses a premanufacutured lead frame as a substitute for wire bonding. The lead frame presents a uniform array of inner leads to be attached to the bond pads on the surface of the die. The die and leads are then excised from the lead frame, and the outer leads are bonded to a package or a multichip substrate. The TAB lead frames are manufactured in a continuous process and are available in reel, strip, or slide format. All the leads can be bonded to the die simultaneously. TAB is often preferred over wire bonding for multichip modules because it can accommodate more leads per chip (more than 300) and higher clock frequencies.

There is a cost overhead for the tape design and tooling for each chip size, and, therefore, TAB is best suited to high-volume applications. TAB is routinely used to fabricate liquid crystal television displays, which require many leads for relatively small die sizes. One brand of hand-held televisions contains TAB with 80 µm lead pitch (about 300 leads per linear inch). The first U.S. applications for high-lead-count TAB will be in computer work stations. This application requires packaging of high-lead-count devices (up to 500 per chip), with operation clock rates of 50 to 100 MHz, and the ability to be manufactured in volumes of tens of thousands. Once these requirements are met, TAB use will then spread to many other applications. Wire bonding will continue to be used for single-chip packages with up to 200 leads and also for prototyping of multichip modules.

From a materials point of view, TAB consists of copper conducting fingers carried on a polyimide film. The joint between the TAB tape and the chip bonding pad requires a metal "bump," either placed on the chip or on the tape. Because TAB tapes are very thin, the mechanical modulus of the polyimide is an important factor in simultaneously positioning all of the lead fingers in register with the bonding pads. Thermal expansion is also important.

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The extendability of TAB technology from the present 200 I/Os per chip to the expected 600 I/O chips of the mid-1990s will require much finer-pitch inner-lead peripheral connections or area array chip-to-TAB connections. Both approaches are difficult, if not impossible, with present TAB substrate materials. TAB carriers with lower TCE and higher modulus are required. The first of these improved substrates is available in the form of a lower-TCE polyimide, but further substrate materials improvements will be required to reach the mid-1990s requirements.

TAB has been a promising technology for many years, but it is still not widely used in the semiconductor electronics industry. At this time, nearly every major semiconductor manufacturer is either using or evaluating the technology. The committee was not in complete agreement regarding the degree of market penetration and the time scale for penetration.

DIAMOND

Diamond is among the most interesting of all materials (DeVries, 1987). In the familiar single-crystal form, it is far too expensive to be employed in ordinary packaging. The physical properties are remarkably attractive, however, and efforts to grow diamond, or diamond-like, films have persisted through the years. Within the past decade, films have been successfully produced by chemical-vapor-deposition (CVD), and research activity in this technology has accelerated. Ion beam epitaxy has also been employed to produce films with good properties that can be deposited on various substrates. Although growth rates are small and conditions involve moderately high temperatures for the substrate, good progress is being made, and it is reasonable to expect that diamond-film passivation layers will become possible within a few years.

Among good dielectrics, diamond has uniquely high thermal conductivity, and CVD films have approached values typical of bulk crystalline diamond. The value of 20 W/cm°K at room temperature is an order of magnitude better than BeO and four orders of magnitude better than epoxy. Hardness, relatively low dielectric constant, and good optical properties also favor diamond films. At liquid nitrogen temperature, thermal conductivity is above 100 W/cm°K.

Applications that would benefit from the singular properties of diamond films include chip passivation, substrate coatings, and interlayer dielectric layers. The design possibilities are sufficiently removed from present materials so that new strategies of thermal management could arise based on these new diamond films.

SUPERCONDUCTORS

It has been recognized for many years that superconducting materials offer great promise for high-speed electronics (Hunt, 1989). A number of organizations have worked on the development of Josephson junction technology, and at least one company, Hypres, has successfully marketed commercial devices. There are important differences between silicon electronics and

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Josephson junction electronics (e.g., voltage level), and it has been difficult to overcome the momentum of the more established technology. Not the least of the Josephson burden is the requirement for liquid helium cooling. With the discovery of high-temperature superconductors (HTSCs), the comparisons have been reopened, because liquid nitrogen cooling is easier and more economical than cooling with helium.

The problem of packaging and interconnection of Josephson circuits is beyond the scope of this report. There is, however, the possibility of employing superconducting striplines as interconnects in printed circuit and multichip module structures. As lateral dimensions of circuit lines shrink (see Figure 2-8), the line resistance can become a problem; for example, a 2 μm x 8 μm copper line has a resistance of 10 ohms per cm at room temperature but only about 2 ohms per cm at liquid nitrogen temperature. As the line resistance becomes an appreciable fraction of the line impedance (50 to 70 ohms), the speed of signal transmission decreases, a feature that favors low-temperature operations.

The new HTSCs are ceramic materials that will require considerable development before their promise can be realized in practical circuits. These materials must be processed at high temperatures and must be protected from atmospheric moisture. In addition, electrical contacts with them to other metals are not easily made, and the properties at high frequencies are less than ideal. These are early days in the HTSC field, but, with a massive level of research under way world-wide, the problems will be overcome. Interconnects for advanced electronics are under consideration as an early application. Unlike superconductor wire applications, much of the ductility and flexibility requirements in interconnections are less demanding.

There can be little doubt that HTSCs will become a part of interconnect structures, although applications are probably several years away. Research on all aspects, scientific and technological, should be strongly encouraged, bearing in mind that materials interactions and process compatibility will be particularly important.

COMPOSITES

Composite materials represent the extent to which materials are being engineered to achieve design intent; for example, strong fibers in polymer matrices have had an enormous impact on the construction of aircraft and other aerospace structures. In electronics, composites have long been used as printed wiring substrates (e.g., FR-4) and silica-filled encapsulation epoxies. Today, new composites are beginning to appear that will broaden the range of materials combinations found in electronic structures.

The more traditional fiberglass substrates (woven E-glass mats embedded in a bisphenol-A epoxy matrix) are being replaced by materials that give better dimensional control, lower dielectric constant, and greater operating temperature range. Polyimide fibers can be designed with small and even negative coefficients of linear expansion, and these are beginning to find their way into electronic substrate composites. Expanded teflon fibers may be

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introduced into epoxy matrices to achieve lower dielectric constant. More highly functionalized epoxy matrices offer better dimensional control and higher glass-transition temperatures. Polyimide matrices also offer high-temperature performance. This latter area is one of intense activity, and new systems can be expected to increasingly penetrate the high-density PWB market. Research in this area will benefit from closer coupling with systems designers.

Filled-plastic encapsulants today employ silica almost exclusively, but the opportunity exists to enhance thermal conductivity by introducing alternative fillers. The thermal conductivity of the encapsulation compounds can be improved by factors of two to six by introducing compounds such as alumina, magnesia, and boron nitride at the expense of larger (less than 50 percent) coefficients of thermal expansion (CTE). Research in this area could yield important results (see the first section of this chapter).

Ceramic-matrix and metal-matrix composites also are available, and the field is developing. Opportunities for matching CTEs of composites and semiconductors while improving thermal conductivity are illustrated in Figure 5-2 cited earlier. Their use in printed wiring and multichip modules is suggested, and some applications already exist; these materials also have been used for housings for microwave and power units. This is an area in which significant work is being done, both in the United States and overseas, but the work is not very visible. Improved composite materials for packaging and interconnection should be a significant focus of future work because the opportunity to design materials with desired substrate properties is worthy of further attention in the context of high-density electronics.

The high thermal conductivity of carbon fibers suggests their use in composite materials for heat sinks. Carbon-fiber-reinforced copper, for example, can be designed for good thermal conductivity coupled with weight reduction. Also, carbon-fiber-reinforced epoxies can be made with high thermal conductivity, dimensional control, and ease of fabrication. In these, continuous fibers are preferred. Here again, composites offer the flexibility to engineer materials with desired properties.

Multichip modules, as discussed in Chapter 3, offer high-density interconnections on a planar surface. These modules may have hundreds of I/Os, usually arranged around the periphery of the module. They may be attached to a mother board through pin grid or pad grid array terminals, or they may be combined in a stacking fashion to form supermodules with short interconnect paths. The z-dimensional connections can be made by special composite materials that electrically conduct in the z-direction, yet are highly resistive in the x-and y-directions. The conductors are metallic and are oriented in a matrix that may be ceramic or polymeric. Photodefined holes are etched in the ceramic substrate, then filled with wadded-up wire ("fuzz-button"). This arrangement can interconnect facing surface pads reliably without solder; i.e., pressure alone suffices (see Appendix D).

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Polymer systems can be made to conduct by using magnetic alignment of nickel balls, oriented wires, or balls of metal whose diameter is greater than the layer thickness. These composites may be held in place mechanically or by adhesives. Many contacts can be made in a single operation, thus facilitating assembly. These composite anisotropic conductors are still in an introductory phase and have not been demonstrated in high-reliability, high-density electronic systems. They have been employed in small television displays, where a large number of contacts (1800) is required and disassembly is important. These techniques offer ease of assembly and other advantages, but much testing remains to demonstrate the reliability needed in high-density electronic systems.

MATERIALS FOR VERY-HIGH-FREQUENCY DIGITAL SYSTEMS

Very-high-frequency digital electronic systems are extremely demanding in terms of materials properties. Generally, inorganics are used as substrates for the first level of interconnects, whereas organics serve as interlayer dielectrics. High-frequency structures require low-dielectric-constant values, whereas the power plane will need very high ϵ' to store charge very close to the chips it is powering.

Inorganic dielectrics generally have high dielectric constants, i.e., $\epsilon' \geq 3.8$. Thus, they are not likely materials of choice for interlayer dielectrics. Ceramic layers can be prepared in porous forms that can achieve $\epsilon' < 2$, but it remains to be demonstrated that these materials have sufficient mechanical durability and can be prepared with a smooth surface. Process compatibility for building multilayer structures must be established and long-term stability characterized. Even so, this is an interesting class of material that offers radiation resistance and low high-frequency loss.

Ferroelectric ceramics can offer high-dielectric-constant ($\epsilon' > 10^3$) capability for essential charge storage near active devices. For high-frequency applications, it will be necessary to demonstrate that the material can respond rapidly enough to deliver the charge in the time scale required. In addition, the dielectric constant of ferroelectrics often decreases dramatically as frequency is increased through the GHz range.

Polyimides have been favored as interlayer dielectrics for MCMs, and a great deal of development work has been focused on such multilayer structures. As circuit speed is pushed higher, lower-dielectric-constant materials will be required, and polyimides will be displaced. Polyimides absorb water, which leads to ϵ' variability and high-frequency losses (ϵ''). Hydrocarbon and fluorocarbon polymers are most promising for $\epsilon' < 3$ and low dielectric loss ($\epsilon'' < 10^{-3}$). Considerable development effort will be required to provide low-dielectric-constant layers that are process-compatible, exhibit good adhesion, and satisfy all the other design requirements.

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MATERIALS FOR CONNECTOR APPLICATIONS

Connectors are necessary in high-density electronic systems to facilitate assembly, repair, and maintenance. Unfortunately, connector design historically has been handled as an afterthought to system design. Although this approach has created serious reliability problems in the past, it has not necessitated a redesign of entire systems. As system performance increases, as measured by signal rise time, electrical discontinuities that are transparent at large rise times cause serious signal reflections. Physical design of connectors that provide thousands of connections and are capable of handling signals with less than 100 psec rise times are a significant technical challenge.

From a materials standpoint, advanced connectors will be driven to the most reliable metallurgy, e.g., gold mated to gold on palladium. The choice of insulator is made on the basis of mechanical strength. Because of the very small cross sections of the molded parts, thermoset materials are favored—e.g., polyethyleneterephthalate, polybutyleneterephthalate, and polyphenylene sulfide. For higher-temperature applications, polyethersulfone and polyetherimide can be employed. Physical design of high-density connectors is becoming a major challenge, with materials properties and processing occupying an important position in meeting the performance needs.

THE THERMAL CONDUCTION MODULE

IBM's thermal conduction module (TCM) has been at the leading edge of integrated circuit chip packaging for some time. This very significant accomplishment has taken a long time to develop since its beginning in 1964. This concept, and early work, started in a program with the appropriate name, "next-generation technology" (NGT). A technical description of the TCM was published by Blodgett (1983). The following discussion briefly describes the history of how the TCM evolved.

The NGT program was started in January 1964, and in April 1964, IBM announced the System 360 with its solid logic technology (SLT). The SLT program made use of small silicon chips containing single transistors that were attached to 1/2-by 1/2-in. ceramic substrates containing 16 pins that were soldered into printed-circuit daughter cards. Small copper spheres, plus solder, were used to connect the inverted transistor chips to the thick-film pattern on the ceramic substrate. Resistors were fabricated on the chip by a silk-screen process, as was the wiring on the chip. The resistors were later trimmed to value by a "sand-blasting" operation.

Within IBM, in 1964, there was a small, but articulate, faction that argued that SLT was threatened by integrated circuits. This issue of SLT versus integrated circuits quickly became polarized and highly emotional. The NGT program, from its inception had, decided that integrated circuits and monolithic memories were the correct technical thrust for the future, and an effort was made to stay out of the highly emotional issue, but with little success. How to package integrated circuits was not resolved within the NGT

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program until about August of 1964. At that time, the NGT program defined a four-phase approach to solve the packaging problem of integrated circuits.

For phase 1, it was proposed to put integrated circuit chips on the SLT substrate, which would provide the benefits of integrated circuits without having to develop a whole new package. In addition, the SLT module was consistent with the level of integration on chips at that time. Phase 1 later became known as the monolythic systems technology (MST), which was the technology used in IBM's System 370.

NGT's phase 2 proposed using a 1 by 1 in. ceramic substrate, which, with its larger area and more I/O pins, could support chips with higher levels of integration. Phases 1 and 2 were based on established packaging technologies, while still concentrating on learning how to produce integrated circuit chips to go on those packages. Phases 3 and 4, being further away in time, proposed a significant departure from the SLT module.

The NGT program recognized that the level of integration would constantly increase with time, and thus a viable packaging strategy must take this into account. It also was recognized that the exponent in Rent's rule was less than 1. This meant that the ratio of I/O pins to circuits would decrease with increasing levels of integration on the chip, a reasoning that held for the next level of packaging as well. Contacts between levels of packaging take up space, are costly, limit performance for high-performance systems, and can create reliability problems. By going to higher levels of integration at all levels of packaging, one or more levels might be eliminated.

During the period from 1964 to 1966, the NGT program had a joint effort with Texas Instruments (TI) that was structured to explore the future problems of large-scale integration (LSI). In this joint program, TI supplied IBM with wafer-scale integration consisting of 9 wafers with 120 circuits per wafer mounted in 9 modules. A small system, using these modules, was working by early 1966. TI used pattern interconnection in fabricating the wafers. At that time, fixed pattern interconnection could not provide LSI capability.

The NGT program selected multilayer ceramics (MLC) as the technology with which to construct the modules for phases 3 and 4. Phase 3 was targeted at future cost-performance types of systems, whereas phase 4 was focused on future high-performance systems. The plan in phase 4 was to use high-performance emitter coupled logic (ECL) on integrated circuit chips. High-performance circuits consume high power per circuit. However, since one NGT objective was to place as many circuits on the chip as the manufacturing process would allow at a given time, a way had to be found to dissipate all the power produced by the many chips on a module. It was felt that fluorocarbons could be used in the module to carry heat from the chip to a heat exchanger on the module.

Use of an MCM with signal conductors embedded in ceramic that had a dielectric constant of approximately 9 caused a debate within IBM. The debate ensued over the advantages of transmitting a signal from one chip to another

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through a relatively low-dielectric-constant material, such as FR-4 epoxy, versus a high-dielectric-constant material, such as alumina ceramic. The velocity of propagation is higher in FR-4 than in ceramic, but the distance can be much shorter in ceramic. Only relatively recently has a consensus emerged that supports the NGT researchers.

By early 1966, IBM decided that a replacement was needed for System 360. To do this, a monolythic systems technology a (MST) program was initiated based on the NGT phase 1 proposal and staffed by NGT people who had been previously asked to concentrate on the highly aggressive phase 4 program. At this time, the NGT program had rudimentary multichip, multilayer ceramic module hardware working. Domestic work was stopped at IBM. Fortunately, the NGT program had generated interest in multilayer ceramics in IBM's Boeblingen laboratory, and researchers there continued and improved on the multilayer ceramics work that had been started in IBM's domestic laboratories. The Boeblingen effort became the basis for IBM's present TCM when this technology was reintroduced to the United States in the mid-1970s.

The purpose of recounting the early history of multilayer ceramics at IBM is to emphasize the point that developing new structures employing new materials is a long and difficult process. When such a process is successful, the payoff can be quite dramatic, as has been demonstrated at IBM.

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Chapter 6

Organizational, Funding, and Policy Issues

The foregoing chapters presented technical aspects of the subject of materials and high-density electronic packaging. The topic was presented from the points of view of systems considerations, existing approaches, and the materials themselves. In this chapter, the business, organizational, policy, and political aspects of the subject are examined. The committee recognizes that some of the discussions below go beyond technical matters, which are the focus of the report. Nevertheless, these discussions are pertinent to giving readers an understanding of the overall industry situation and provide a basis for some of the recommendations developed by the committee. This inevitably leads to comparisons of the U.S. versus the Japanese approach, involving issues of competitiveness, research funding, vertical integration, and the range of business vision in the United States. The 1980s could well be labeled the decade of "electronics consortia," and this mode of organization must also be considered.

One must acknowledge that the loss of the U.S. technological edge in electronics can be related to the U.S. electronic industry's concentration on IC chip design and overall systems aspects. By contrast, the Japanese industry moved into the volume commercial marketplace, with particular focus on the packaging area, that gave them a major advantage in the technological advancement of their industry. The U.S. industry placed emphasis on the high-end, low-volume technologies, hoping for a "trickledown" effect. This was contrary to the Japanese approach of getting into the low-end, high-volume products, that were then upgraded to the high-end technologies where their new dominance is appearing today. In addition, large Japanese electronics companies are fully integrated from raw materials through the consumer product, giving them full control of all fabrication steps. U.S. companies have found it difficult to assimilate this type of integration into their manufacturing schemes and philosophy.

INTEGRATION

The U.S. electronics industry is fragmented laterally. Manufacturers do not share component, system, and process design information beyond those necessary to establish needed industry standards. This leads to nationally expensive redundance, at least some of which could be eliminated without exposing the public to the negative aspects that can result from monopoly control. U.S. corporations are, however, reluctant to engage in activities that could bring antitrust enforcement actions. There is some progress in cooperation, but caution is evident.

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The U.S. electronics business is also fragmented vertically, and it is the lower levels of the supply and manufacturing chain that are most closely involved with the materials aspects of packaging and interconnection. The following sequence illustrates the problem for organic materials employed in chip encapsulation. A compounder (i.e., an independent company) purchases epoxy resins, accelerators, curing agents, silica fillers, antimony oxide (a flame retardant), and other components from various chemical suppliers, quite possibly a different supplier for each compound. The chemicals are supplied according to specifications, but they are normally not "pure" by electronics standards. Epoxy resins are usually somewhat ambiguous in chemical structure, and the silica powder varies in particle size distribution and possibly in surface characteristics. The compounder normally is not sophisticated in the characterization of incoming supplies. The materials are mixed (compounded) by a proprietary process that is controlled to some degree, but not precisely.

Solid preforms, which are about 2 in. in diameter and 11/2 in. thick, are made and sent to the encapsulation facility, a different company, commonly in the Far East. The preform is preheated, placed in a plunger cylinder, heated further, and forced through runners of a transfer mold and into cavities containing individual chips (perhaps as many of 300 at a shot). In this process, the epoxy precursors react to form a highly crosslinked polymer, release heat, and undergo first a decrease in viscosity, then an increase to form a rigid solid case surrounding the chip.

This encapsulated device is tested (under considerable stress) and shipped to an assembly factory, where it is put on a circuit board and soldered in place. (It should be noted that the circuit board, organic or ceramic, also has arrived at the assembly factory by a similarly complex chain of suppliers and processors.) Following more testing, the board is plugged into the system by the final system manufacturer.

Clearly, the system works remarkably well, and the existence of complex electronic apparatus attests to the dedication and expertise of the various contributors along the way. There is, however, very little information flow along the chain because the materials and processes employed are secret and proprietary at each fabrication stage. This places great importance on the consistency for each process. When problems arise, it can be difficult to identify the source. A molder can be expected to find fault with the epoxy compound, even when it is known that the molding process is not quite right. And so it goes at each stage. As packaging and interconnection become more and more demanding (and fine lines, large lead counts, and higher power dissipation will test the technology), process maintenance, quality assurance, and production schedules will be increasingly difficult to guarantee.

The chain of transfer from one company to another creates even greater challenges for research and development. The U.S. companies involved are traditionally secret-process-based, and this mentality runs deep. An organization does not transmit technical details to its customers, and, although there are signs of movement to a more cooperative posture, reform requires changes in this ingrained behavior.

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The alternative is the entry of a vertically integrated U.S. company that could carry through several or all of the steps in material production, compounding, and molding. No serious U.S. effort is known in this direction for chip encapsulation, printed circuit board manufacture, or ceramic detail production.

SYSTEMS VERSUS MATERIALS APPROACHES

A central technical issue is the balance of package and interconnect materials considerations, building-block approaches, system-architectural approaches, and system-organization approaches. Past packaging approaches have not been materials-focused but have stressed configuration of known materials. Past system-performance approaches have focused on parallelism and enhanced building blocks having tighter physical configurations. These approaches might have come to a point of diminishing returns, but progress continues to be made, and rate of improvement does not appear to be tapering off. Even so, it is clear that materials contributions to the enhancement of system capability will be centrally important in the next decade and should be addressed.

The political issues being addressed in this report are probably the more important ones because these issues appear to limit progress in resolving todya's technical problems. A few of these political issues are scrutinized here.

First, the relationship between the materials supplier community and the user community is universally unsatisfactory. The suppliers are perceived as secretive, concerned with establishing a proprietary position for their financial advantage, unwilling to invest for a long-term goal, and unwilling to speculate beyond their current status. The users, in turn, are perceived as indifferent to physical limitations, unwilling to share their evaluation results with their suppliers, playing off suppliers against each other, and always blaming the materials when things do not work out as they would like. The problem is that the suppliers and the users are not of a common technical culture and are separated by marketing and purchasing communities that are not concerned with technical progress. There is need for a technical community in which the users and suppliers can engage in technical interchange without being cornered by the interplay of financial, accounting, and business activities. This is difficult to accomplish in this corporate-based culture.

A second political issue that will have a major impact on the packaging and interconnect approach is that of funding and control. Funding is one of the levers with which it is possible to move the suppliers and the users of packaging and interconnect materials to work with each other. It can be noted that government funding seems to perform this unifying role especially well, since all the participants involved sense that they are benefiting from funding that does not come from their own pockets. Government funding seems to flow naturally from the Department of Defense, but for packaging, the most serious problem appears to be the divergence of military packaging from the

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packaging approaches of mainstream developers of high-performance systems. It is easy to cite some specifics:

- Military systems insist on the use of hermetic packages, but most high-performance systems in the commercial world use plastic-packaged (or unpackaged) parts.
- Military system technology tends to lag a generation behind that used in the commercial world because military systems development and deployment have at least a 10-year time frame, whereas commercial systems must get to market 3 years after the start of development, or they will have missed the market and another supplier will have gotten there first.
- Military systems are tied to conservative approaches, such as hermeticity, no organics inside the package, and the value of old technologies in the face of rapid progress in the commercial world.

Nevertheless, the military services have funding, and their willingness to fund (if not to use) advanced technology makes them a partner to be sought.

The most serious issue is the choice of vehicle for the materials development activities. To develop materials in isolation from a system application is a futile exercise even under the best of circumstances, but, when the materials are required to be structurally and electrically stable and to be subject to a variety of environments and applications, it is impossible to imagine a successful outcome. The materials user should choose a challenging system application and pick a system supplier (or suppliers) that will support them in applying their materials expertise to the system in a real-time (scheduled) program.

PROGRAMS AND CONSORTIA

During the 1980s, several U.S. cooperative technical ventures have been implemented. These programs came in response to a number of Japanese efforts that began in the mid-1970s that are perceived to be extremely successful. Competing efforts began to appear in Europe in 1983. Some are governmental in origin, and others were organized privately. In addition, some are solely funding operations, whereas others have established facilities for technology development and demonstration. Some of the programs have a healthy component of packaging technology, but none is focused on packaging and interconnection. In the following paragraphs, several programs are described briefly in the context of this report.

Very-High-Speed Integrated Circuits (VHSIC)

The VHSIC program was intiated by the Department of Defense in 1980 as the program, Advanced Technology Weapons Systems. Funding of more than a billion dollars has been committed to cover 10 years' work. An aggressive processor design program was developed, and contract work was undertaken by Honeywell, Hughes, IBM, TI, TRW, and Westinghouse. Packaging and PWBs are a

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part of the program, and significant advances have been made in chip carrier, pin grid array, and TAB technologies.

Microwave and Millimeter-Wave Monolithic Integrated Circuits (MIMIC)

The MIMIC program was initiated by DOD in 1987 as a spin-off of VHSIC. The purpose is to develop high-speed transmitters and receivers for phased-array radar. Initial funding of $11 million was made available, and work was undertaken by a large number of firms.

Semiconductor Research Corporation (SRC)

The SRC was formed in 1982 to support generic research in universities on behalf of industrial members (initially AT&T, DEC, DuPont, HP, and IBM). Research results and trained engineers are said to be the main products. The funding level was about $20 million in 1986. Government agencies also have begun to provide funds under the SRC program. Packaging research has received considerable emphasis, giving rise to broadly-based thermal management and reliability results.

Microelectronics and Computer Technology Corporation (MCC)

The MCC began operations in 1983 with funding by share owners AMD, Control Data, DEC, Harris, Honeywell, Motorola, National, NCR, RCA, and Sperry (and later Allied, Mostek, Martin Marietta, Rockwell, and BMC). Over 300 employees conduct R&D at the MCC facility in Austin, Texas, and to date over $200 million has been supplied by the member firms. The purpose of MCC is to provide techniques of manufacture and design, and packaging is one of the specifically identified areas of focus. Significant programs in TAB technology are already well established.

SEMATECH

Sematech is a consortium of electronics companies established in 1987 to help U.S. chip makers by developing advanced microelectronic manufacturing technology and equipment. It receives DOD funding in the amount of $100 million, and industrial members will supply funding at the same level. The physical facility is located in Austin, Texas; corporate members include AMD, AT&T, DEC, Harris, HP, Intel, IBM, LSI Logic, Micron, Motorola, National, NCR, Rockwell, and TI.

Other Considerations

Thus, it seems that packaging is an important consideration in the various consortia formed recently to support advanced electronics system

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manufacture. None of the consortia or programs are specifically directed at materials problems or packaging as the primary issue. Therefore, it may be reasonable to work within the structure of the existing consortia and programs to enhance an integrated approach to package and interconnect design in which materials properties and processing are given emphasis at every step. As circuit performance limitations become more and more package-based, the joint programs will gravitate to design factors at the package level, and the materials and combinations of materials involved will be central issues.

An alternative approach could lie in the establishment of a U.S. consortium for pre-competitive research and development for packaging and interconnection materials and processes. Both industry and government funding would be desirable, and the organization could contribute positively to cooperation between materials users and materials suppliers. The materials focus would permit emphasis on synthesis, compounding, processing, reliability, and characterization. Many of the facilities needed are expensive and must be operated by knowledgeable people, and the existence of a materials-oriented consortium would provide economies of scale through pooling of such a capability. Coupling to systems-oriented organizations would be essential. The Table in the Executive Summary illustrates features of the consortium, Sepatech as composed with Sematech. (The Air Force is now attempting to implement such a cooperative.)

It may be perceived that consortia that are concerned with research and applied research aspects of package design can involve cooperation among industrial companies yet have little effect on their ability to compete at the completed system level. It will be important for U.S. companies to learn this lesson in the near future, and programs along these lines deserve encouragement. Somehow, corporate members should receive incentives in some form to place first-class people into the consortia activity.

THE UNIVERSITY ROLE

U.S. universities are outstanding in all areas of engineering and science and, as such, should offer a solid foundation for the electronics industry, including materials issues in packaging and interconnection. At present, gratifying efforts are being made to improve the coupling of academia with industry. However, cultural mismatches impede progress. There is too little understanding of needs and directions by the university community, and industry has been ineffective in establishing lines of (two-way) communication. The consortia can help, but they should realize, as part of their founding concepts, that university interactions require both money and the time commitment of bright, well-connected people.

Engineering departments are the sensible academic points of contact, and benefits accrue to both parties. The high proportion of foreign students in U.S. engineering departments is a concern, particularly for DOD-funded work. There is often a degree of insularity among university departments and colleges, a factor that can make it difficult for science departments to interact effectively with the electronics industry. Competition for funding and for good students is a source of difficulty. Industrial firms, consortia,

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and funding agencies will be well-advised to require reasonable levels of interdisciplinary activity. Again, materials and systems factors cannot be separated. Materials compatibility also is critical, and isolated studies and development of individual materials is unlikely to be as valuable as work in context.

The Engineering Research Centers (ERCs) program of the National Science Foundation could provide an innovative focus for materials aspects of packaging. Industrial participation and interdisciplinary organization are strongly encouraged in the ERC format. Substantial ongoing funding and program accountability are necessary features of the established ERC format. The ERCs bring together many elements that are perceived as essential in a successful pursuit of materials for high-density electronics packaging.

Not to be neglected are the contributions made by the private "think-tank" types of laboratories and institutions such as, Battelle, SRI, A. D. Little, David Sarnoff Research Center, SWRI, and MITRE Corporation. These organizations are funded by government, industry, and foundations to examine various technical and policy questions. They are capable of addressing specific questions that are often too complex or too sensitive for others to undertake without apparent major conflicts of interest.

Universities also are uniquely qualified to integrate the knowledge base for areas such as packaging. Packaging and interconnection involve complex engineering judgments involving diverse properties and structures. Modeling, scaling theory, and physical design fundamentals require a breadth of knowledge and facility for codification that are well-adapted to academic engineering programs. Again, work in isolation is less effective.

Universities also have the culture and freedom to pursue breakthrough technologies, as opposed to incrementally improving the materials that are normally employed. Current materials have real limitations, and ultimate limitations of materials properties in systems terms are now within sight. The payback is becoming increasingly important for adoption of materials with lower dielectric constant, higher electrical conductivity, higher thermal conductivity, and controlled coefficient of thermal expansion. University work can probe and bring understanding to the physical limitations in these characteristics, beginning with long-range programs that address materials structures that are far removed from materials of commerce.

The U.S. electronics industry has many examples of new corporations started by academic staff members that are based on research from university laboratories. It is, perhaps, surprising that more of these firms are not based on materials developments. As materials limits are approached, the opportunities for commercial applications of exotic materials will proliferate. Smaller companies can more easily commercialize materials measured in grams rather than tons, but success will depend on the technical depth and patent protection. University laboratories should be highly successful in this general area, and the near future is ripe for materials development in the electronics packaging business.

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To fully enjoy the fruits of the U.S. academic community, it is important for U.S. industry to improve the industrial-academic interface. Industrial cultures tend to be secretive to an excessive degree, which is harmful to the corporations that the secrecy is designed to protect. Universities are perceived as receptive to industrial collaboration only as a means to funding. It is a fact that engineers and scientists in industry have difficulty in being received as equals in technical discussions with academics. These cultural characteristics are antagonistic to cooperative working relationships, and they can be overcome by participation in projects in which goals and rewards are shared.

Thus, universities represent a U.S. resource that can provide considerable leverage in electronic packaging. Generally, the universities will be most effective in connection with the knowledge base and knowledge integration, but, where revolutionary advances occur, academic research can be translated quickly into commercial products and processes. The materials area today is attractive in this connection. [Note: Recently, the Air Force (Wright R&D Centre) initiated action on a cooperative program to determine the areas in which industry would be willing to participate. Progress has been made in stimulating interest by all parties to work together on packaging problems for mutual benefit, e.g., the MCC-Lehigh University cooperative under the guidance of R.J. Jaccodine of Lehigh University.]

EMIGRATION OF TECHNOLOGY

In the past three decades, the United States has moved from a world position of technical dominance to a position of insecurity and reliance on foreign supply of high-technology goods. The emergence of a world market has eliminated any protection based on geography. Manufacture of many items has moved abroad for reasons of wages, cost of supplies, and entry into foreign markets. Engineering and design are following manufacturing. A major cause is that the U.S. workforce has declined both in education and motivation. All of these factors bear strongly on the future of the U.S. standard of living.

In electronics, the area of consumer products has been taken over mainly by Japan. The Japanese have also become pre-eminent in memory production and in building machines for integrated circuit manufacture. Japan is now mounting a strong effort in the computer area. On the materials side, the Japanese are self-sufficient, but the United States is not. In both ceramics and organic polymers, Japanese firms lead the United States in many important segments. Specifically, electronic ceramic materials come principally from Japan, and now the suppliers have integrated forward into the manufacture of encapsulation modules (e.g., chip carriers and pin grid arrays). They also are dominant in the supply of transfer molding epoxy compounds. In printed wiring boards, multichip modules, chip-board assembly technology, and other interconnection media, both countries appear to be equally capable.

The United States will do well to study and understand the causes of its loss in relative position in these critical technologies. Studies have been conducted for other technology sectors, but the materials chain may have unique features because of its high degree of vertical and horizontal

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fragmentation. Loss of technical capability must be arrested, and domestic production in critical areas must be restored. The present trends leave the United States vulnerable both militarily and financially. For materials, U.S. industries, universities, and technologies are fundamentally strong, but there are signs of weakness. For example, too few young people are attracted to ceramic and polymer science and engineering. Without wishing for government management of business, it would be desirable that encouragement be offered in critical technologies.

PRIVATE FUNDING AND PUBLIC FUNDING

The programs and consortia summarized in this chapter provide interesting examples of funding options, but many forms can be made to work. There are, however, forces at work in the United States today that work against effective long-range approaches to maintaining a high-technology industry. Funding of research and development must be kept reasonably stable. Good programs require a hierarchy of knowledge that takes years to acquire. A field can attract excellent people only if satisfying careers can be predicted with confidence. An infrastructure of communication links supports funding, development efforts, and the manufacturing and marketing that feed back the ongoing supporting funds. Once lost, these links are difficult to rebuild.

Private funding in engineering and research is less robust. Many factors characteristic of U.S. business patterns today inhibit the long-range view necessary for good engineering and research. The mergers, takeovers, and resulting restructurings of major corporations are harmful to the creation of wealth and the maintenance of long-term satisfying employment within the United States. As corporations become more thinly capitalized, they become more susceptible to inevitable fluctuations in business. This leads to episodic retrenchment in long-range, high-technology segments of the business, an effect that is deadly.

Government agency funding may become unstable as a consequence of the deficit, negative balance of payments, and other factors that lead to calls for cuts in the budget. The Department of Defense, however, has been remarkably consistent in its support of engineering and science, and optimism in this regard extends into the Bush administration. So, too, the Department of Energy's National Laboratory system has been well supported, and the National Science Foundation budget permits funding of a number of important technical initiatives. Thus, federal funding appears to be in reasonably good shape in spite of the negative factors mentioned.

The Department of Defense has special reasons to support work on materials for high-density electronic packaging and interconnection. Military circuitry traditionally has been based on IC chips that are contained in hermetic packages. As intrachip communication becomes ever more important as a limitation on circuit performance, the single-chip hermetic packaging requirement becomes increasingly burdensome. Therefore, it is important that new approaches be found that will achieve the most advanced systems requirements without losing the long-term reliability presumed to accrue from hermetic packaging. New materials will play an important role in resolving

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this problem, and enhanced DOD funding can be expected for materials applications in packaging and interconnection.

Mixed government and private funding is a healthy approach and is recommended. Stability can be improved through funding diversity, and national policy needs can be injected into programs at a point of leverage. Somehow, preference should be given to programs directed to the nation's fiscal welfare. For all the right reasons, programs in materials engineering and science, in the context of advanced electronic packaging and interconnection, deserve continuing substantial support and attention.

CONCLUSION

The United States has lost control of major segments of the supply chain of materials that are essential to electronic packaging and interconnection. Furthermore, the organizational culture and legal framework of U.S. industry is such that it is likely that further erosion of the U.S. world position will occur. Thus, the supremacy (or even the viability) of the United States in computers, telecommunications equipment, aircraft, defense hardware, automobiles, space technology, and other key areas could well go the way of the consumer electronics business. New mechanisms and policies must be developed to support and stimulate domestic materials suppliers to work closely with electronics systems houses in long-range programs aimed at recapturing world leadership.

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Appendix A

Glossary of Some Terms and Acronyms Used in This Report

BiCMOS an integration of bipolar and complementary MOS devices on a single chip
Blind via - a via that terminates only on one side of the board
Buried via - a via that terminates on two buried planes
CAD computer-aided design
CAM - computer-aided manufacturing
Captive production- company in-house component production and consumption, not for outside sale
CC - chip carrier
Chip - diced semiconductor active element to be mounted (bonded) in a package [see "die"]
CMOS - complementary metal-oxide-semiconductor
COB - chip on board
CPU - central processing unit
C4 - controlled collapse chip connection
CTE - coefficient of thermal expansion (α) [also see "TCE"]
Die IC chip as cut (diced) from a finished wafer, to be mounted (bonded) in a package [see "chip"]
DIP - dual in-line package
DRAM - dynamic random access memory
ϵ'- real part of dielectric permittivity ($\epsilon'/\epsilon_0 = k$)

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ϵ''-	imaginary part of dielectric permittivity
ϵ_o-	dielectric permittivity of free space
$\tilde{\epsilon}$-	dielectric constant [used interchangeably with k in the text]
ECL	emitter-coupled logic
EMI -	electromagnetic interference
FET	field effect transistor
GaAs	gallium arsenide
HTSC	high-temperature superconductor
IC	integrated circuit
I/O -	inputs/outputs
k	relative dielectric constant (ϵ'/ϵ_o) [used interchangeably with $\tilde{\epsilon}$]
-	thermal conductivity
MCM	multichip module
MLB -	multilayer board
MOS -	metal -oxide-semiconductor
MOSFET -	metal -oxide-semiconductor field effect transistor
NAND	"not" "and" (a logic circuit function designation)
NMOS -	n-channel metal-oxide-semiconductor
NOR -	"not" "or" (a logic circuit function designation)
PCB	printed circuit board [used interchangeably with PWB in the text]
PGA -	pin grid array
P -	glass-phosphosilicate glass used for chip passivation
PNP -	bipolar device layer structure (hole-rich layer/electron-rich layer/hole-rich layer) [transistor]
PTH -	plated through holes
PWB -	printed wiring board [used interchangeably with PCB in the text]

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RIE reactive ion etching
RISC - reduced instruction set computer (or processor)
SMA surface-mount assembly
SCM - single chip modules
SRAM - static random access memory
TAB tape automated bonding
TCE - thermal coefficient of expansion (α) [see "CTE"]
Via a conducting through path perpendicular to the plane of the substrate [see also blind via]
WSI wafer-scale integration

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Appendix B

Some Industry Component Data

The three tables that follow contain some specific industry data from a copyrighted report "Chip Carriers and Other Integrated Circuit Packages: A Review and Update, 1988" prepared by Welterlen, Inc. for client companies. These data are fraction of the comprehensive analysis covered in these annual reports and are presented here with the kind permission of Dr. James W. Welterlen, President of Welterlen, Inc. The tables illustrate the complexity of the chip encapsulation situation.

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Table B-1 DISTRIBUTION OF PACKAGE TYPES*

	ACT 1987				92/87	92/87	EST 1992			
	UNIT	UNITS	ASP	VALUE	ANN GR	ANN GR	UNIT	UNITS	ASP	VALUE
	%	MIL	$	mil $	UNIT %	VALUE %	%	MIL	$	MIL $
CHIP CARRIERS:										
CERAMIC MULTILYR LDLESS	1.15	103.50	1.54	159.39	7.65	9.42	1.10	149.60	1.67	249.95
CERAMIC MULTILYR LEADED	0.35	31.50	3.30	103.95	45.30	40.51	1.50	204.00	2.79	569.32
CERAMIC SLAM LEADLESS	0.26	23.13	0.39	8.91	8.01	9.60	0.25	34.00	0.41	14.08
CERAMIC SLAM LEADED	0.02	1.59	2.50	3.96	47.00	41.12	0.08	10.88	2.04	22.18
CERAMIC SLAM ARRAYS	0.20	18.00	0.33	5.94	35.30	31.65	0.60	81.60	0.29	23.49
CERQUAD LEADED	0.23	21.05	0.50	10.42	45.23	40.45	1.00	136.00	0.42	56.93
CERAMIC FINE PITCH	0.03	2.29	13.50	30.91	60.62	49.05	0.18	24.48	9.29	227.40
PLASTIC PREMOLDED LEADED	0.08	6.93	1.30	9.01	-39.89	-34.18	0.00	0.54	2.05	1.11
PLASTIC POSTMOLD LEADED	5.75	517.50	0.39	199.24	23.65	22.04	11.00	1496.00	0.36	539.33
PLASTIC QUAD FLAT PACK	0.11	10.17	0.75	7.63	121.65	101.26	4.00	544.00	0.46	251.85
PLASTIC LEADLESS	0.00	0.09	0.64	0.06	8.61	7.17	0.00	0.14	0.60	0.08
DUAL-INLINE-PACKAGE:										
CERAMIC SIDE BRAZE DIP	1.62	145.80	2.00	291.60	-4.54	-0.93	0.85	115.60	2.41	278.31
CERDIP	9.80	882.00	0.21	185.22	-4.69	-1.61	5.10	693.60	0.25	170.77
PLASTIC POSTMOLDED DIP	72.50	6525.00	0.09	574.20	2.33	2.43	53.84	7322.24	0.09	647.37
PIN GRID ARRAY:										
CERAMIC MULTILAYER	0.45	40.24	9.15	368.20	24.92	22.78	0.90	122.40	8.39	1027.39
CERAMIC SLAM	0.04	3.36	5.17	17.39	15.12	14.67	0.05	6.80	5.07	34.47
PLASTIC MULTILAYER	0.06	5.08	3.96	20.13	96.67	81.98	1.10	149.60	2.69	401.82
CERAMIC FLAT PACK	0.28	25.20	2.00	50.40	-11.61	-6.95	0.10	13.60	2.58	35.15
PLASTIC SOIC	5.55	499.50	0.15	74.93	30.96	25.64	14.15	1924.40	0.12	234.61
TAB	0.30	27.00	0.33	8.91	58.72	48.18	2.00	272.00	0.23	63.64
COB	0.50	45.00	0.26	11.70	24.76	20.20	1.00	136.00	0.22	29.35
METAL PLATFORM TYPE	0.04	3.60	10.00	36.00	8.61	8.61	0.04	5.44	10.00	54.40
METAL FLAT PACK TYPE	0.16	14.40	7.00	100.80	7.21	7.21	0.15	20.40	7.00	142.80
OTHER	0.53	47.70	-	-	-	-	1.00	136.00	-	-
ALL CC	8.17	735.74	0.73	539.41	29.52	29.38	19.72	2681.24	0.73	1955.73
ALL DIP	83.92	7552.80	0.14	1051.02	1.49	0.85	59.79	8131.44	0.13	1096.45
ALL PGA	0.54	48.69	8.33	405.72	41.77	29.25	2.05	278.80	5.25	1463.68
ALL OTHER	7.36	662.40	-	282.74	30.51	14.65	18.44	2507.84	-	559.96
ALL PLASTIC	84.05	7564.28	0.12	885.19	8.62	18.59	84.09	11436.92	0.18	2076.17
ALL CERAMIC	14.42	1297.66	0.95	1236.28	4.18	16.99	11.71	1592.56	1.70	2709.46
ALL OTHER	1.53	137.70	-	157.41	32.85	13.01	4.19	569.84	-	290.20
ALL IC PACKAGES	100.00	9000.00	0.25	2278.89	8.61	17.37	100.00	13600.00	0.37	5075.83

ACT = actual
ASP = average sale price
- = not applicable or data not available
ANN GR = annual growth rate
EST = estimated
MIL = million

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Table B-2 1987 PACKAGE COSTS*

(COST-CENTS)																		
NUMBER OF CONTACTS	16	18	20	22	24	28	32	36	40	44	48	52	60	64	68	72	84	100
CHIP CARRIERS:																		
CERAMIC MULTILYR LDLESS	44	50	66		77	88	110			155		165			275		375	450
CERAMIC MULTILYR LEADED	90	105	160		165	225	225			300		400			500		800	975
CERAMIC SLAM LEADLESS	24		29		30	40				60		55			135		220	
CERAMIC SLAM LEADED			110		127	149				275		303			457		539	
CERAMIC SLAM ARRAYS	17					22									110			
CERAMIC FINE PITCH												330			430		550	670
CERAMIC FINE PITCH LEADED															1400		1700	
AuALLOY 42 LID/AU/SN 'SEAL	40	50	60		80	80	80			80		80			120		120	120
CERAMIC LID GLASS/SOLDER	12	12	20		20	20	20			25		25			34		34	
CERQUAD LEADED	22		28			39	42			49		60			66		110	300
PLASTIC PREMOLDED LEADED			36	43	43	50				79		94			200		250	
PLASTIC POSTMOLD LEADED		25	25			30				40					60		75	
PLASTIC QUAD FLAT PACK										35	40		50	55	60		80>75	100
PLASTIC LEADLESS	38		39			75				149		192			297		463	
DUAL-IN-LINE PACKAGES:																		
CERAMIC SIDE BRAZE DIP	150		170		220		215		315		400			700	800			
AuALLOY 42 LID/AU/SN SEAL	40	50	60		80	80	80			80		80			120		120	120
CERDIP GOLD DOT BASE	10		20		32		39		64									
CERDIP GOLD SUB BASE	8		11		22		22		33									
CERDIP GLASSED CAP	6		8		12		12		19									
LEAD FRAME AL ON ALLOY 42	2		4		6		8		13									
PLASTIC DIP ALLOY 42 LF	5				10				17									
PLASTIC DIP ALLOY 194 LF	4				9				15									
CERAMIC FLAT PACK	200	210	220		250		275				350			450				
AuALLOY 42 LID/AU/SN SEAL	40	50	60		80	80	80			80		80			120		120	120
CERAMIC LID GLASS/SOLDER	12	12	20		20	20	20			25		25			34		34	
PLASTIC SOIC	12		18		21	23												

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Table B-3 1987 PACKAGE COSTS*

(COST-CENTS)																				
NUMBER OF CONTACTS	68	72	84	100	114	121	132	144	149	156	168	172	180	196	224	244	256	264	299	320
CHIP CARRIERS:																				
CERAMIC	430		550	670		850	935	1075	1100	1160	1265	1300	1350	1475	1750	1875	2875	3000		3650
FINE PITCH CERAMIC			1000			1200			1500					2200	3000					
FINE PITCH LEADED PLASTIC	60		80>75	100		125	150			200			250							
QUAD FLAT PACK																				
PIN GRID ARRAY:																				
CERAMIC	600		800	900		1000	1150	1200	1450				1500		1800					
MULTILAYER CERAMIC		495			743		880													
SLAM 440 AuALLOY 42	120		120		150		180						200							
LID/AU/SN SEAL CERAMIC	34		34																	
LID GLASS/ SOLDER PLASTIC	300	300	400	450		550	600	600							675					
MULTILAYER PLASTIC	170			240				360												
SLAM PLASTIC	275														675					
MOLDED METAL LID	30			30			35				40		45							

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Appendix C

Microprocessor Operating and Structural Parameters

Progress in operating and structural parameters of microprocessors has been rapid in recent years. The progress and future projections are shown in the accompanying figures, C-1 through C-4. These figures were prepared from information drawn from trade journals, forecasting reports, and the direct knowledge of committee members of developments in the field. It should be clear that predictions beyond 10 years are hazardous, at best.

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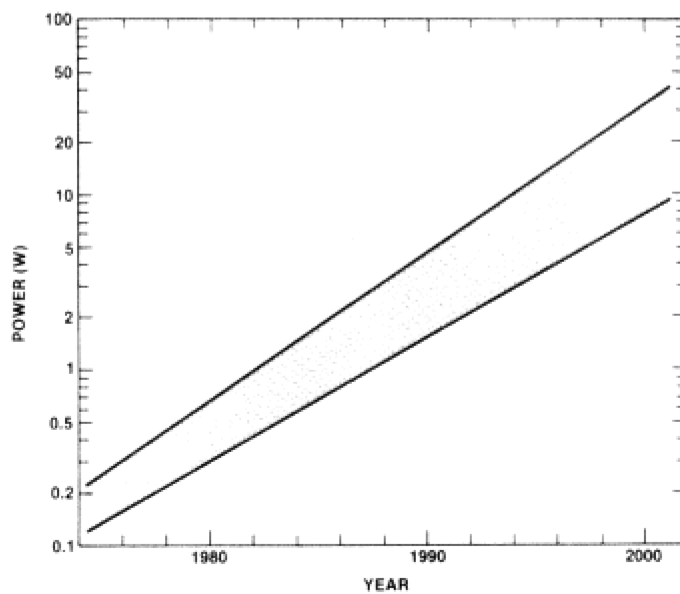

Figure C-1
Microprocessor power requirements: history and forecast.

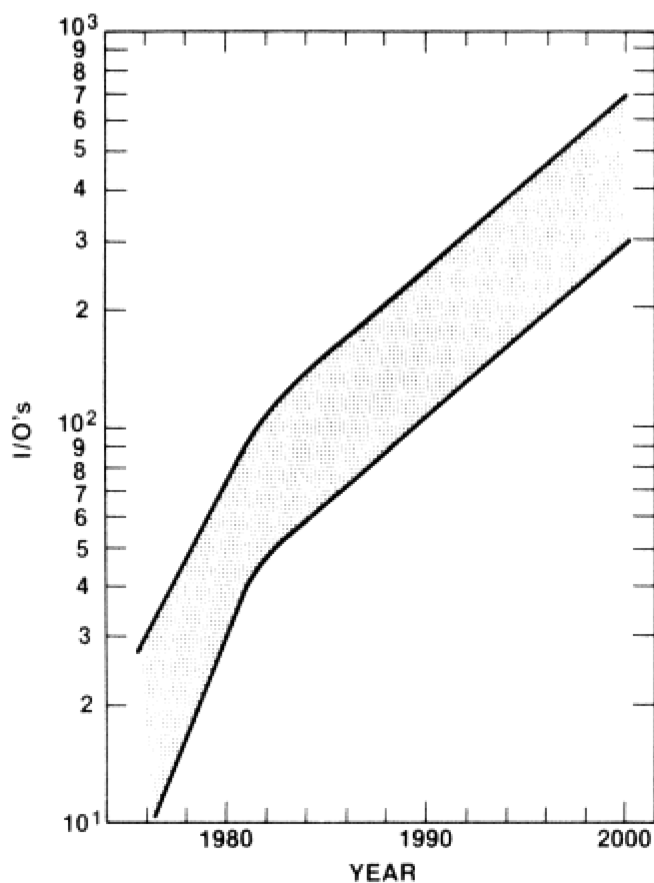

Figure C-2
Microprocessor lead count (I/O): history and forecast.

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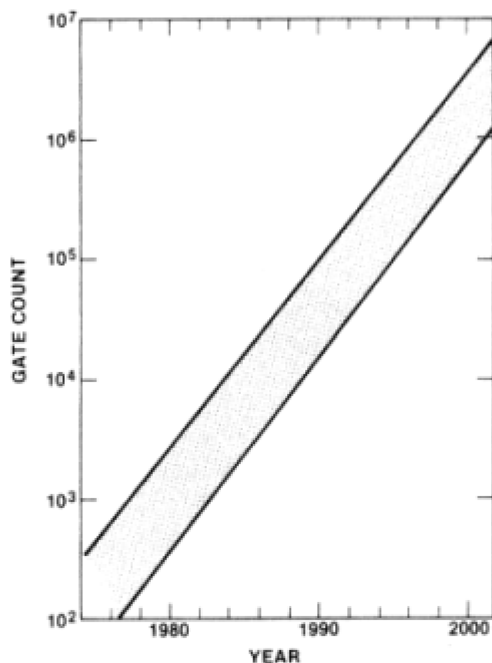

Figure C-3
Microprocessor gate count: history and forecast.

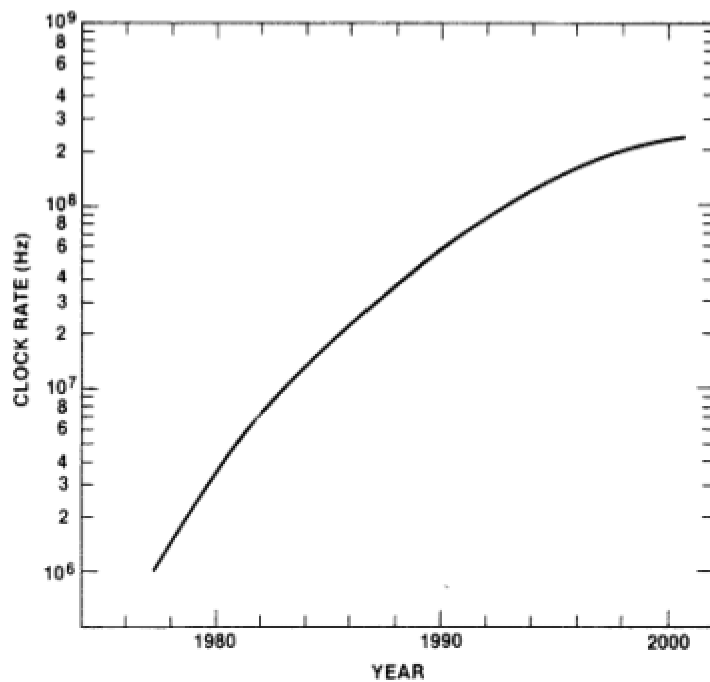

Figure C-4
Microprocessor clock rate: history and forecast.

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Appendix D

Examples of Developments in Board Technologies

Various technologies have been developed for assembling complex circuits employing novel circuit and interconnect designs. Some objectives include attempts to minimize the interconnect lengths and make manufacturing reasonably simple, with the possibility of disassembly for repair and circuit changes. Two of these are shown in the accompanying figures, D-1 and D-2, based on sketches furnished by TRW.

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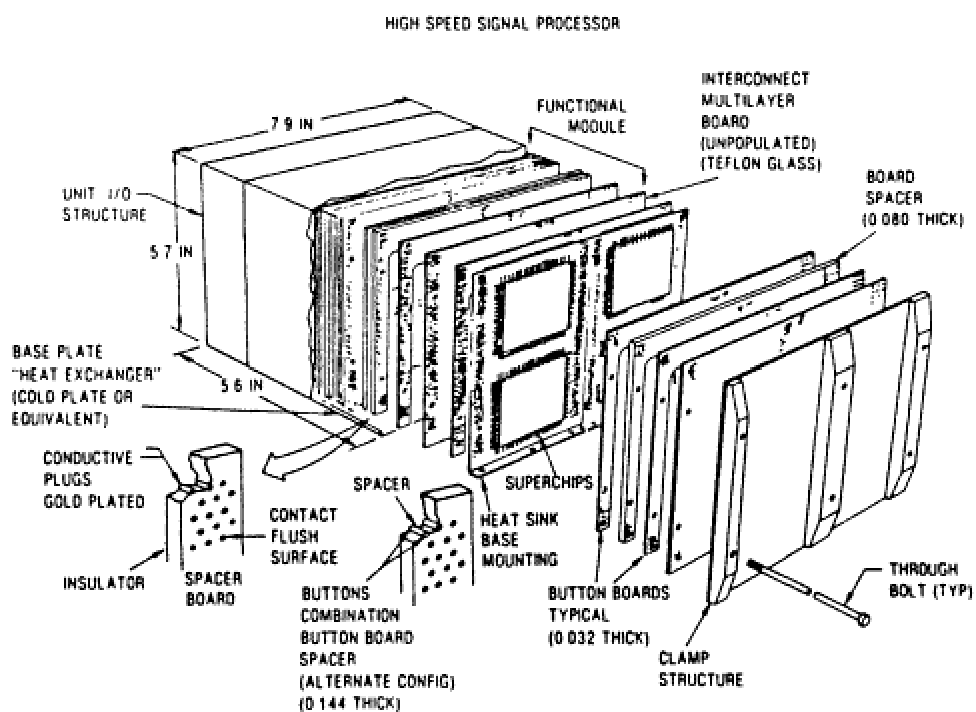

Figure D-1
Circuit assembly employing button board technology for face-to-face interconnection of modules. (Courtesy of TRW)

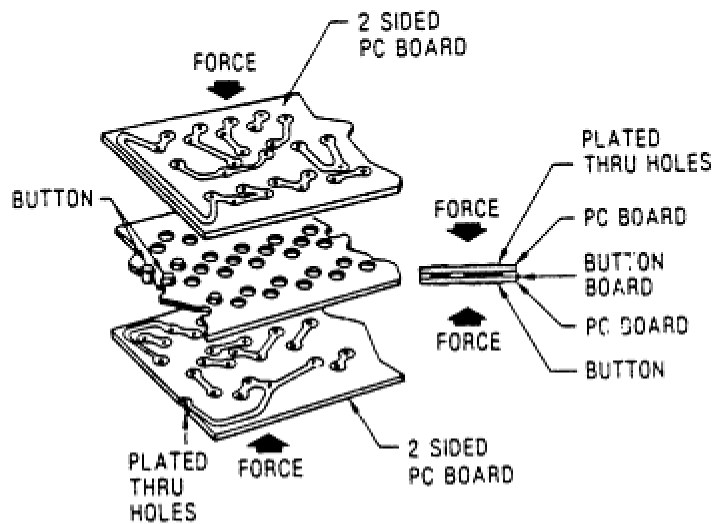

Figure D-2
Button board interconnection concept developed by TRW. (Courtesy of TRW)

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Appendix E

Materials Properties

In the course of preparation of this report, information on packaging and interconnection structures and the materials employed has been compiled. Some materials properties are listed in the accompanying tables E-1 through E-3. Sources of these data ranged from original literature to review articles, monographs, and handbooks, too numerous to be listed here. The reader is reminded that property data found in these reports vary widely, so the values listed should be regarded as representative and indicative of what properties are available for packaging design and manufacture. A recommended source of data for important packaging materials is the "American Institute of Physics Handbook," McGraw-Hill Book Company, New York, an annual publication.

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Table E-1 Interconnection and Packaging Materials: metals

Material	M. P. (°C)	ρ (gr/cm^3)	σ (Ω;-cm)	TCE (ppm/°C)	(W/cm°)	Uses
Aluminum	660	2.7	2.6×10^{-6}	23	2.1	Chip conductor and wire bonds
Gold	1063	19.3	2.4×10^{-6}	14	3.4	Hybrid conductor and wire bonds
Copper	1083	8.9	1.7×10^{-6}	17	3.8	Lead frame and hybrid, PWB, and conductor
Lead	327	11	2×10^{-5}	29	0.3	Solder attach
Molybdenum	2610	10	$4.8\times^{-6}$	4	1.3	Co-fired on ceramic conductor
Tungsten	3380	19	5.5×10^{-6}	4	1.5	Co-fired on ceramic conductor

Table E-2 Interconnection and Packaging Materials: Organic

	max use temp (°C)	ρ (gr/cm^3)	ε'	ε''	ρ (Ω;-cm)	TCE (ppm/°C)	(W/cm°C)	Uses
Epoxy (70% SiO^2)	170	1.8	3.8	0.03	4×10^{16}	20	0.002	Packaging
Epoxy glass (FR-4)	120	1.9	4-5	0.05	10^{11}	15	0.02	Multilayer Board Substrate
Adv. epoxy (resin only)	180	1.2	3.7	0.02	10^{14}	55	0.02	Multilayer Board Substrate
Triazine	250	1.26	3.1	0.001	$>10^{13}$	50	0.002	Hybrid dielectric
BT resin (laminate)	290	1.28	4.0	0.01	10^{15}	15	0.005	Flexible Substrate
Polyimide	400	1.42	3.6	0.01	10^{16}	50	0.0007	Flexible Substrate
Polyimide	310	1.4	3.5-5	0.01	10^{16}	50	0.0007	Interlayer Dielectric

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Table E-3 Interconnection and Packaging Materials: Inorganics

Material	max use temp (°C)	ρ (gr/cm^3)	ϵ'	ϵ''	σ (Ω;-cm°C)	TCE (ppm/°C)	(W/cm°C)	Uses
Alumina (ceramic)	1,600	4.0	9.5	0.003	10^{14}	6.5	0.3	Hybrid substrates/ chip carriers
Silica (fused)	1,100	2.2	3.8	$<10^{-4}$	$>10^{17}$	0.6	0.02	Filler for molding epoxies
Silicon nitride	2,000	3	6	NM	10^{16}	0.8	0.3	Candidate substrates
Aluminum nitride	1,800	3.3	8.9	0.004	10^{13}	4.5	3.2	Candidate substrates
Silicon carbide	2,100	3.2	40	0.2	10^{13}	3.7	2.7	Candidate substrates
Silicon	1,400	2.3	12	NM	V	2.6	1.5	Candidate substrates
Diamond	>3,500	3.5	5.7	NM	$>10^{20}$	0.9	20	Candidate encapsulation
Glass-ceramic	>1,000	>4	7-10	NM	V	>3	0.05	Candidate substrates
Beryllia	1,500	3	7	10^{-3}	10^{14}	6	2.6	Chip carriers

NM = not meaningful
V = varies with composition and impurity level

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Appendix F

Examples of Multichip Modules

Chip modules have increased over the years in operating capability and complexity, and the demands on the materials employed have increased accordingly; these are discussed in Chapter 3. Some examples of multichip modules are shown in the accompanying figures, E-1 through E-7. These were based on figures found in the literature[1] and sketches furnished by IBM and the General Electric Company. The diversity of detail illustrates that work in this area is being pursued widely. The figures are presented here as being representative of the advancements in the state of the art of module design and manufacture. Many similarities can be discerned.

[1] Johnson, Wayne. 1989. Thin Film Multichip Hybrids: An Overview. Proc. Nepcon, p. 655.

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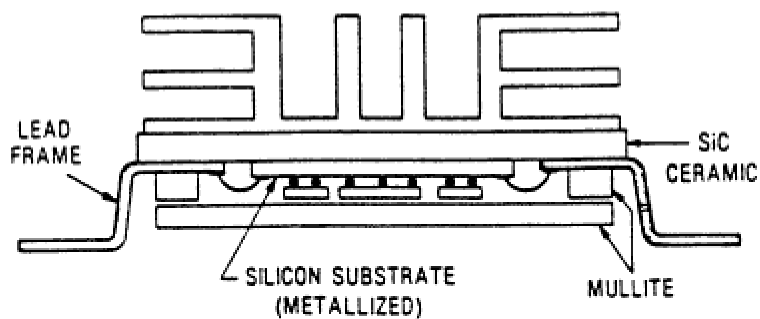

Figure F-1 Ceramic package developed by Hitachi for Silicon Substrate. (After Johnson *)
* Wayne Johnson, Proc. Nepcon, 655 (1989).

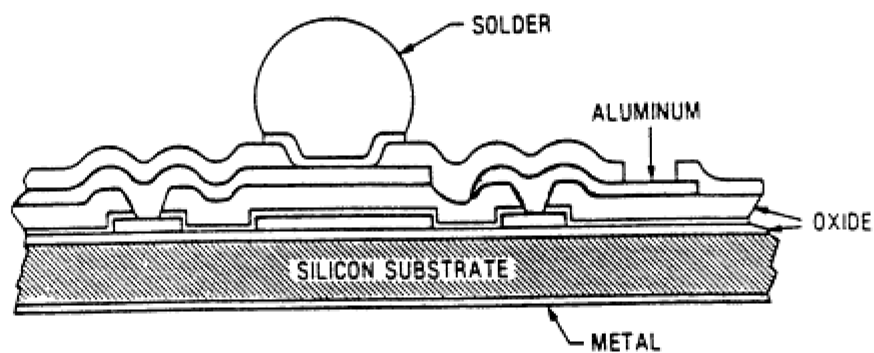

Figure F-2 Silicon-based multichip module developed by Hitachi for ECL RAM. (After Johnson *)
* Wayne Johnson, Proc. Nepcon, 655 (1989).

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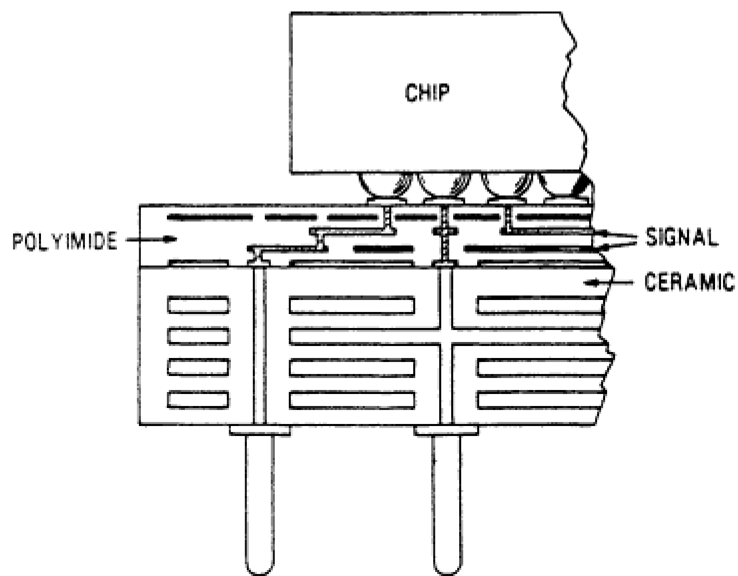

Figure F-3 Thin film on co-fired ceramic multichip module developed by NEC. (After Johnson [*])
[*] Wayne Johnson, Proc. Nepcon, 655 (1989).

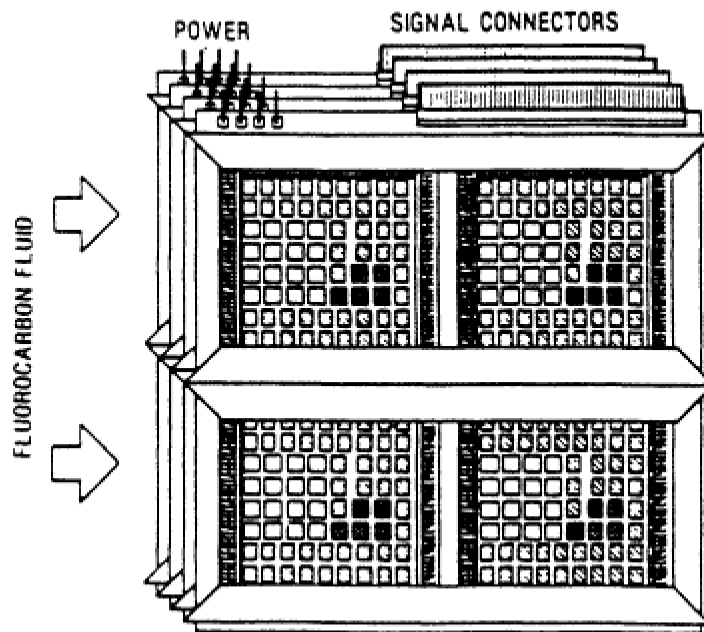

Figure F-4 Three-dimensional assembly of GaAs modules developed by NEC. (After Johnson [*])
[*] Wayne Johnson, Proc. Nepcon, 655 (1989).

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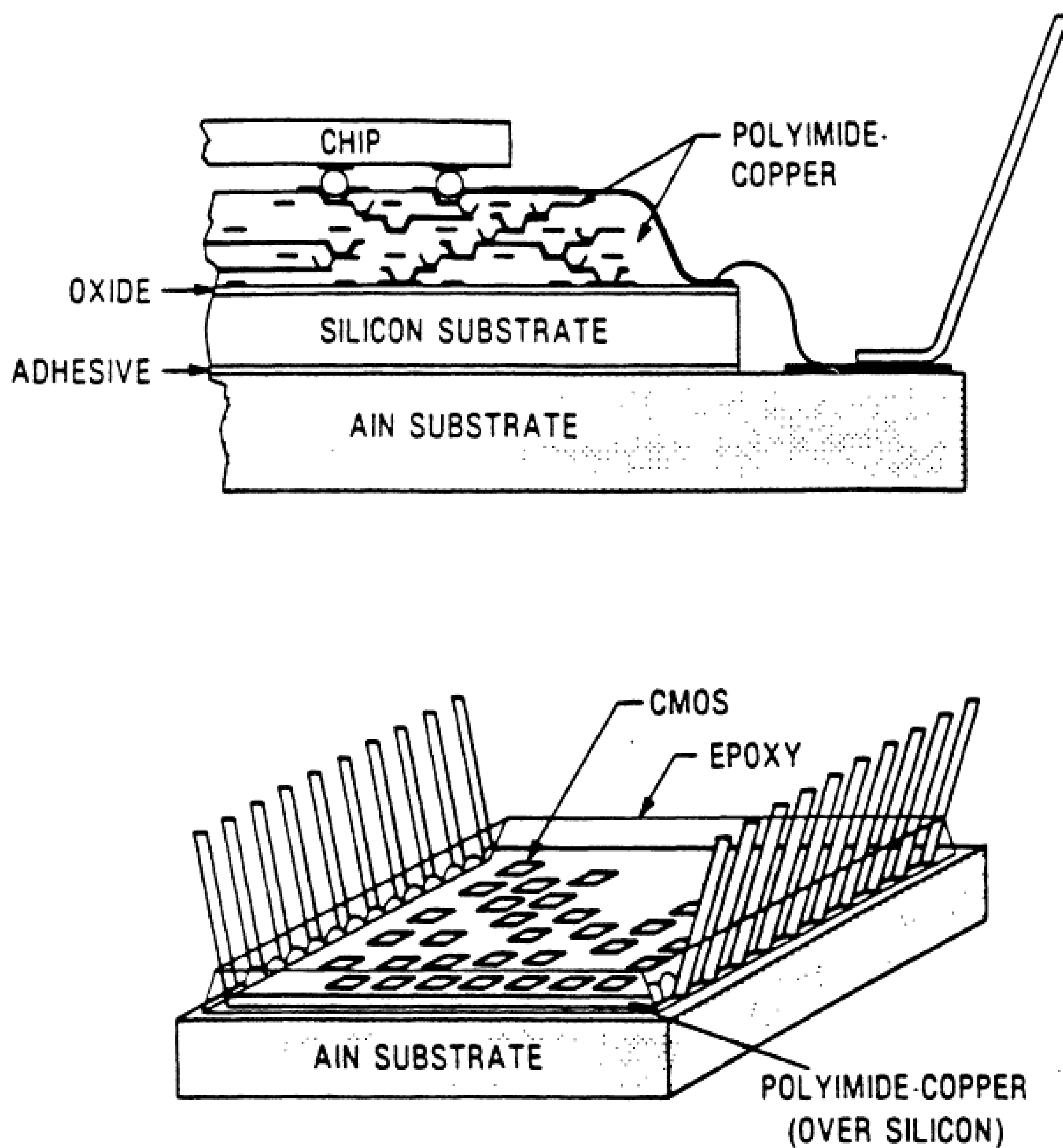

Figure F-5 Multichip module developed by Toshiba. (After Johnson *)
* Wayne Johnson, Proc. Nepcon, 655 (1989).

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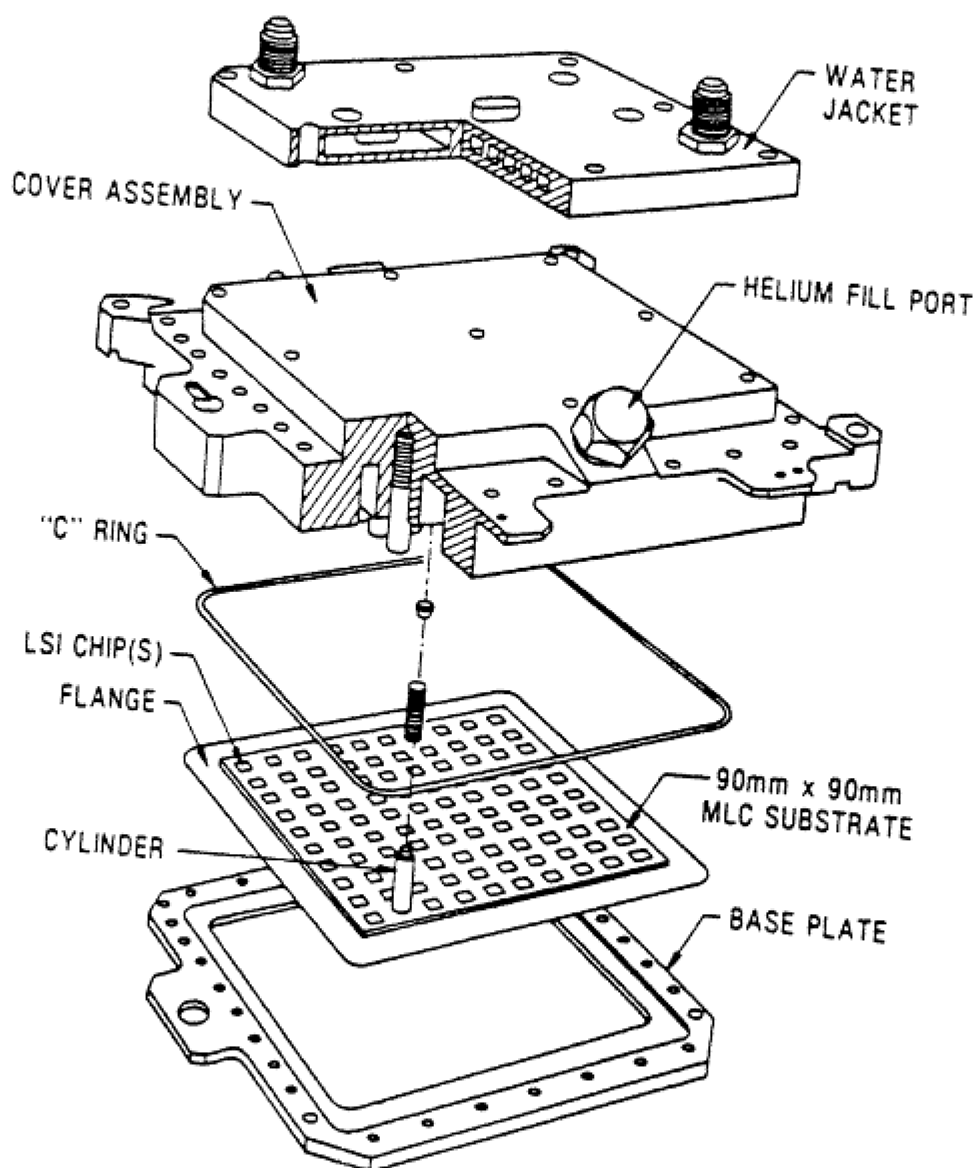

Figure F-6
Thermal condition module developed by IBM. (Courtesy of IBMCorp.)

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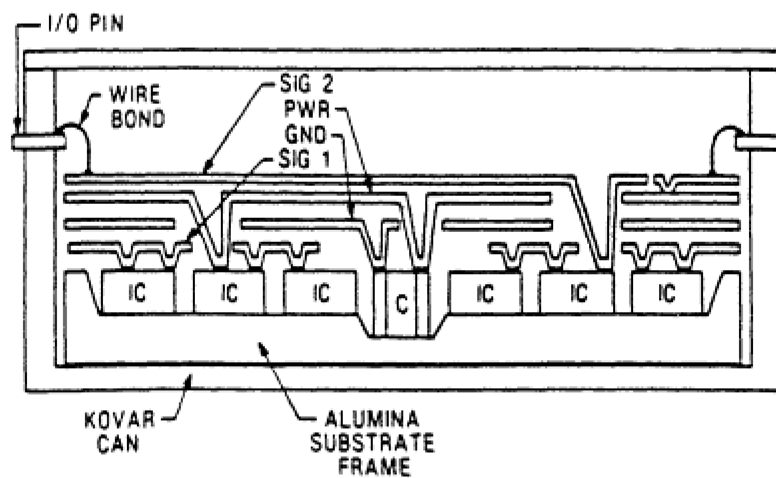

Figure F-7
Cross section of GE module. (Courtesy of General Electric Co.)

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Appendix G

Biographical Sketches of Committee Members

DAVID W. McCALL received a B.S. degree in 1950 in physical chemistry from the University of Wichita and M.S. (1951) and Ph.D. (1953) degrees in chemistry from the University of Illinois. He has been with the AT&T Bell Laboratories since 1953, moving from head of physical chemistry to his present position (since 1973) as director of the chemical research laboratory. He is a member of the American Chemical Society and American Institute of Chemical Engineers and is also a member and fellow of the American Physical Society, the American Association for the Advancement of Science, and the Royal Society of Chemists. In 1984 he was elected to the National Academy of Engineering and has served on a number of Academy study programs. In April 1989, President Bush appointed him chairman of the National Commission on Superconductivity. His areas of expertise include nuclear magnetic resonance, diffusion in liquids, polymer relaxation, dielectric properties, and materials for communications systems.

GENE M. AMDAHL received a B.S. degree in 1948 in engineering physics from South Dakota State University and M.S. and Ph.D. degrees in 1952 in theoretical physics from Cornell University. He received honorary degrees of D.Eng. in 1974 from South Dakota State University and D.Sc. degrees in 1974 from the University of Wisconsin in Madison, in 1980 from Luther College (Iowa), and in 1984 from Augustana College (South Dakota). From 1951 to 1952 he served as research associate at the Wisconsin Alumni Research Foundation (University of Wisconsin), from 1952 to 1955 as senior engineer at the International Business Machines Corporation, as a member of the technical staff in 1956 at Ramo-Wooldridge, Inc., as laboratory manager from 1956 to 1960 at Aeronutronic, Inc., and as director of the computer R&D laboratory from 1960 to 1970 at IBM. He was president and chairman of the board of the Amdahl Corporation from 1970 to 1979. In 1980, he formed Trilogy Systems Corporation and served as chairman of the board until 1987, when he became chairman of the board of ELXSI Corporation. He founded ANDOR Systems Corporation in 1987 and serves as its president and chairman of the board. He was visiting professor from 1965 to 1967 at Stanford University, an IBM fellow from 1965 to 1971, and a lecturer at the NATO School in 1969 and in 1976. He has received numerous honors and awards and was elected to the National Academy of Engineering in 1967. He is a member of the American Physical Society and the Marconi Society (Italy) and is a member and fellow of the Institute of Electrical and Electronics Engineers and the British Computer Society. His areas of expertise include internal machine and system organization of very-high-speed computing systems and the measurement of the characteristics of the workload environment involved.

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DEBORAH D. L. CHUNG received a B.S. degree in engineering and applied science, her M.S. degree in engineering science in 1973 from the California Institute of Technology, and her S.M. degree in 1975 and Ph.D. degree in 1977 in materials science from the Massachusetts Institute of Technology. She worked at Carnegie-Mellon University from 1977 to 1982 as assistant professor and from 1982 to 1986 as associate professor in metallurgical engineering and materials science. She moved to her current position in 1986 as professor of mechanical and aerospace engineering at the State University of New York at Buffalo, where she also serves as director of the Composite Materials Research Laboratory. She was visiting scientist at the Francis Bitter National Magnet Laboratory from 1974 to 1977 and principal investigator on research projects for the Air Force Office of Scientific Research (1978 to 1983), for the National Science Foundation (1980-1984), for the Department of Energy (1986 to 1988), and for the Strategic Highway Research Program (1989). In 1979 she received the Ladd Award from Carnegie-Mellon University, in 1980 the Hardy Gold Medal from the American Institute of Mining, Metallurgical, and Petroleum Engineers, and in 1987 the Teetor Educational Award from the Society of Automotive Engineers. She holds memberships in the American Carbon Society, ASM INTERNATIONAL, American Ceramic Society, and the Society of Automotive Engineers. Her areas of expertise include graphite, carbon fibers, polymer-matrix composites, metal-matrix composites, silicate materials, superconductors, electronic packaging, and plasma deposition.

BARRY K. GILBERT received a B.S. degree in 1965 in electrical engineering from Purdue University and a Ph.D. degree in 1972 in physiology and biophysics from Mayo Graduate School of Medicine and the University of Minnesota. He worked as research assistant at the Mayo Clinic (Mayo Foundation) from 1971 to 1973 and moved through various staff and academic positions at the Mayo Foundation to his present position in 1978 as staff scientist at the Mayo Foundation (Department of Physiology and Biophysics). He was a National Institutes of Health Postdoctoral Fellow from 1972 to 1974. He is a member of the American Physiological Society and the Institute of Electrical and Electronics Engineers and has served on the Materials Research Council of the Defense Advanced Research Analysis Agency since 1985. His areas of expertise include applications of engineering and computational methods to biomedical research and clinical medicine, design of high-performance signal processors, development of computer-aided design software for signal processors, and integrated circuit design.

JACK HILIBRAND received a B.E.E. degree from City College of New York in 1951 and his Sc.D. degree from the Massachusetts Institute of Technology in 1956. He joined the Radio Corporation of America and was a member of the technical staff at RCA Laboratories. In 1961 he transferred to the RCA Semiconductor Division, where he was involved in the design and development of silicon power transistors and MOS and bipolar integrated circuits. In 1971 he joined the RCA Government Systems Division, which is now part of GE Aerospace, where he is a principal staff scientist. He is a fellow of the Institute of Electrical and Electronics Engineers and a member of the American Physical Society. His areas of expertise include integrated circuit design and technology and IC packaging.

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DONALD C. HOFER received a B.S. degree in chemistry at Bethel College in 1961 and a Ph.D. degree in physical chemistry from the University of California in Davis in 1967, which was followed by postdoctoral work at the University of Illinois in Urbana from 1967 to 1969. At the University of Arizona in Tucson he was assistant professor from 1969 to 1974. He joined the IBM Corporation staff in 1974, working first on fundamental studies of materials, then pursued interests in x-ray resists and mask technologies. In 1980, he went to the IBM San Jose Almaden Research Center where, in 1983, he became manager of the polymers for memory and logic group, and in 1988 he moved to New York as manager of advanced polymer materials. In 1989, he returned to the Almaden Research Center on the staff of the director. He is a member of the American Chemical Society. His areas of expertise include x-ray and UV. resists and lithography, mask and alignment technologies, multilayer resists, polymer materials and process development for semiconductor chips and packaging, high-temperature polymers, microstructure of oriented polymers, stress in multilayer polymer-metal structures, and low-permeability chip encapsulants for packaging.

JOSEPH C. LOGUE received his B.E.E. degree in 1944 and his M.E.E. in 1949 in electrical engineering from Cornell University, where he also was instructor over that period. He served as assistant professor (special assignment) from 1949 to 1951 at the Brookhaven National Laboratory. He joined IBM in 1951 as technical engineer and advanced through various managerial positions to director of packaging technology in 1986. He retired from IBM in 1988 and now serves as consultant to Lorex Industries, Inc., and other companies. In 1961 he received the IBM Invention Achievement Award and in 1964 the Outstanding Invention Award, and in 1971 he was made an IBM fellow. He was elected to the National Academy of Engineering in 1983. He is a member of the American Association for the Advancement of Science and the Society of the Sigma Xi and a member and fellow of the Institute of Electrical and Electronics Engineers. His areas of expertise include development and application of new discoveries to advanced digital computers and systems, solid-state devices, and electronic aids to aircraft navigation.

SHIRO MATSUOKA received his M.E. degree in 1955 in mechanical engineering from Stevens Institute of Technology and his M.S.E. and Ph.D. degrees in 1957 and 1959 respectively in mechanical engineering from Princeton University. He was research assistant at Princeton University from 1955 to 1957. He joined AT&T Bell Laboratories in 1959 as a member of the technical staff and in 1974 moved to his present position as head of the plastics research and development department. He was lecturer at Stevens Institute of Technology from 1962 to 1964 and visiting professor from 1964 to 1971. Since 1977 he has been visiting professor at Rutgers University. In 1980 he received the International Award of the Society of Plastics Engineers, and in 1989 he was elected to the National Academy of Engineering. He is a member of the American Chemical Society and the Society of Rheology and a member and fellow of the American Physical Society and the Society of Plastics Engineers. His areas of expertise include mechanical, electrical, and morphological properties of high polymers and molecular relaxation phenomena.

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CONSTANTINE A. NEUGEBAUER received a B.S. degree in 1953 in physical chemistry from Union University and a Ph.D. degree in 1957 in chemistry from the University of Wisconsin in Madison. He joined the General Electric Company in 1957 as research associate and became manager of the semiconductor packaging program in 1976. He is a member of the American Physical Society, the American Vacuum Society, and the Institute of Electrical and Electronics Engineers. He is currently chairman of the Semiconductor Research Corporation's Electronic Packaging Subcommittee. His areas of expertise include calorimetry, thermodynamics, structure and properties of thin films, large-scale integration, hybrids, power semiconductor packaging, and very-large-scale integration packaging.

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